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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008psg

List of Tables

Z80180, Z8S180, Z8L180 MPU Operation 1

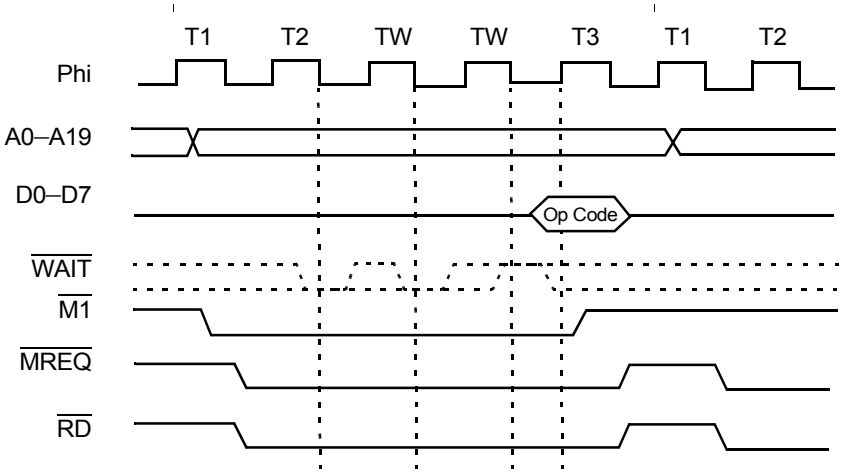

Figure 10. Op Code Fetch (with Wait State) Timing Diagram

Operand and Data Read/Write Timing

The instruction operand and data read/write timing differs from Op Code fetch timing in two ways:

- The $\overline{M1}$ output is held inactive
- The read cycle timing is relaxed by one-half clock cycle because data is latched at the falling edge of T3

Instruction operands include immediate data, displacement, and extended addresses, and contain the same timing as memory data reads.

During memory write cycles the $\overline{MREQ}$ signal goes active in the second half of T1. At the end of T1, the data bus is driven with the write data.

At the start of T2, the $\overline{WR}$ signal is asserted Low enabling the memory. $\overline{MREQ}$ and $\overline{WR}$ go inactive in the second half of T3 followed by disabling of the write data on the data bus.

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
Timer	Data Register Ch 0 L	TMDR0L	XX001100	0CH	159
	Data Register Ch 0 H	TMDR0H	XX001101	0DH	159
	Reload Register Ch 0 L	RLDR0L	XX001110	0EH	159
	Reload Register Ch 0 H	RLDR0H	XX001111	0FH	159
	Timer Control Register	TCR	XX010000	10H	161
	Reserved		XX010001	11H	
			↕	↕	
			XX010011	13H	
	Data Register Ch 1 L	TMDR1L	XX010100	14H	160
	Data Register Ch 1 H	TMDR1H	XX010101	15H	160
	Reload Register Ch 1 L	RLDR1L	XX010110	16H	159
	Reload Register Ch 1 H	RLDR1H	XX010111	17H	159
Others	Free Running Counter	FRC	XX011000	18H	172
	Reserved		XX011001	19H	
			↕	↕	
			XX011111	1FH	

CPU Control Register (CCR: 1FH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Clock Divide	STAND BY/ IDLE Enable	BREXT	LNPHI	STAND BY/ IDLE Enable	LNIO	LNCPU CTL	LNAD/ DATA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	Clock Divide	R/W	0 1	XTAL/2 XTAL/1
6	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 3 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)
5	BREXT	R/W	0 1	Ignore BUSREQ in STANDBY/IDLE STANDBY/IDLE exit on BUSREQ
4	LNPHI	R/W	0 1	Standard Drive 33% Drive on EXTPHI Clock
3	STANDBY /IDLE Mode	R/W	 00 01 10 11	In conjunction with Bit 6 No STANDBY IDLE after SLEEP STANDBY after SLEEP STANDBY after SLEEP 64 Cycle Exit (Quick Recovery)

Bits 5–3

Reserved. Must be 0.

Bits 2–0

With DIM1, bit 1 of DCNTL, these bits control which request is presented to DMA channel 1, as described below:

DIM1	IAR18–16	Request Routed to DMA Channel 1
0	000	$\overline{\text{DREQ1}}$
0	001	ASCI0 Tx
0	010	ASCI1 Tx
0	011	ext CKA0/$\overline{\text{DREQ0}}$
0	10X	Reserved
0	1X0	Reserved
0	111	Reserved
1	000	ext $\overline{\text{DREQ1}}$
1	001	ASCI0 Rx
1	010	ASCI1 Rx
1	011	ext CKA0/$\overline{\text{DREQ0}}$
1	10X	Reserved
1	1X0	Reserved
1	111	Reserved

DMA Operation

This section discusses the three DMA operation modes for channel 0:

- Memory to/from memory
- Memory to/from I/O
- Memory to/from memory mapped I/O

cycle is extended to 4 clocks by automatic insertion of one internal Ti state.

DMAC Channel Priority

For simultaneous $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$ requests, channel 0 has priority over channel 1. When channel 0 is performing a memory to/from memory transfer, channel 1 cannot operate until the channel 0 operation has terminated. If channel 1 is operating, channel 0 cannot operate until channel 1 releases control of the bus.

DMAC and BUSREQ, BUSACK

The $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$ inputs allow another bus master to take control of the Z8X180 bus. $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$ take priority over the on-chip DMAC and suspends DMAC operation. The DMAC releases the bus to the external bus master at the breakpoint of the DMAC memory or I/O access. Since a single byte DMAC transfer requires a read and a write cycle, it is possible for the DMAC to be suspended after the DMAC read, but before the DMAC write. Hence, when the external master releases the Z8X180 bus ($\overline{\text{BUSREQ}}$ High), the on-chip DMAC correctly continues the suspended DMA operation.

Bit Position	Bit/Field	R/W	Value	Description
0	TIE	R/W		**Transmit Interrupt Enable** — TIE must be set to 1 to enable ASCI transmit interrupt requests. If TIE is 1, an interrupt is requested when TDRE is 1. TIE is cleared to 0 during RESET.

CSI/O and RESET

During RESET each bit in the CNTR is initialized as defined in the CNTR register description. CSI/O transmit and receive operations in progress are aborted during RESET. However, the contents of TRDR are not changed.

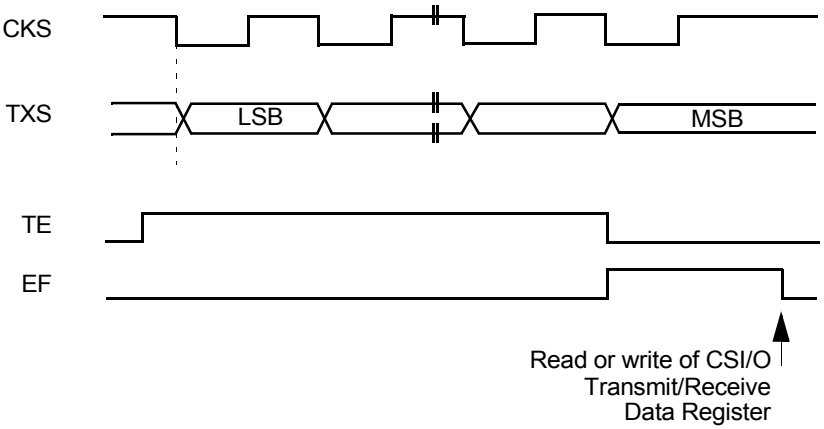

Figure 59. Transmit Timing Diagram–Internal Clock

Table 23. Timer Output Control

TOC1	TOC0	OUTPUT	
0	0	Inhibited	(A18/TOUT pin is selected as an address output function.)
0	1	Toggled	
1	0	0	A18/TOUT pin is selected as a PRT1 output function!
1	1	1	

Figure 64 illustrates timer initialization, count down, and reload timing. Figure 65 depicts timer output (A18/TOUT) timing.

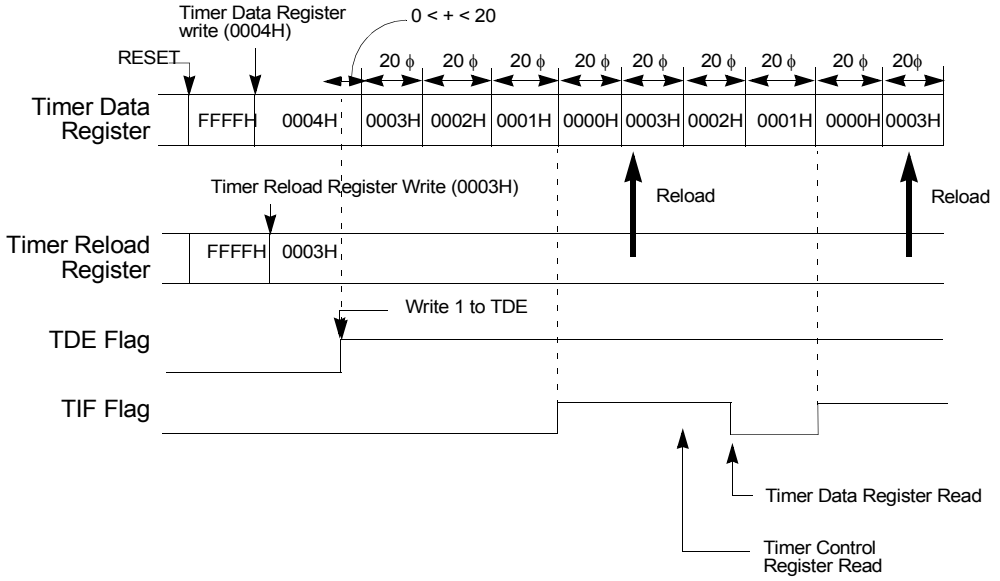

Figure 64. Timer Initialization, Count Down, and Reload Timing Diagram

Immediate (IMMED)

The memory operands are contained within one or two bytes of the instruction, as depicted in Figure 79.

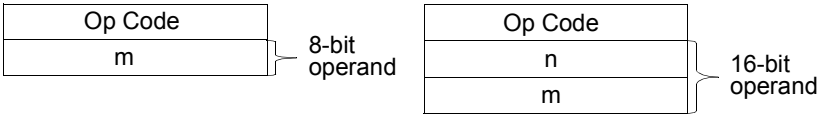

Figure 79. Immediate Addressing

Relative (REL)

Relative addressing mode is only used by the conditional and unconditional branch instructions (refer to Figure 80). The branch displacement (relative to the contents of the program counter) is contained in the instruction.

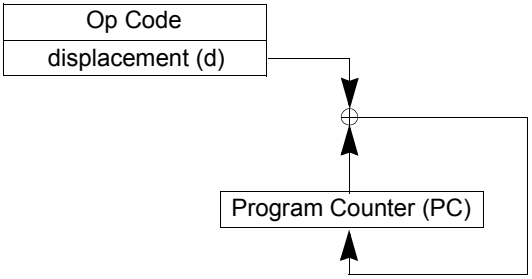

Figure 80. Relative Addressing

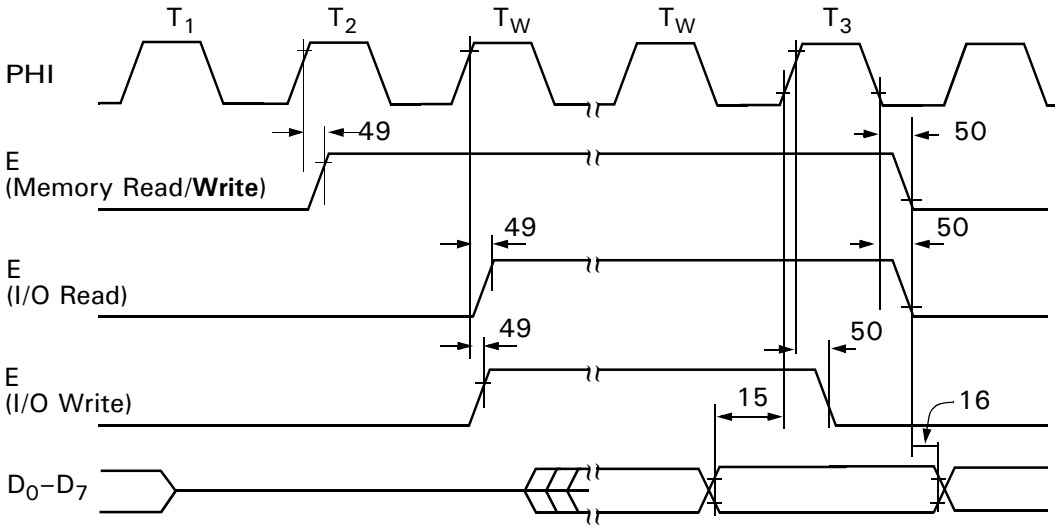

Figure 85. E Clock Timing (Memory R/W Cycle) (I/O R/W Cycle)

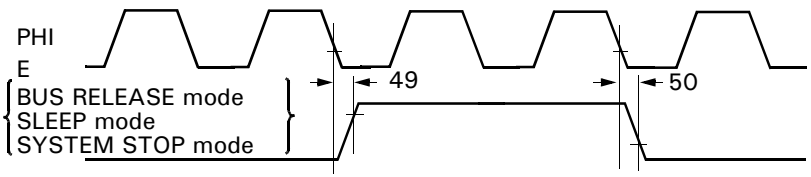

Figure 86. E Clock Timing (BUS RELEASE Mode, SLEEP Mode, and SYSTEM STOP Mode

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
		11 001 011																
		<d>																
		00 001 110																
	RRD	11 101 101						S/D		2	16		↑	↑	R	P	R	•
		01 100 111										Ar b7 b0						
	SLA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 100 g																
	SLA (HL)	11 001 011					S/D			2	13	(HL)M b7 b0	↑	↑	R	P	R	↑
		00 100 110																
	SLA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011										C b7 b0 0						
		<d>																
		00 100 110																
	SLA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 100 110																
	SRA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 101 g																
	SRA (HL)	11 001 011					S/D			2	13	b7 b0 C	↑	↑	R	P	R	↑
		00 101 110																
	SRA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRL g	11 001 011				S/D				2	7	0 b7 b0 C	↑	↑	R	P	R	↑
		00 111 g																

MNEMONICS	Bytes	Machine Cycles	States
SRL (IY+d)	4	7	19
SRL g	2	3	7
SUB (HL)	1	2	6
SUB (IX+d)	3	6	14
SUB (IY+d)	3	6	14
SUB m	2	2	6
SUB g	1	2	4
**TSTIO m	3	4	12
**TST g	2	3	7
TST m**	3	3	9
TST (HL)**	2	4	10
XOR (HL)	1	2	6
XOR (IX+d)	3	6	14
XOR (IY+d)	3	6	14
XOR m	2	2	6
XOR g	1	2	4

Op Code Map

Table 48. 1st Op Code Map Instruction Format: XX

				ww (L0 = ALL)												L0 = 0~7				
				BC	DE	HL	SP									BC	DE	HL	AF	zz
				g (LO = 0~7)												NZ	NC	P0	P	f
				B	D	H	(HL)	B	D	H	(HL)					00H	10H	20H	30H	v
		HI / LO		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
				0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
S (HI = ALL)	B	0000	0	N0P	DJNZj	JR NZ,j	JR NC,j	LD g, s			note 1)	ADD A,s	SUB s	AND s	OR s	RET f				0
	C	0001	1	LD ww, mn												POP zz				1
	D	0010	2	LD (ww), A		LD (mn) ,HL	LD (mn), A									JP f, mn				2
	E	0011	3	INC ww												JP mn	OUT (m),A	EX(SP), HL	DI	3
	H	0100	4	INC g			note1									CALL f, mn				4
	L	0101	5	DEC g			note1									PUSH zz				5
	(HL)	0110	6	LD g,m			note1	note2			HALT	note2	note2	note2	note2	ADD A,m	SUB m	AND m	OR m	6
	A	0111	7	RLCA	RLA	DAA	SCF									RST v				7
	B	1000	8	EXAF,A F'	JR j	JR Z,j	JR C,j	LD g, s				ADC A,s	SBC A,s	XOR s	CP s	RET f				8
	C	1001	9	ADD HL, ww												RET	EXX	JP(HL)	LD SP, HL	9
	D	1010	A	LD A,(ww)		LD HL, (mn)	LD A, (mn)									JP f, mn				A
	E	1011	B	DEC ww												Table2	IN A(m)	EXDE,HL	EI	B
	H	1100	C	INC g												CALL f, mn				C
	L	1101	D	DEC g												CALL mn	note3	Table3	note3	D
	(HL)	1110	E	LD g,m				note2				note2	note2	note2	note2	ADC A,m	SBC A,m	XOR m	CP m	E
	A	1111	F	RRCA	RRA	CPL	CCF									RST v				F
				0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
				C	E	L	A	C	E	L	A					Z	C	PE	M	f
				g(L0 = 8~F)												08H	18H	28H	3BH	v
																LO = 8~F				

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
INIR INDR (If Br=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	BC	DATA	0	1	1	0	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1
JP mn	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
JP f,mn (if is false)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
JP f,mn (If f is true)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
JP (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
JP (IX) JP (IY)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
OTIR OTDR (if Br=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	BC	DATA	1	0	1	0	1	1	1
POP zz	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC3	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
POP IX POP IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
PUSH zz	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC3	TiTi	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	zzH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	zzL	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RETI (Z)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0*5 1	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0*5 1	1	1
	MC3 ~MC5	TiTiTi	*	Z	1	1	1	1	1*5 1	1	1
	MC6	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0*5 0	1	1
	MC7	Ti	*	Z	1	1	1	1	1*5 1	1	1
	MC8	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0*5 0	1	1
	MC9	T1T2T3	SP	data	0	1	0	1	1*5 1	1	1
	MC10	T1T2T3	SP+1	data	0	1	0	1	1*5 1	1	1
RLCA RLA RRCA RRA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
RLC g RL g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
RRC g RR g SLA g SRA g SRL g	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
*5 The upper and lower data show the state of $\overline{M1}$ when $\overline{IOC}$ = 1 and $\overline{IOC}$ = 0 respectively.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RLC (HL) RL (HL) RRC (HL) RR (HL) SLA (HL) SRA (HL) SRL (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	HL	DATA	1	0	0	1	1	1	1
RLC (IX + d) RLC (IY + d) RL (IX + d) RL (IY + d) RRC (IX + d) RRC (IY + d) RR (IX + d) RR (IY + d) SLA (IX + d) SLA (IY + d) SRA (IX + d) SRA (IY + d) SRL (IX + d) SRL (IY + d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2ndOp Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	3rd Op Code Address	3rd Op Code	0	1	0	1	0	1	1
	MC5	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
	MC6	Ti	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	DATA	1	0	0	1	1	1	1
RLD RRD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC7	TiTiTiTi *		Z	1	1	1	1	1	1	1
	MC8	T1T2T3	HL	DATA	1	0	0	1	1	1	1

N

O

P

R