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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008vec

MANUAL OBJECTIVES

This user manual describes the features of the Z8018x MPUs.This manual provides basic programming information for the Z80180/Z8S180/ Z8L180. These cores and base peripheral sets are used in a large family of ZiLOG products. Below is a list of ZiLOG products that use this class of processor, along with the associated processor family. This document is also the core user manual for the following products:

Part	Family
Z80180	Z80180
Z8S180	Z8S180
Z8L180	Z8L180
Z80181	Z80180
Z80182	Z80180, Z8S180*
Z80S183	Z8S180
Z80185/195	Z8S180
Z80189	Z8S180

* Part number-dependant

Intended Audience

This manual is written for those who program the Z8018x.

Manual Organization

The Z8018x User Manual is divided into five sections, seven appendices, and an index.

List of Tables

Z80180, Z8S180, Z8L180 MPU Operation 1

on-chip memory management unit (MMU) with the capability of addressing up to 1 MB of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several *glue* functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z8X180 consume a low amount of power during normal operation, but processors with Z8S180 and Z8L180 class processors also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a *stopped* state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a *stopped* state, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z8X180 provides an excellent solution to system applications requiring high performance, and low power operation.

Figures 1 through 3 illustrate the three pin packages in the Z8X180 MPU family:

- 64-Pin Dual In-line Package (DIP), Figure 1
- 68-Pin Plastic Leaded Chip Carrier (PLCC), Figure 2
- 80-Pin Quad Flat Pack (QFP), Figure 3

Pin out package descriptions for other Z8X180-based products are covered in their respective product specifications.

Figure 4 depicts the block diagram that is shared throughout all configurations of the Z8X180.

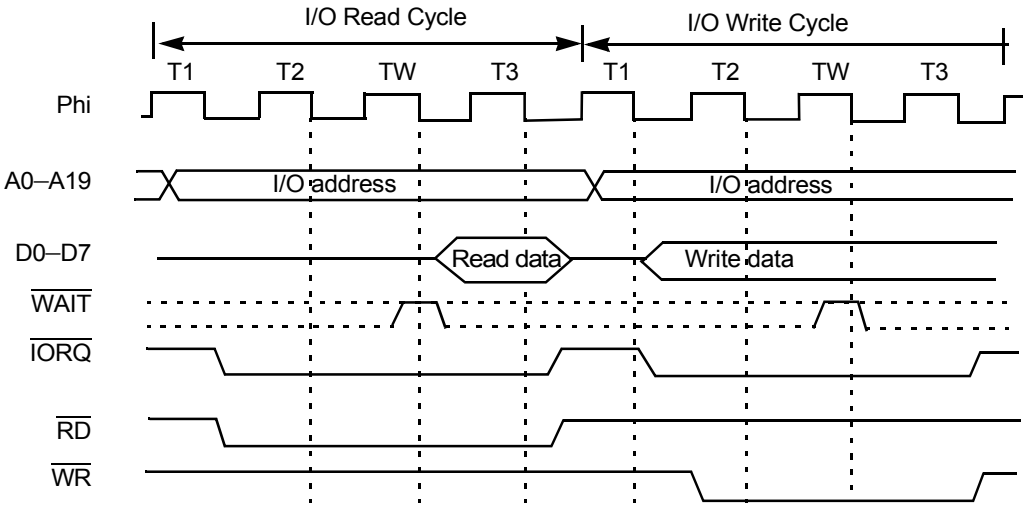


Figure 13. I/O Read/Write Timing Diagram

Basic Instruction Timing

An instruction may consist of a number of machine cycles including Op Code fetch, operand fetch, and data read/write cycles. An instruction may also include cycles for internal processes which make the bus IDLE. The example in Figure 14 illustrates the bus timing for the data transfer instruction LD (IX+d),g.

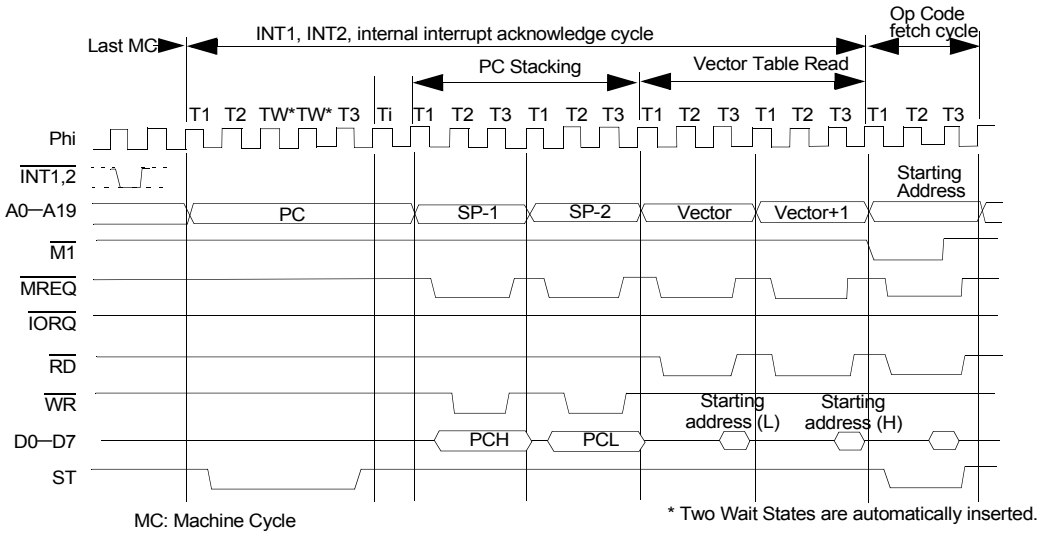


Figure 43. INT1, INT2 and Internal Interrupts Timing Diagram

Dynamic RAM Refresh Control

The Z8X180 incorporates a dynamic RAM refresh control circuit including 8-bit refresh address generation and programmable refresh timing. This circuit generates asynchronous refresh cycles inserted at the programmable interval independent of CPU program execution. For systems which do not use dynamic RAM, the refresh function can be disabled.

When the internal refresh controller determines that a refresh cycle should occur, the current instruction is interrupted at the first breakpoint between machine cycles. The refresh cycle is inserted by placing the refresh address on A0–A7 and the $\overline{\text{RFSH}}$ output is driven Low.

- $\overline{\text{DREQ}}$ Input

  Level- and edge-sense DREQ input detection are selectable.

  $\overline{\text{TEND}}$ Output Used to indicate DMA completion to external devices.

- Transfer Rate

  Each byte transfer occurs every 6 clock cycles. Wait States can be inserted in DMA cycles for slow memory or I/O devices. At the system clock (ϕ) = 6 MHz, the DMA transfer rate is as high as 1.0 megabytes/second (no Wait States).

There is an additional feature disc for DMA interrupt request by DMA END. Each channel has the following additional specific capabilities:

Channel 0

- Memory to memory
- Memory to I/O
- Memory to memory mapped I/O transfers.
- Memory address increment, decrement, no-change
- Burst or cycle steal memory to/from memory transfers
- DMA to/from both ASCI channels
- Higher priority than DMAC channel 1

Channel 1

- Memory to/from I/O transfer
- Memory address increment, decrement

DMAC Registers

Each channel of the DMAC (channel 0, 1) contains three registers specifically associated with that channel.

Table 13. Channel 0 Source

SM1	SM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 14 describes all DMA TRANSFER mode combinations of DM0 DM1, SM0 SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
0	0	0	0	Memory to Memory	SAR0+1, DAR0+1
0	0	0	1	Memory to Memory	SAR0-1, DAR0+1
0	0	1	0	Memory* to Memory	SAR0 fixed, DAR0+ 1
0	0	1	1	I/O to Memory	SAR0 fixed DAR0+1
0	1	0	0	Memory to Memory	SAR0+1, DAR0-1
0	1	0	1	Memory to Memory	SAR0-1,DAR0-1
0	1	1	0	Memory to Memory	SAR0 fixed, DAR0-1
0	1	1	1	I/O to Memory	SAR0 fixed. DAR0-1
1	0	0	0	Memory to Memory*	SAR0+ 1, DAR0 fixed
1	0	0	1	Memory to Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	

In addition, the operation of channel 0 DMA with the on-chip ASCI (Asynchronous Serial Communication Interface) as well as Channel 1 DMA are described.

Memory to Memory—Channel 0

For memory to/from memory transfers, the external $\overline{\text{DREQ0}}$ input is not used for DMA transfer timing. Rather, the DMA operation is timed in one of two programmable modes – BURST or CYCLE STEAL. In both modes, the DMA operation automatically proceeds until termination (shown by byte count-BCR0) = 0.

In BURST mode, the DMA operation proceeds until termination. In this case, the CPU cannot perform any program execution until the DMA operation is completed. In CYCLE STEAL mode, the DMA and CPU operation are alternated after each DMA byte transfer until the DMA is completed. The sequence:

- 1 CPU Machine Cycle
- DMA Byte Transfer

is repeated until DMA is completed. Figure 46 describes CYCLE STEAL mode DMA timing.

4. Specify whether $\overline{\text{DREQ1}}$ is level- or edge- sense in the DMS1 bit in DCNTL.
5. Enable or disable DMA termination interrupt with the DIE1 bit in DSTAT.
6. Program DE1 = 1 (with $\overline{\text{DWE1}}$ = 0 in the same access) in DSTAT and the DMA operation with the external I/O device begins using the external $\overline{\text{DREQ1}}$ input and $\overline{\text{TEND1}}$ output.

DMA Bus Timing

When memory (and memory mapped I/O) is specified as a source or destination, $\overline{\text{MREQ}}$ goes Low during the memory access. When I/O is specified as a source or destination, $\overline{\text{IORQ}}$ goes Low during the I/O access.

When I/O (and memory mapped I/O) is specified as a source or destination, the DMA timing is controlled by the external $\overline{\text{DREQ}}$ input and the $\overline{\text{TEND}}$ output indicates DMA termination

Note: External I/O devices may not overlap addresses with internal I/O and control registers, even using DMA.

For I/O accesses, one Wait State is automatically inserted. Additional Wait States can be inserted by programming the on-chip wait state generator or using the external $\overline{\text{WAIT}}$ input.

Note: For memory mapped I/O accesses, this automatic I/O Wait State is not inserted.

For memory to memory transfers (channel 0 only), the external $\overline{\text{DREQ0}}$ input is ignored. Automatic DMA timing is programmed as either BURST or CYCLE STEAL.

When a DMA memory address carry/borrow between bits A15 and A16 of the address bus occurs (crossing 64KB boundaries), the minimum bus

Bit Position	Bit/Field	R/W	Value	Description
4	FE	R		**Framing Error** — If a receive data byte frame is delimited by an invalid stop bit (that is, 0, should be 1), FE is set to 1. FE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
3	RIE	R/W		**Receive Interrupt Enable** — RIE must be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, if any of the flags RDRF, OVRN, PE, or FE become set to 1, an interrupt request is generated. For channel 0, an interrupt is also generated by the transition of the external $\overline{\text{DCD0}}$ input from Low to High.
2	CTS1E	R/W		**Channel 1 $\overline{\text{CTS}}$ Enable** — Channel 1 has an external $\overline{\text{CTS1}}$ input which is multiplexed with the receive data pin (RXS) for the CSI/O (Clocked Serial I/O Port). Setting CTS1E to 1 selects the $\overline{\text{CTS1}}$ function and clearing CTS1E to 0 selects the RXS function.
1	TDRE	R		**Transmit Data Register Empty** — TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. When the external $\overline{\text{CTS}}$ input is High, TDRE is reset to 0.
0	TIE	R/W		**Transmit Interrupt Enable** — TIE must be set to 1 to enable ASCI transmit interrupt requests. If TIE is 1, an interrupt is requested when TDRE is 1. TIE is cleared to 0 during RESET.

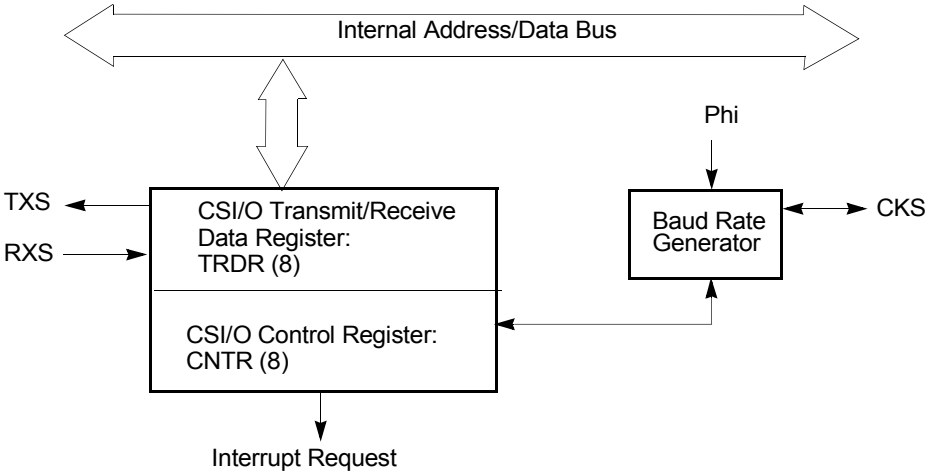


Figure 57. CSI/O Block Diagram

CSI/O Registers Description

CSI/O Control/Status Register (CNTR: I/O Address 0AH)

CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

CSI/O Control/Status Register (CNTR: 0AH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	EF	EIE	RE	TE	—	SS2	SS1	SS0
R/W	R	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

PRT Operation Notes

- TMDR data is accurately read without stopping down counting by reading the lower (TMDRnL*) and higher (TMDRnH*) bytes in that order. Also, TMDR is read or written by stopping the down counting.[1]

  Take care to ensure that a timer reload does not occur during or between lower (RLDRnL*) and higher (RLDRnH*) byte writes. This may be guaranteed by system design/timing or by stopping down counting (with TMDR containing a non-zero value) during the RLDR updating. Similarly, in applications where TMDR is written at each TMDR overflow, the system/software design must guarantee that RLDR can be updated before the next overflow occurs. Otherwise, time base inaccuracy occurs.

- During RESET, the multiplexed A18/TOUT pin reverts to the address output. By reprogramming the TOC1 and TOC0 bits, the timer output function for PRT channel 1 is selected. The following paragraph describes the initial state of the TOUT pin after TOC1 and TOC0 are programmed to select the PRT channel 1 timer output function.

  PRT (channel 1) has not counted down to 0.

  If the PRT has not counted down to 0 (timed out), the initial state of TOUT depends on the programmed value in TOC1 and TOC0.

Secondary Bus Interface

E clock Output Timing

The Z8X180 also has a secondary bus interface that allows it to easily interface with other peripheral families.

1. *n = 0, 1

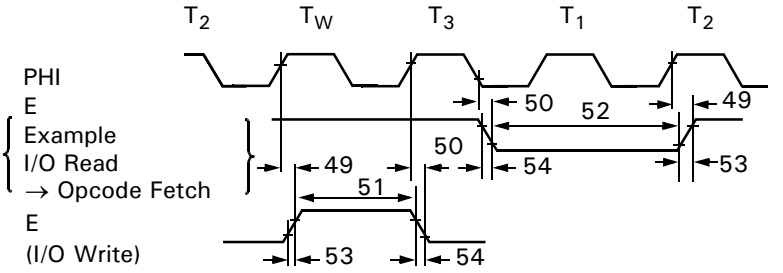


Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

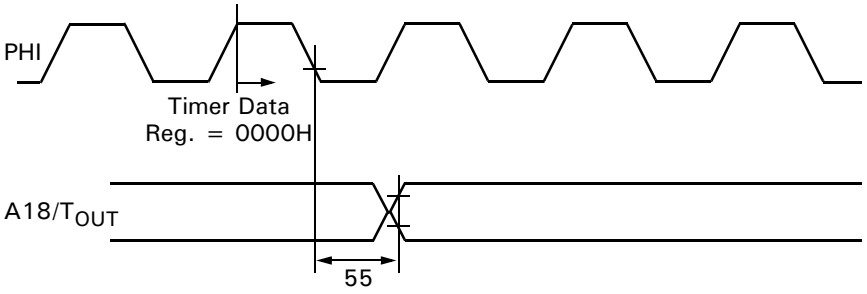


Figure 88. Timer Output Timing

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	XOR (IY + d)	11 111 101			S			D		3	14	$Ar \oplus + (IY + d))_M \rightarrow Ar$	↑	↑	R	P	R	R
		10 101 110 <d>																

Table 39. Rotate and Shift Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Rotate and Shift Data	RL A	00 010 1111						S/D		1	3		•	•	R	•	R	↑
	RL g	11 001 011 00 010 g				S/D				2	7		↑	↑	R	P	R	↑
	RL (HL)	11 001 011 00 010 110					S/D			2	13		↑	↑	R	P	R	↑
	RL (IX + d)	11 011 101 11 001 011 <d> 00 010 110			S/D					4	19		↑	↑	R	P	R	↑
	RL (IY + d)	11 111 101 11 001 011 <d> 00 010 110			S/D					4	19		↑	↑	R	P	R	↑
	RLC A	00 000 111						S/D		1	3		•	•	R	•	R	↑
	RLC g	11 001 011 00 000 g				S/D				2	7		↑	↑	R	P	R	↑
	RLC (HL)	11 001 011 00 000 110					S/D			2	13		↑	↑	R	P	R	↑

Table 46. I/O Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	OTIMR**	11 101 101 10 010 011					S		D	2	16 (Br ≠ 0) 14 (Br = 0)	$(HL)_M \rightarrow (00C)_I$ $HL_R + 1 \rightarrow HL_R$ Q $Cr + 1 \rightarrow Cr$ $Br-1 \rightarrow Br$ Repeat Q until Br = 0 $Cr \rightarrow A0 \sim A7$ $00 \rightarrow A8 \sim A16$	R	S (5)	R	S	↑ (6)	R
	OUTD	11 101 101 10 101 011						S	D	2	12	$(HL)_M \rightarrow (BC)_1$ $HL_R-1 \rightarrow HL_R$ $Br-1 \rightarrow Br$ $Cr \rightarrow A0 \sim A7$ $Br \rightarrow A8 \sim A16$	X	↑	X	X	↑	X

(5) Z = 1 : Br-1 = 0
Z = 0 : Br-1 ≠ 0
(6) N = 1: MSB of Data = 1
N = 0 : MSB of Data = 0

Table 50. 2nd Op Code Map Instruction Format: ED XX

						ww (L0 = ALL)												
						BC	DE	HL	SP									
		G (L0 = 0~7)																
		B	D	H		B	D	H										
HI / LO		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	IN0 g, (m)				IN g, (C)						LDI	LDIR					0
0001	1	OUT0 (m),g				OUT (C),g						CPI	CPIR					1
0010	2					SBC HL, ww						INI	INIR					2
0011	3					LD (mn), ww				OTIM	OTIM R	OUTI	OTIR					3
0100	4	TST g			TST (HL)	NEG		TST m	TSTIO m									4
0101	5					RETN												5
0110	6					IM 0	IM 1		SLP									6
0111	7					LD I,A	LD A,I	RRD										7
1000	8	IN0 g, (m)				IN g, (C)						LDD	LDDR					8
1001	9	OUT0 (m), g				OUT (C) , g						CPD	CPDR					9
1010	A					ADC HL,ww						IND	INDR					A
1011	B					LD ww, (mn)				OTD M	OTD MR	OUTD	OTDR					B
1100	C	TST g				MLT ww												C
1101	D					RETI												D
1110	E						IM 2											E
1111	F					LDR, A	LD A,R	RLD										F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
		C	E	L	A	C	E	L	A									
		g (L0 = 8~F)																

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
ADD A,g ADC A,g SUB g SBC A,g AND g OR g XOR g CP g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
ADD A,m ADC A,m SUB m SBC A,m AND m OR m XOR m CP m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
ADD A, (HL) ADC A, (HL) SUB (HL) SBC A, (HL) AND HU OR (HL) XOR (HL) CP (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	HL	DATA	0	1	0	1	1	1	1
ADD A, (IX+ d) ADD A, (IY+d) ADC A, (IX+d) ADC A, (IY+d) SUB (lX+d) SUB (IY+d) SBC A, (IX+ d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
SBC A, (IY+ d) AND (IX+d)	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1

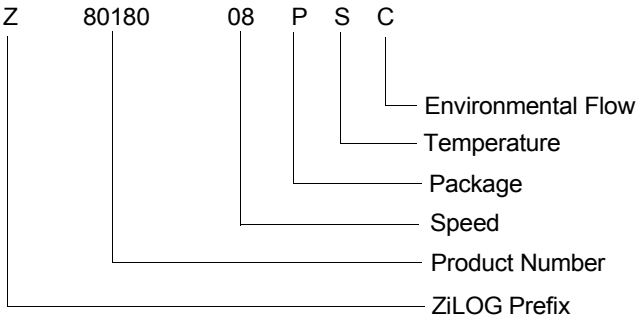
Table 52. Interrupts (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{INT0}$ Mode 2	MC1	T1T2TW TWT3	Next Op Code Address (PC)	Vector	1	1	1	0	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1		1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3 T1T2,TW	I, Vector+1	DATA	0	1	0	1	1	1	1
$\overline{INT1}$ $\overline{INT2}$ Internal Interrupts	MC1	T1T2,TW TWT3	Next Op Code Address (PC)		1	1	1	1	1	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	I, Vector+1	DATA	0	1	0	1	1	1	1

ORDERING INFORMATION

Codes

- Package
  P = Plastic Dip
  V = Plastic Chip Carrier
  F = Quad Flat Pack
- Temperature
  S = 0°C to +70°C
  E = -40°C to 100°C
- Speed
  06 = 6 MHz
  08 = 8 MHz
  10 = 10 MHz
- Environmental
  C = Plastic Standard
- Example
  Z8018008PSC is an 80180 8 MHz, Plastic DIP, 0°C to 70°C, Plastic Standard Flow.



A

B

C