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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

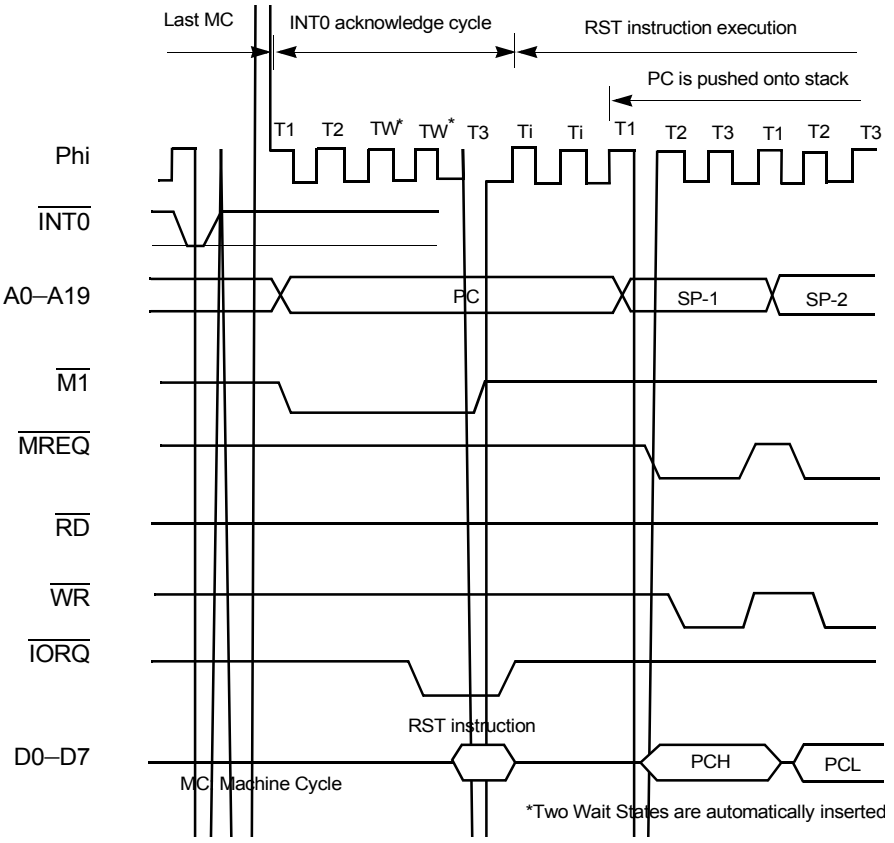
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008vec00tr

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
INT	IL Register (Interrupt Vector Low Register)	IL	XX110011	33H	67
	INT/TRAP Control Register	ITC	XX110100	34H	68
	Reserved		XX110101	35H	
Refresh	Refresh Control Register	RCR	XX110110	36H	88
	Reserved		XX110111	37H	
MMU	MMU Common Base Register	CBR	XX111000	38H	61
	MMU Bank Base Register	BBR	XX111001	39H	62
	MMU Common/Bank Area Register	CBAR	XX111010	3AH	60
I/O	Reserved		XX111011	3BH	
			↕	↕	
			XX111101	3DH	
	Operation Mode Control Register	OMCR	XX111110	3EH	15
	I/O Control Register	ICR	XX111111	3FH	42



Note: The TRAP interrupt occurs if an invalid instruction is fetched during Mode 0 interrupt acknowledge. (Reference Figure 36.)

Figure 36. $\overline{\text{INT0}}$ Mode 0 Timing Diagram

INT0 Mode 1

When $\overline{\text{INT0}}$ is received, the PC is stacked and instruction execution restarts at logical address `0038H`. Both IEF1 and IEF2 flags are reset to `0`,

disabling all maskable interrupts. The interrupt service routine normally terminates with the EI (Enable Interrupts) instruction followed by the RETI (Return from Interrupt) instruction, to reenable the interrupts. Figure 37 depicts the use of $\overline{\text{INT0}}$ (Mode 1) and RETI for the Mode 1 interrupt sequence.

Figure 37. INT0 Mode 1 Interrupt Sequence

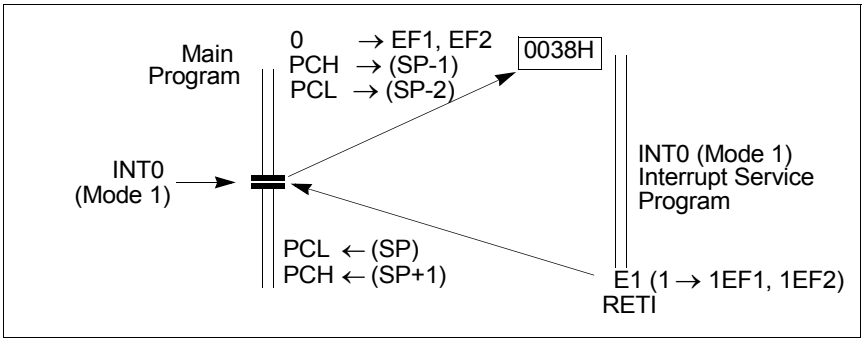


Figure 38 illustrates $\overline{\text{INT0}}$ Mode 1 Timing.

The vector table address is located on 256 byte boundaries in the 64KB logical address space programmed in the 8-bit Interrupt Vector Register (1). Figure 39 depicts the $\overline{\text{INT0}}$ Mode 2 Vector acquisition.

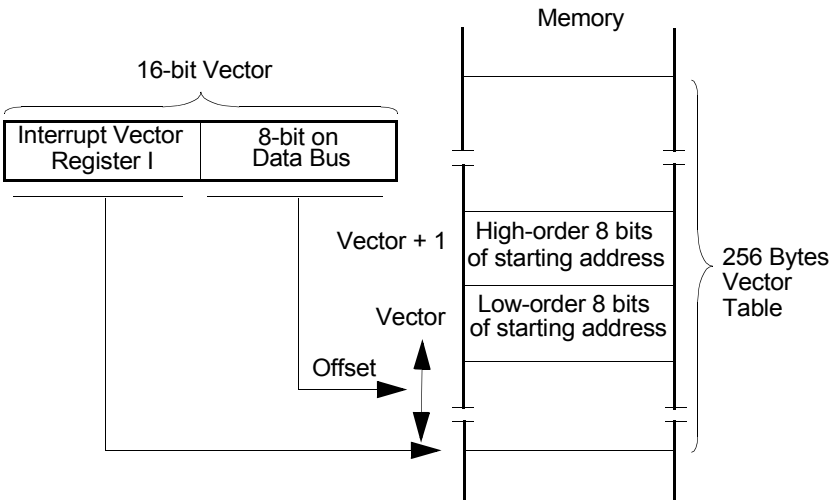


Figure 39. INT0 Mode 2 Vector Acquisition

During the $\overline{\text{INT0}}$ Mode 2 acknowledge cycle, the low-order 8 bits of the vector is fetched from the data bus at the rising edge of T3 and the CPU acquires the 16-bit vector.

Next, the PC is stacked. Finally, the 16-bit restart address is fetched from the vector table and execution begins at that address.

Note: External vector acquisition is indicated by both $\overline{\text{MI}}$ and $\overline{\text{IORQ}}$ LOW. Two Wait States (TW) are automatically inserted for external vector fetch cycles.

During RESET the Interrupt Vector Register (I) is initialized to `00H` and, if necessary, should be set to a different value prior to the occurrence of a Mode 2 $\overline{\text{INT0}}$ interrupt. Figure illustrates $\overline{\text{INT0}}$ interrupt Mode 2 Timing.

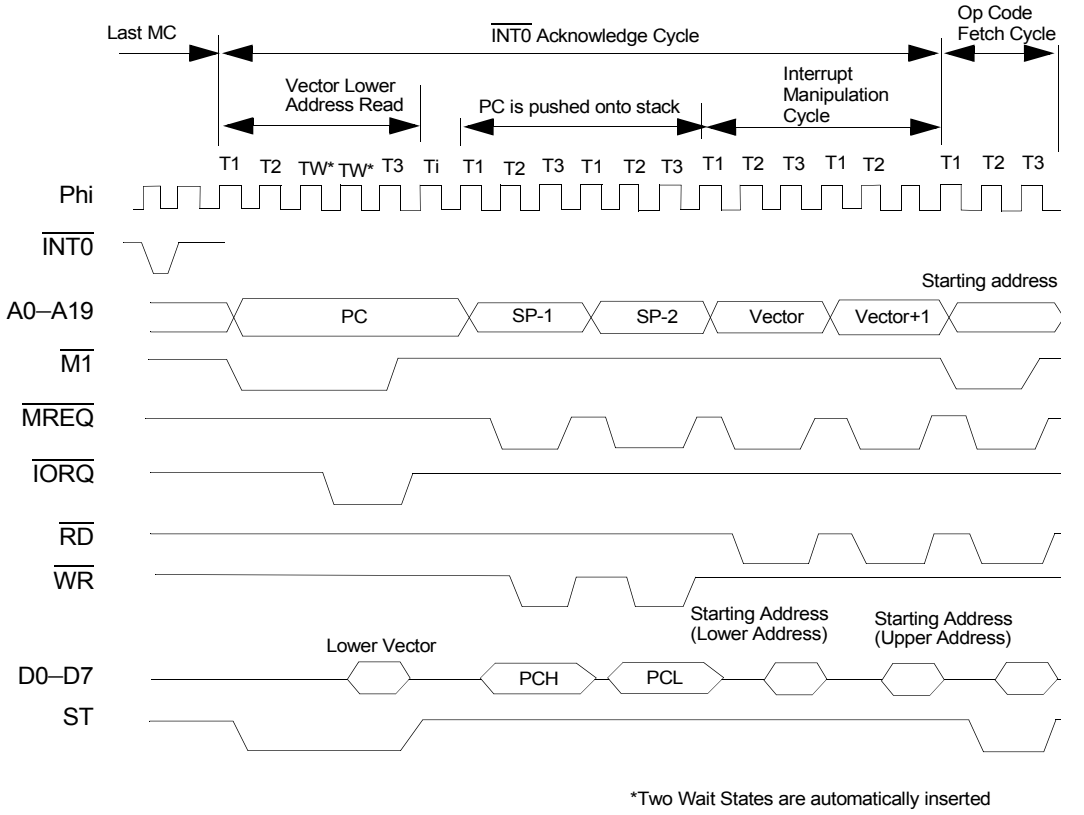


Figure 40. $\overline{\text{INT0}}$ Interrupt Mode 2 Timing Diagram

$\overline{\text{INT1}}$, $\overline{\text{INT2}}$

The operation of external interrupts $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ is a vector mode similar to $\overline{\text{INT0}}$ Mode 2. The difference is that $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ generate the low-order byte of vector table address using the IL (Interrupt Vector Low) register rather than fetching it from the data bus. This difference is

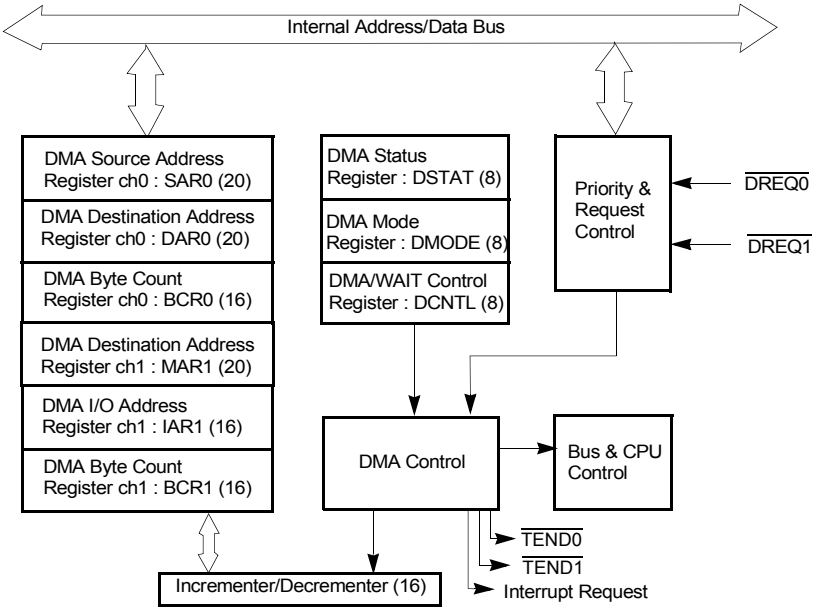


Figure 45. DMAC Block Diagram

DMAC Register Description

DMA Source Address Register Channel 0 (SAR0 I/O Address = 20H to 22H)

Specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O.

Memory to I/O (Memory Mapped I/O) — Channel 0

For memory to/from I/O (and memory to/from memory mapped I/O) the $\overline{\text{DREQ0}}$ input is used to time the DMA transfers. In addition, the $\overline{\text{TEND0}}$ (Transfer End) output is used to indicate the last (byte count register BCR0 = 00H) transfer.

The $\overline{\text{DREQ0}}$ input can be programmed as level- or edge-sensitive.

When level-sense is programmed, the DMA operation begins when $\overline{\text{DREQ0}}$ is sampled Low. If $\overline{\text{DREQ0}}$ is sampled High, after the next DMA byte transfer, control is relinquished to the Z8X180 CPU. As illustrated in Figure 47, $\overline{\text{DREQ0}}$ is sampled at the rising edge of the clock cycle prior to T3, (that is, either T2 or Tw).

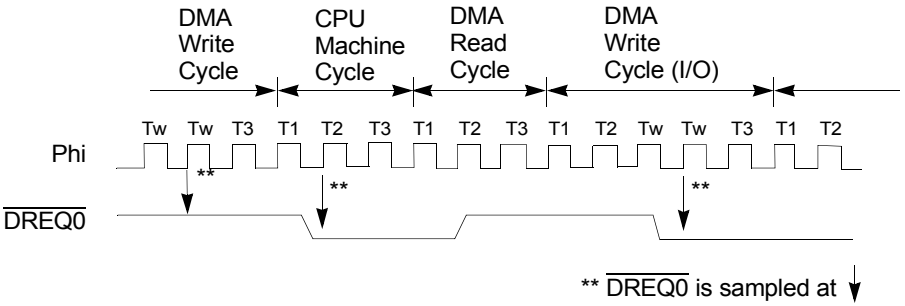


Figure 47. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Level-Sense

When edge-sense is programmed, DMA operation begins at the falling edge of $\overline{\text{DREQ0}}$ If another falling edge is detected before the rising edge of the clock prior to T3 during DMA write cycle (that is T2 or Tw), the DMAC continues operating. If an edge is not detected, the CPU is given control after the current byte DMA transfer completes. The CPU continues operating until a $\overline{\text{DREQ0}}$ falling edge is detected before the

0, data can be written into the ASCII Receive Data Register, and the data can be read.

ASCI Status Register 0, 1 (STAT0, 1)

Each channel status register allows interrogation of ASCI communication, error and modem control signal status, and enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: 04H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF	OVRN	PE	FE	RIE	$\overline{\text{DCD0}}$	TDRE	TIE
R/W	R	R	R	R	R/W	R	R	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF	R		**Receive Data Register Full** — RDRF is set to 1 when an incoming data byte is loaded into RDR. If a framing or parity error occurs, RDRF remains set and the receive data (which generated the error) is still loaded into RDR. RDRF is cleared to 0 by reading RDR, when the $\overline{\text{DCD0}}$ input is High, in IOSTOP mode, and during RESET.
6	OVRN	R		**Overrun Error** — OVRN is set to 1 when RDR is full and RSR becomes full. OVRN is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.

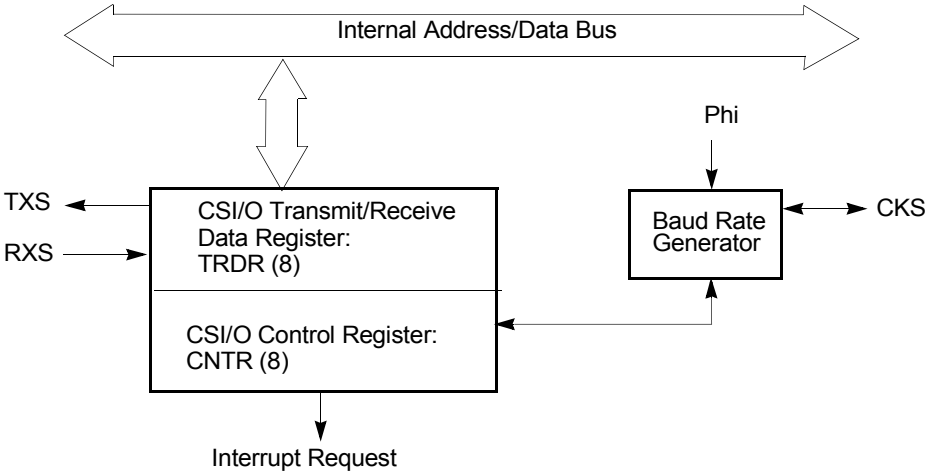


Figure 57. CSI/O Block Diagram

CSI/O Registers Description

CSI/O Control/Status Register (CNTR: I/O Address 0AH)

CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

CSI/O Control/Status Register (CNTR: 0AH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	EF	EIE	RE	TE	—	SS2	SS1	SS0
R/W	R	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	EF	R		**End Flag** — EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If EIE (End Interrupt Enable) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF is 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.
6	EIE	R/W		**End Interrupt Enable** — EIE is set to 1 to enable EF = 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.
5	RE	R/W		**Receive Enable** — A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external dock mode, the dock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and ISTOP mode. RXS is multiplexed with $\overline{\text{CTS1}}$ modem control input of ASCI channel 1. In order to enable the RXS function, the CTS1E bit in CNTA1 must be reset to 0.

Timing Diagrams

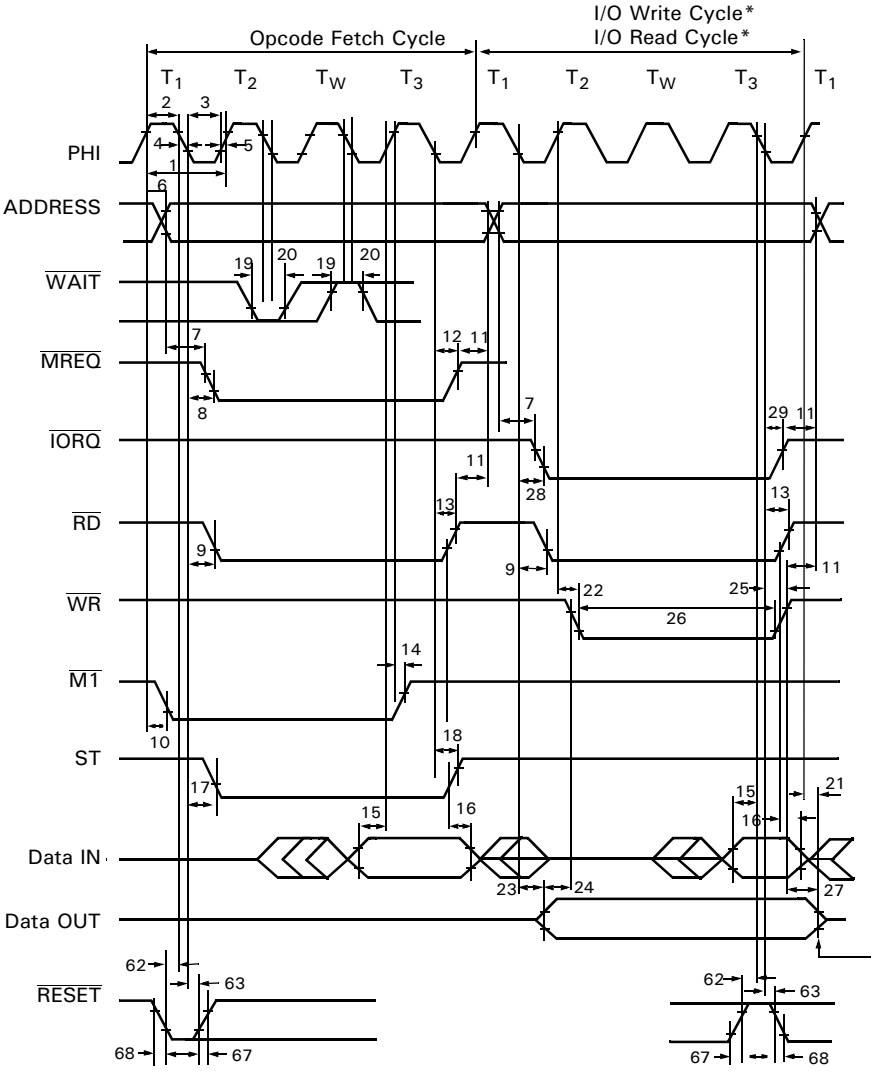


Figure 81. AC Timing Diagram 1

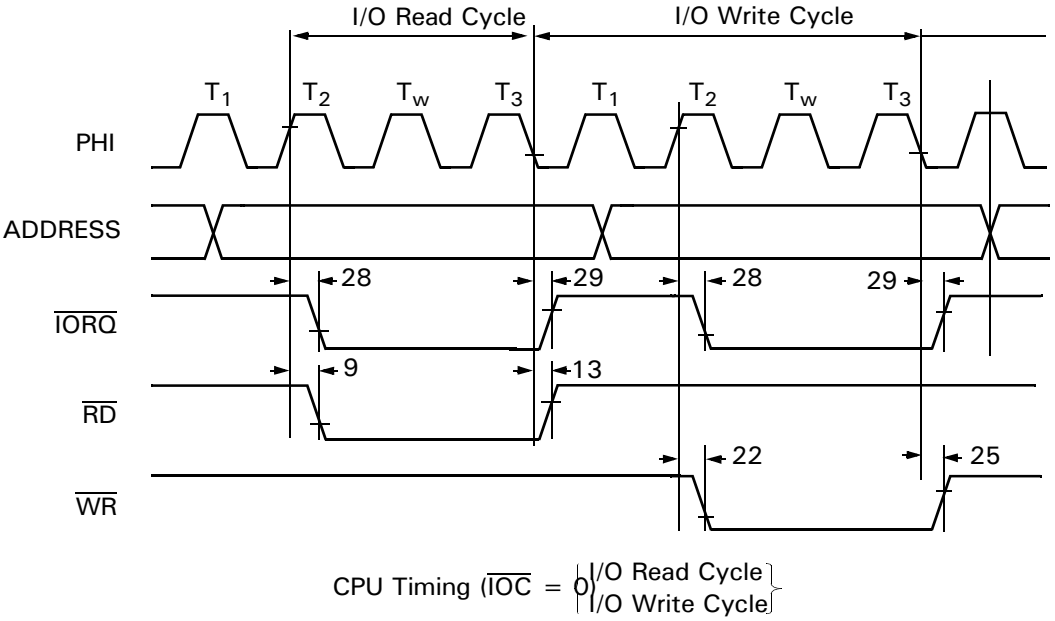


Figure 83. CPU Timing ($\overline{IOC}$ = 0) (I/O Read Cycle, I/O Write Cycle)

Table 33. Bit Values

b	Bit
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

CONDITION

f specifies the condition in program control instructions. Table 34 describes the correspondence between **f** and conditions.

Table 34. Instruction Values

f	Condition	
000	NZ	Nonzero
001	Z	Zero
010	NC	Non Carry
011	C	Carry
100	PO	Parity Odd
101	PE	Parity Even
110	P	Sign Plus
111	M	Sign Minus

DATA MANIPULATION INSTRUCTIONS

Table 38. Arithmetic and Logical Instructions (8-bit)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
ADD	ADD A,g	10 000 g				S		D		1	4	Ar + gr→Ar	↑	↑	↑	V	R	↑
	ADD A, (HL)	10 000 110					S	D		1	6	Ar + $(HL)_M$→Ar	↑	↑	↑	V	R	↑
	ADD A, m	11 000 110	S					D		2	6	Ar + m→Ar	↑	↑	↑	V	R	↑
		<m>																
	ADD A,(IX + d)	11 011 101			S			D		3	14	Ar + $(IX + d)_M$→Ar	↑	↑	↑	V	R	↑
		10 000 110																
		<d>																
	ADD A,(IY + d)	11 111 101			S			D		3	14	Ar + $(IY + d))_M$→Ar	↑	↑	↑	V	R	↑
		10 000 I10																
		<d>																
ADC	ADC A,g	10 001 g				S		D		1	4	Ar + gr + c→Ar	↑	↑	↑	V	R	↑
	ADC A,(HL)	10 001 110					S	D		1	6	Ar + $(HL)_M$ + c→Ar	↑	↑	↑	V	R	↑
	ADC A,m	11 001 110	S					D		2	6	Ar + m + c→Ar	↑	↑	↑	V	R	↑
		<m>																
	ADC A,(IX + d)	11 011 101			S			D		3	14	Ar + $(IX + d))_M$ + c→Ar	↑	↑	↑	V	R	↑
		10 001 110																
		<d>																
	ADC A,(IY + d)	11 111 101			S			D		3	14	Ar + $(IY + d))_M$ + c→Ar	↑	↑	↑	V	R	↑
		10 001 110																
		<d>																

Table 40. Arithmetic Instructions (16-bit)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
ADD	ADD HL,ww	00 ww1 001				S		D		1	7	$HL_R + ww_R \rightarrow HL_R$	•	•	X	•	R	↑
	ADD IX,xx	11 011 101 00 xx1 001				S		D		2	10	$IX_R + xx_R \rightarrow {}^*IX_R$	•	•	X	•	R	↑
	ADD IY,yy	11 111 101 00 yy1 001				S		D		2	10	$IY_R + yy_R \rightarrow IY_R$	•	•	X	•	R	↑
ADC	ADC HL,ww	11 101 101 01 ww1 010				S		D		2	10	$HL_R + ww_R + c \rightarrow HL_R$	↑	↑	X	V	R	↑
DEC	DEC ww	00 ww1 011				S/D				1	4	$ww_R - 1 \rightarrow \bullet ww_R$	•	•	•	•	•	•
	DEC IX	11 011 101 00 101 011						S/D		2	7	$1X_R - 1 \rightarrow IX_R$	•	•	•	•	•	•
	DEC IY	11 111 101 00 101 011						S/D		2	7	$1Y_R - 1 \rightarrow IY_R$	•	•	•	•	•	•
INC	INC ww	00 ww 0011				S/D				1	4	$ww_R + 1 \rightarrow ww_R$	•	•	•	•	•	•
	INC IX	11 011 101 00 100 011						S/D		2	7	$1X_R + 1 \rightarrow IX_R$	•	•	•	•	•	•
	INC IY	11 111 101 00 100 011						S/D		2	7	$1Y_R + 1 \rightarrow IY_R$	•	•	•	•	•	•
SBC	SBC HL ww	11 101 101 01 ww0 010				S		D		2	10	$HL_R - ww_R - c \rightarrow HL_R$	↑	↑	X	V	S	↑

Bus Control Signal Conditions

BUS AND CONTROL SIGNAL CONDITION IN EACH MACHINE CYCLE

* (ADDRESS) invalid

Z (DATA) high impedance.

** added new instructions to Z80

Table 51. Bus and Control Signal Condition in Each Machine Cycle

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
ADD HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC5	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADD IX,xx ADD IY,yy	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADC HL,ww SBC HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1

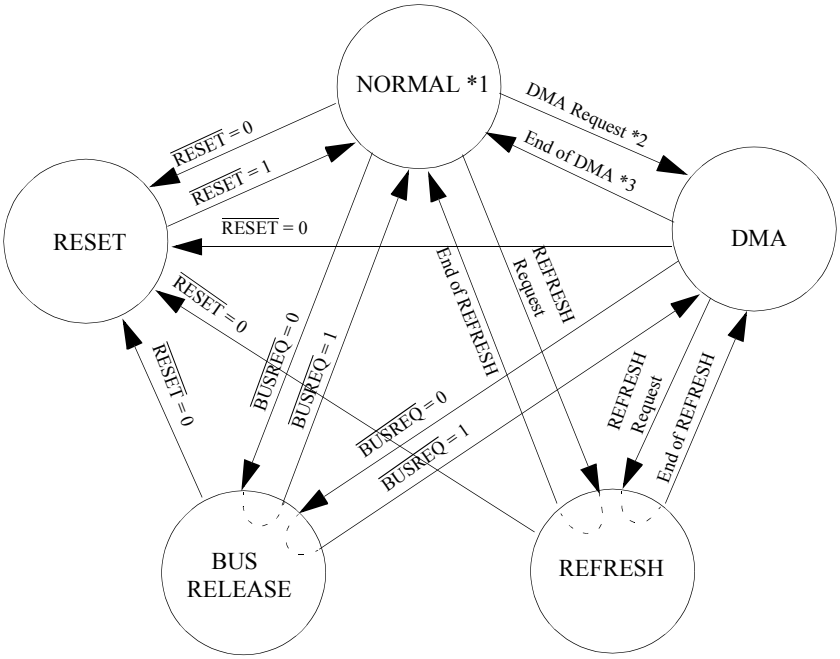


Figure 94. Operation Mode Transition

* 1. NORMAL: CPU executes instructions normally in NORMAL mode.

* 2. DMA request: DMA is requested in the following cases.
  - $\overline{DREQ0}$, $\overline{DREQ1}$ = 0
    memory to/from (memory mapped) I/0 DMA transfer
  - b. DEO = 1 (memory to/from memory DMA transfer)

* 3. DMA end: DMA ends in the following cases:

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Status Channel 0:	STAT0	0	4	

bit	RDRF	OVRN	PE	FE	RIE	$\overline{DCD0}$	TDRE	TIE
during RESET	0	0	0	0	invalid	*	**	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
Data Carrier Detect
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

** $\overline{CTS_0}$ Pin	TDRE
L	1
H	0

* $\overline{DCD_0}$: Depending on the condition of $\overline{DCD_0}$ Pin.

ASCI Status Channel 1:	STAT1	0	5

bit	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
during RESET	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
$\overline{CTS1}$ Enable
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.