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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008veg

List of Tables

Z80180, Z8S180, Z8L180 MPU Operation 1

Note: The user must program the Operation Mode Control Register before the first I/O instruction is executed.

CPU Timing

This section explains the Z8X180 CPU timing for the following operations:

- Instruction (Op Code) fetch timing
- Operand and data read/write timing
- I/O read/write timing
- Basic instruction (fetch and execute) timing
- RESET timing
- $\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ bus exchange timing

The basic CPU operation consists of one or more Machine Cycles (MC). A machine cycle consists of three system clocks, T1, T2, and T3 while accessing memory or I/O, or it consists of one system clock (T1) during CPU internal operations. The system clock is half the frequency of the Crystal oscillator (that is, an 8-MHz crystal produces 4 MHz or 250 nsec). For interfacing to slow memory or peripherals, optional Wait States (TW) may be inserted between T2 and T3.

Instruction (Op Code) Fetch Timing

Figure 9 illustrates the instruction (Op Code) fetch timing with no Wait States. An Op Code fetch cycle is externally indicated when the $\overline{\text{M1}}$ output pin is Low.

In the first half of T1, the address bus (A0–A19) is driven from the contents of the Program Counter (PC). This address bus is the translated address output of the Z8X180 on-chip MMU.

In the second half of T1, the $\overline{\text{MREQ}}$. (Memory Request) and $\overline{\text{RD}}$ (Read) signals are asserted Low, enabling the memory.

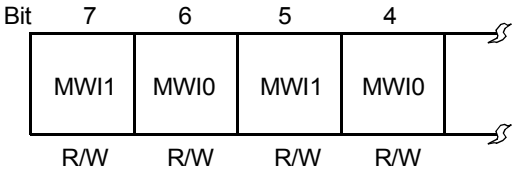

Figure 19. Memory and I/O Wait State Insertion (DCNTL – DMA/Wait Control Register)

The number of Wait States (TW) inserted in a specific cycle is the maximum of the number requested by the $\overline{\text{WAIT}}$ input, and the number automatically generated by the on-chip Wait State generator.

Bit 7, 6: MWI1 MWI0, (Memory Wait Insertion)

For CPU and DMAC cycles which access memory (including memory mapped I/O), zero to three Wait States may be automatically inserted depending on the programmed value in MWI1 and MWI0 as depicted in Table 3

Table 3. Memory Wait States

MW11	MWI0	The Number of Wait States
0	0	0
0	1	1
1	0	2
1	1	3

Bit 5, 4: IWI1, IWI0 (I/O Wait Insertion)

For CPU and DMA cycles which access external I/O (and interrupt acknowledge cycles), one to six Wait States (TW) may be automatically

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
Timer	Data Register Ch 0 L	TMDR0L	XX001100	0CH	159
	Data Register Ch 0 H	TMDR0H	XX001101	0DH	159
	Reload Register Ch 0 L	RLDR0L	XX001110	0EH	159
	Reload Register Ch 0 H	RLDR0H	XX001111	0FH	159
	Timer Control Register	TCR	XX010000	10H	161
	Reserved		XX010001	11H	
			↕	↕	
			XX010011	13H	
	Data Register Ch 1 L	TMDR1L	XX010100	14H	160
	Data Register Ch 1 H	TMDR1H	XX010101	15H	160
	Reload Register Ch 1 L	RLDR1L	XX010110	16H	159
	Reload Register Ch 1 H	RLDR1H	XX010111	17H	159
Others	Free Running Counter	FRC	XX011000	18H	172
	Reserved		XX011001	19H	
			↕	↕	
			XX011111	1FH	

DMA/WAIT Control Register (DCNTL: 32H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–6	MWI1–0	R/W		**Memory Wait Insertion** —Specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET. See section on Wait State Generator for details.
5–4	IWI1–0	R/W		**Wait Insertion** — Specifies the number of Wait States introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET. See section on Wait State Generator for details.
3–2	DMS1–0	R/W		**DMA Request Sense** — Specifies the DMA request sense for channel 0 ($\overline{\text{DREQ0}}$) and channel 1 ($\overline{\text{DREQ1}}$) respectively. When reset to 0, the input is level-sense. When set to 1, the input is edge-sense.
1–0	DIM1–0	R/W		**DMA Channel 1 I/O and Memory Mode** — Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. Reference Table 15.

DMAC Internal Interrupts

Figure 50 illustrates the internal DMA interrupt request generation circuit.

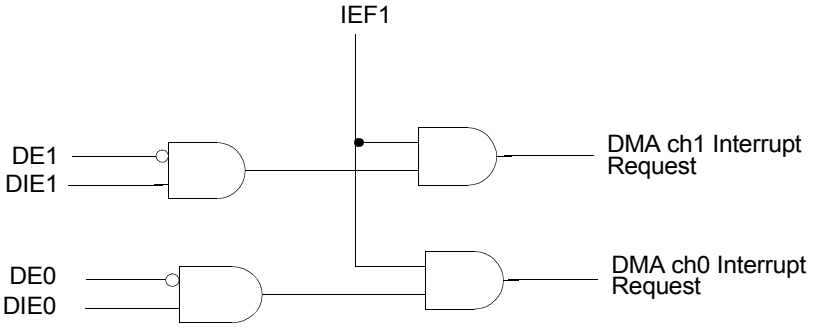

Figure 50. DMA Interrupt Request Generation

DE0 and DE1 are automatically cleared to 0 by the Z8X180 at the completion (byte count is 0) of a DMA operation for channel 0 and channel 1, respectively. They remain 0 until a 1 is written. Because DE0: and DE1 use level sense, an interrupt occurs if the CPU IEF1 flag is set to 1. Therefore, the DMA termination interrupt service routine disables further DMA interrupts (by programming the channel DIE bit is 0) before enabling CPU interrupts (for example, IEF1 is set to 1). After reloading the DMAC address and count registers, the DIE bit can be set to 1 to reenable the channel interrupt, and at the same time DMA can resume by programming the channel DE bit = 1.

DMAC and $\overline{\text{NMI}}$

$\overline{\text{NMI}}$, unlike all other interrupts, automatically disables DMAC operation by clearing the DME bit of DSTAT. Thus, the $\overline{\text{NMI}}$ interrupt service routine responds to time-critical events without delay due to DMAC bus usage. Also, $\overline{\text{NMI}}$ can be effectively used as an external DMA abort input, recognizing that both channels are suspended by the clearing of DME.

Bit Position	Bit/Field	R/W	Value	Description
2–0	MOD2–0	R/W		**ASCI Data Format Mode 2, 1, 0** — These bits program the ASCI data format as follows. **MOD2** 0: 7 bit data 1: 8 bit data **MOD1** 0: No parity 1: Parity enabled **MOD0** 0: 1 stop bit 1: 2 stop bits The data formats available based on all combinations of MOD2, MOD1 and MOD0 are described in Table 17.

a common baud rate of up to 512 Kbps to be selected. The BRG can also be disabled in favor of an external clock on the CKA pin.

The Receiver and Transmitter subsequently divide the output of the BRG (or the signal from the CKA pin) by 1, 16, or 64, under the control of the DR bit in the CNTLB register, and the X1 bit in the ASCI Extension Control REgister. To compute baud rate, use the following formulas:

Where:

BRG mode is bit 3 of the ASEXT register

PS is bit 5 of the CNTLB register

TC is the 16-bit value in the ASCI Time Constant register

If ss2.1.0 = 111, baud rate - f_{CKA}/Clock mode

else if BRG mode baud rate = f_{PHI}/(2*(TC+2)*Clock mode)

else baud rate -f_{PHI}/((10 + 20*PS) * 2^ss*Clock mode)

The TC value for a given baud rate is:

TC = (f_{PHI}/*2*baud rate*Clock mode)) -2

Clock mode depends on bit 4 in ASEXT and bit 3 in CNTLB, as described in Table 20.

Table 20. Clock Mode Bit Values

X1	DR	Clock Mode
0	0	16
0	1	64
1	0	1
1	1	Reserved, do not use

2^ss depends on the three least significant bits of the CNTLB register, as described in Table 21.

Table 21. 2^ss Values

ss2	ss1	ss0	2^ss
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	External Clock from CKA0

The ASCIs require a 50% duty cycle when CKA is used as an input. Minimum High and Low times on CKA0 are typical of most CMOS devices.

RDRF is set, and if enabled, an Rx Interrupt or DMA REquest is generated when the receiver transfers a character from the Rx Shift Register to the RX FIFO. The FIFO provides a margin against overruns. When the is more than one character in the FIFO, and software or a DMA channel reads a character, RDRF either remains set or is cleared and then immediately set again. For example, if a receive interrupt service routine does not real all the characters in the RxFIFO, RDRF and the interrupt request remain asserted.

The Rx DMA request is disabled when any of the error flags PE or FE or OVRN are set, so that software can identify with which character the problem is associated.

If Bit 7, RDRF Interrupt Inhibit, is set to 1, the ASCI does not request a Receive interrupt when its RDRF flag is 1. Set this bit when programming a DMA channel to handle the receive data from an ASCI. The other

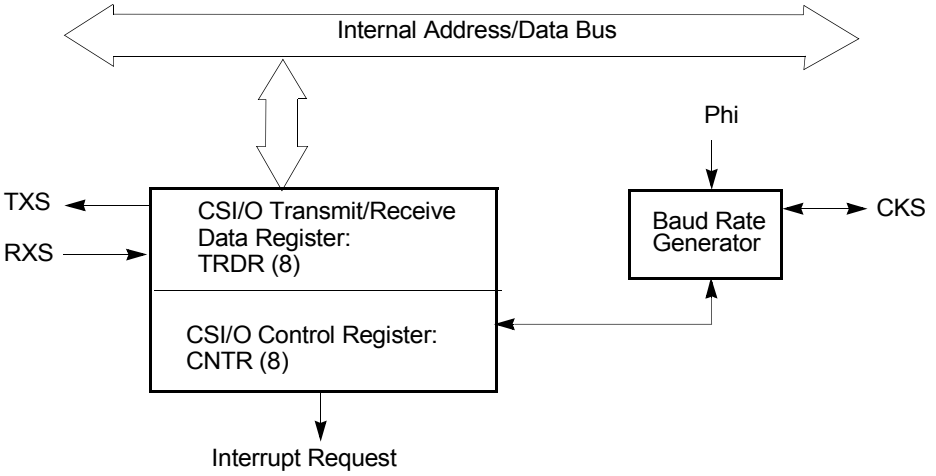

Figure 57. CSI/O Block Diagram

CSI/O Registers Description

CSI/O Control/Status Register (CNTR: I/O Address 0AH)

CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

CSI/O Control/Status Register (CNTR: 0AH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	EF	EIE	RE	TE	—	SS2	SS1	SS0
R/W	R	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

IO (I/O)

IO addressing mode is used only by I/O instructions. This mode specifies I/O address ($\overline{\text{IORQ}}$ is 0) and outputs them as follows.

1. An operand is output to A0–A7. The contents of accumulator is output to A8–A15.
2. The contents of Register B is output to A0–A7. The contents of Register C is output to A8–A15.
3. An operand is output to A0–A7. 00H is output to A8–A15 (useful for internal I/O register access)
4. The contents of Register C is output to A0–A7. 00H is output to A8–A15 (useful for internal I/O register access).

Table 30. Z8L180 DC Characteristics (Continued)

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
ICC	Power Dissipation* (Normal Operation)	f = 20 MHz		20	100	mA
	Power Dissipation* (SYSTEM STOP Mode)	f = 20 MHz		2	10	mA
	Power Dissipation* (IDLE Mode)	f = 20 MHz		3	10	mA
	Power Dissipation* (STANDBY Mode)	External Oscillator, Internal Clock Stops		4	10	µA
CP	Pin Capacitance	VIN = 0V, f = 1MHz TA = 25°C	–	–	12	pF
Notes: * VIN min = V_{CC} –1.0V. VIL max = 0.8V (All output terminals are a no load.) V_{CC} = 3.3V						

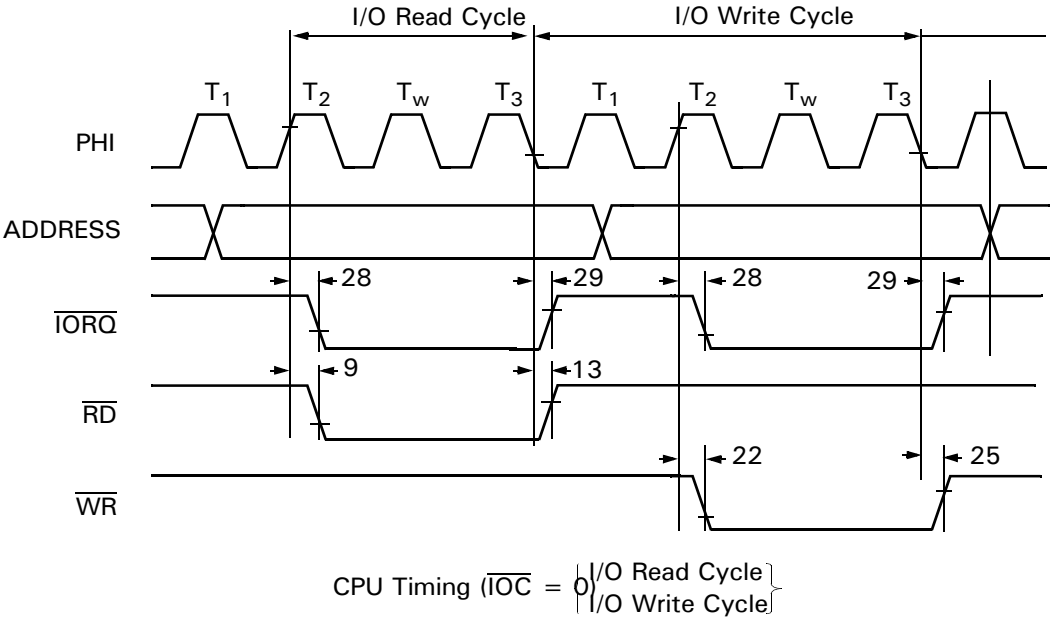

Figure 83. CPU Timing ($\overline{IOC}$ = 0) (I/O Read Cycle, I/O Write Cycle)

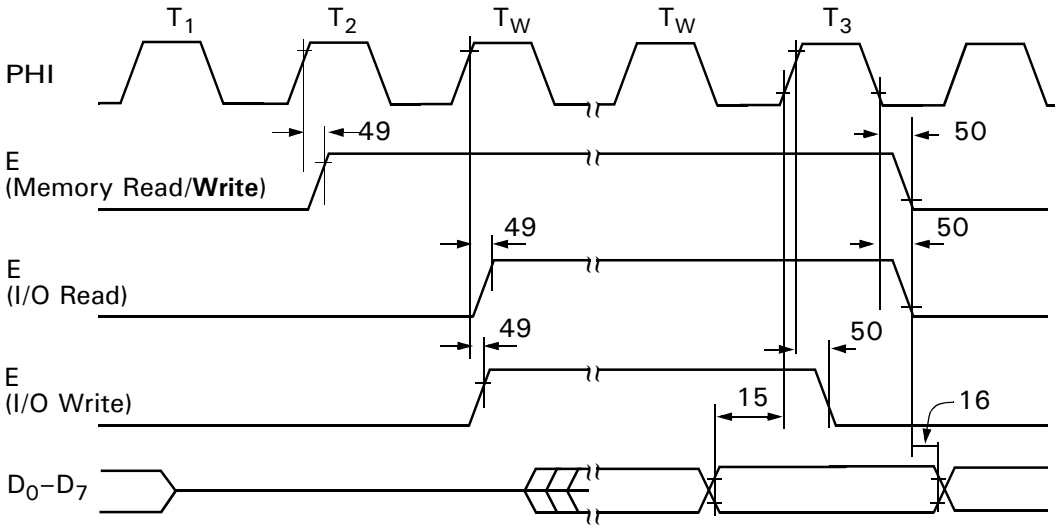

Figure 85. E Clock Timing (Memory R/W Cycle) (I/O R/W Cycle)

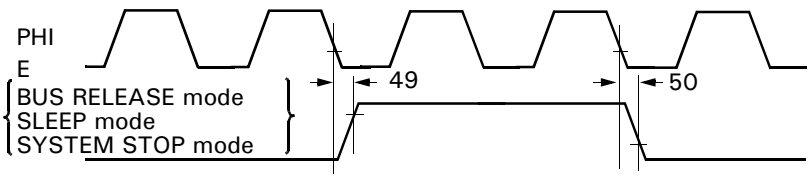

Figure 86. E Clock Timing (BUS RELEASE Mode, SLEEP Mode, and SYSTEM STOP Mode

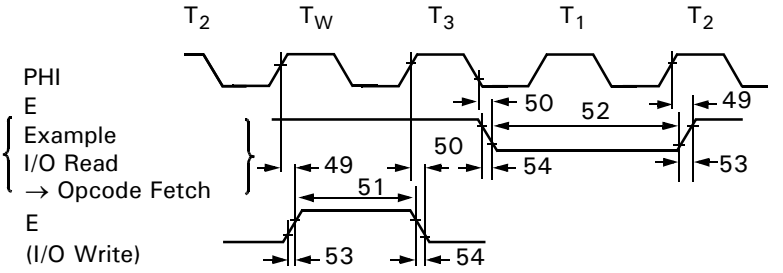

Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

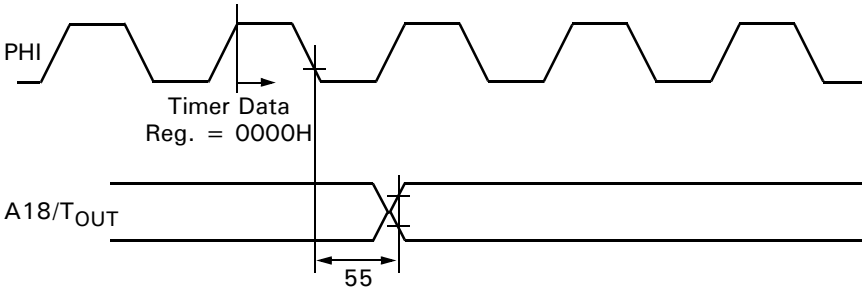

Figure 88. Timer Output Timing

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
													7	6	4	2	1	0
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				S	Z	H	P/V	N	C
SUBC	SBC A,g	10 011 g				S		D		1	4	Ar-gr-c→Ar	↑	↑	↑	V	S	↑
	SBC A,(HL)	10 011 110					S	D		1	6	Ar-$(HL)_M$-c→Ar	↑	↑	↑	V	S	↑
	SBC A,m	11 011 110	S					D		2	6	Ar-m-c→Ar	↑	↑	↑	V	S	↑
		<m>																
	SBC A,(IX + d)	11 011 101			S			D		3	14	Ar-$(IX + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 011 110																
		<d>																
	SBC A,(IY + d)	11 111 101			S			D		3	14	Ar-$(IY + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 011 110																
		<d>																
TEST	TST g**	11 101 101				S				2	7	Ar•gr	↑	↑	S	P	R	R
		00 g 100																
	TST {HL)**	11101101					S			2	10	Ar•$(HL)_M$	↑	↑	S	P	R	R
	00 110 100																	
	TST m**	11 101 101	S							3	9	Ar•m	↑	↑	S	P	R	R
		01 100 100																
		<m>																
XOR	XOR g	10 101 g				S		D		1	4	Ar⊕ + gr→Ar	↑	↑	R	P	R	R
	XOR (HL)	10 101 110					S	D		1	6	Ar⊕ + $(HL)_M$→Ar	↑	↑	R	P	R	R
	XOR m	11 101 110	S					D		2	6	Ar⊕ + m→Ar	↑	↑	R	P	R	R
		<m>																
	XOR (IX + d)	11 011 101			S			D		3	14	Ar⊕ + $(IX + d))_M$→Ar	↑	↑	R	P	R	R
		10 101 110																
		<d>																

Operating Modes Summary

REQUEST ACCEPTANCES IN EACH OPERATING MODE

Table 53. Request Acceptances in Each Operating Mode

Current Status / Request		Normal Operation (CPU mode and IOSTOP Mode)	WAIT State	Refresh Cycle	Interrupt Acknowledge Cycle	DMA Cycle	BUS RELEASE Mode	SLEEP Mode	SYSTEM STOP Mode
$\overline{WAIT}$		Acceptable	Acceptable	Not acceptable	Acceptable	Acceptable	Not acceptable	Not acceptable	Not acceptable
Refresh Request Request of Refresh by the on-chip Refresh Controller		Refresh cycle begins at the end of Machine Cycle (MC)	Not acceptable	Not acceptable	Refresh cycle begins at the end MC	Refresh cycle begins at the end of MC	Not acceptable	Not acceptable	Not acceptable
$\overline{DREQ0}$ $\overline{DREQ1}$		DMA cycle begins at the end of MC	DMA cycle begins at the end of MC	Acceptable Refresh cycle precedes. DMA cycle begins at the end of one MC	Acceptable DMA cycle begins at the end of MC.	Acceptable Refer to "DMA Controller" for details.	Acceptable *After BUS RELEASE cycle, DMA cycle begins at the end of one MC	Not acceptable	Not acceptable
$\overline{BUSREQ}$		Bus is released at the end of MC	Not acceptable	Not acceptable	Bus is released at the end of MC	Bus is released at the end of MC	Continue BUS RELEASE mode	Acceptable	Acceptable
Interrupt	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$	Accepted after executing the current instruction.	Accepted after executing the current instruction	Not acceptable	Not acceptable	Not acceptable	Not acceptable	Acceptable Return from SLEEP mode to normal operation.	Acceptable Return from SYSTEM STOP mode to normal operation

Status Signals

PIN OUTPUTS IN EACH OPERATING MODE

Table 55 describes pin outputs in each operating mode.

Table 55. Pin Outputs in Each Operating Mode

Mode		$\overline{M1}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{RD}$	$\overline{WR}$	$\overline{RFSH}$	$\overline{HALT}$	$\overline{BUSACK}$	ST	Address BUS	Data BUS
CPU Operation	Op Code Fetch (1st Op Code)	0	0	1	0	1	1	1	1	0	A	IN
	Op Code Fetch (except 1 st Op Code)	0	0	1	0	1	1	1	1	1	A	IN
	MemRead	1	0	1	0	1	1	1	1	1	A	IN
	Memory Write	1	0	1	1	0	1	1	1	1	A	OUT
	I/O Read	1	1	0	0	1	1	1	1	1	A	IN
	I/O Write	1	1	0	1	0	1	1	1	1	A	OUT
	Internal Operation	1	1	1	1	1	1	1	1	1	A	IN
Refresh		1	0	1	1	1	0	1	1	*	A	IN
Interrupt Acknowledge Cycle (1st Machine Cycle)	$\overline{NMI}$	0	0	1	0	1	1	1	1	0	A	IN
	$\overline{INT0}$	0	1	0	1	1	1	1	1	0	A	IN
	$\overline{INT1}$, $\overline{INT2}$ & Internal Interrupts	1	1	1	1	1	1	1	1	0	A	IN
BUS RELEASE		1	Z	Z	Z	Z	1	1	0	*	Z	IN
HALT		0	0	1	0	1	1	0	1	0	A	IN
SLEEP		1	1	1	1	1	1	0	1	1	1	IN

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
	CKA0 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{DREQ0}}$	Z	IN (N)	IN (A)	IN (N)
TXA1	—	1	OUT	H	H
RXA1	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA1/$\overline{\text{TEND0}}$	CKA1 (Internal Clock Mode)	Z	OUT	Z	Z
	CKA1 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{TEND0}}$	Z	1	OUT	1
TXS	—	1	OUT	H	H
RXS/$\overline{\text{CTS}}_1$	RXS	IN (N)	IN (A)	IN (N)	IN (N)
	$\overline{\text{CTS1}}$	IN (N)	IN (A)	IN (N)	IN (N)
CKS	CKS (Internal Clock Mode)	Z	OUT	1	1
	CKS (External Clock Mode)	Z	IN (A)	Z	Z
$\overline{\text{DREQ}}_1$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{\text{TEND}}_1$	—	1	1	OUT	1
$\overline{\text{HALT}}$	—	1	0	OUT	0
$\overline{\text{RFSH}}$	—	1	1	OUT	1
$\overline{\text{IORQ}}$	—	1	1	OUT	1