Zilog - Z8018008VSC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008vsc

TOUT. *Timer Out (Output, Active High).* TOUT is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. *Transmit Data 0 and 1 (Outputs, Active High).* These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. *Clocked Serial Transmit Data (Output, Active High).* This line is the transmitted data from the CSIO channel.

$\overline{\text{WAIT}}$. *Wait (Input; Active Low).* $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The $\overline{\text{WAIT}}$ input is sampled on the falling edge of T2 (and subsequent Wait States). If the input is sampled Low, then additional Wait States are inserted until the $\overline{\text{WAIT}}$ input is sampled High, at which time execution continues.

$\overline{\text{WR}}$. *Write (Output, Active Low, 3-state).* $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. *Crystal (Input, Active High). Crystal oscillator connection.* This pin must be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

Multiplexed pins are described in Table 2.

Refresh Control Register (RCR)

The RCR specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

Refresh Control Register (RCR: 36H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	REFE	REFW	?				CYC1	CYC0
R/W	R/W	R/W	?				R/W	R/W
Reset	1	1	?				0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	REFE	R/W		**REFE: Refresh Enable**
			0	Disables the refresh controller
			1	Enables refresh cycle insertion.
6	REFW	R/W		**Refresh Wait** (bit 6)
			0	Causes the refresh cycle to be two clocks in duration.
			1	Causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW).
1–0	CYC1–0	R/W		**Cycle Interval** — CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. In the case of dynamic RAMs requiring 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET. Refer to Table 11.

Table 11. DRAM Refresh Intervals

CYC1	CYC0	Insertion Interval	Time Interval				
			10 MHz	8 MHz	6 MHz	4 MHz	2.5 MHz
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.8 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

* Calculated interval

Refresh Control And RESET

After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of ten clock cycles and are three clock cycles in duration.

Dynamic Ram Refresh Operation Notes

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   - During RESET
   - When the bus is released in response to $\overline{\text{BUSREQ}}$
   - During SLEEP mode
   - During Wait States
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. Thus, the time at which the first refresh cycle occurs after the Z8X180 re-acquires the bus depends on the refresh timer and has no timing relationship with the bus exchange.

DMA Status Register (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also determines DMA transfer status, that is, completed or in progress.

DMA Status Register (DSTAT: 30H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	DE1	DE0	$\overline{\text{DWE1}}$	$\overline{\text{DWE0}}$	DIE1	DIE0	?	DME
R/W	R/W	R/W	W	W	R/W	R/W	?	R
Reset	0	0	1	1	0	0	?	

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	DE1	R/W		**Enable Channel 1** — When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU. To perform a software write to DE1, DWE1 is written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

Bit Position	Bit/Field	R/W	Value	Description
3–2	SM1:0	W		**Source Mode Channel** — Specifies whether the source for channel 0 transfers is memory, I/O, or memory mapped I/O and the corresponding address modifier. Reference Table 13.
1	MMOD	R/W		**DMA Memory Mode Channel 0** — When channel 0 is configured for memory to/from memory transfers, the external $\overline{\text{DREQ}}$0 input is not used to control the transfer timing. Instead, two automatic transfer timing modes are selectable - BURST (MMOD is 1) and CYCLE STEAL (MMOD is 0). For BURST memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as shown by the byte count register is 0). In CYCLE STEAL mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed. For channel 0 DMA with I/O source or destination, the $\overline{\text{DREQ}}$0 input times the transfer and thus MMOD is ignored.

Table 12. Channel 0 Destination

DM1	DM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Bit Position	Bit/Field	R/W	Value	Description
0	Send Break	R/W	0 1	Normal Xmit Drive TXA Low

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

ASCI1 Extension Control Register (I/O Address: 13H) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF Int Inhibit	Reserved		X1 Bit Clk ASCI1	BRG1 Mode	Break Feature Enable	Break Detect (RO)	Send Break
R/W	R/W	?		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF Interrupt Inhibit	R/W	0 1	RDRF Interrupt Inhibit On RDRF Interrupt Inhibit Off
6–5	Reserved	?	0	Reserved. Must be 0
4	X1 Bit Clk ASCI1	R/W	0 1	CKA1 /16 or /64 CKA1 is bit clock
3	BRG1 Mode	R/W	0 1	As S180 Enable 16-bit BRG counter

ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

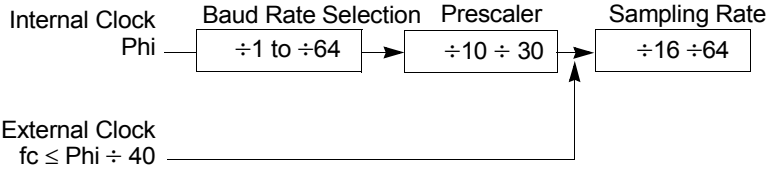

Figure 56. ASCI Clock

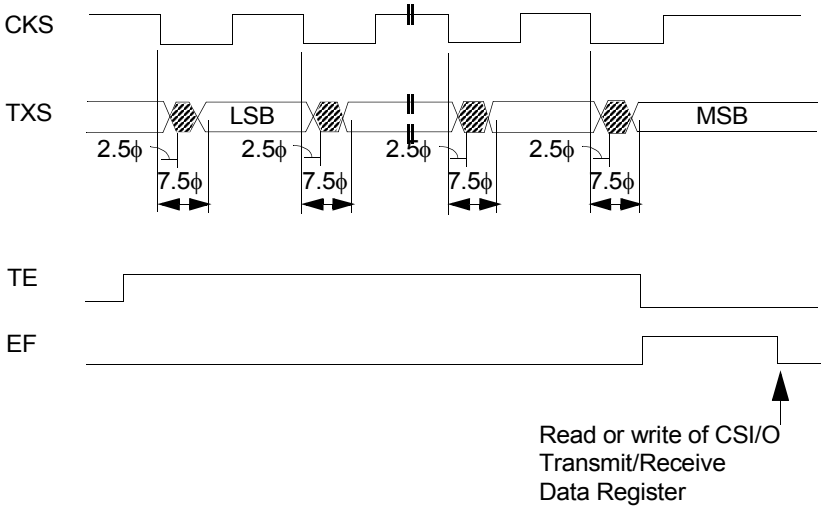

Figure 60. Transmit Timing–External Clock

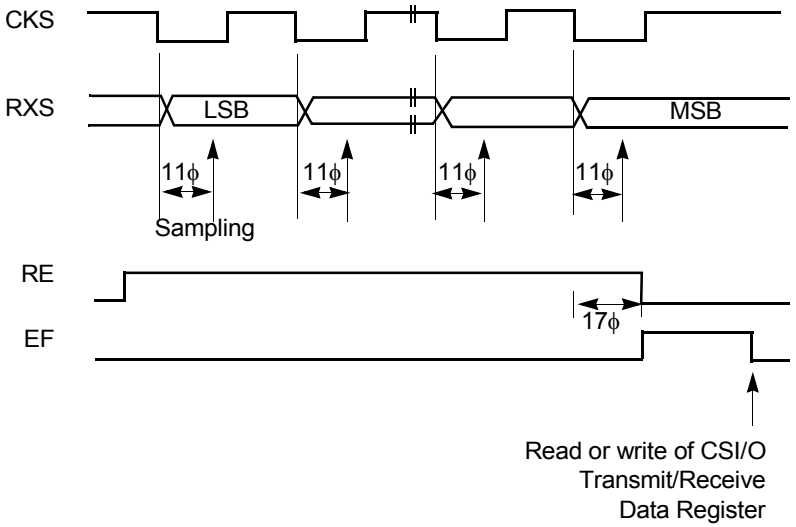

Figure 61. CSI/O Receive Timing–Internal Clock

Timer Reload Register Channel 1L (RLDR1L: 16H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Timer Reload Register Channel 1H (RLDR1H: 17H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Timer Control Register (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/TOUT for PRT1.

Timer Control Register (TCR: 10H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Stack Pointer (SP)

The Stack Pointer (SP) contains the memory address based LIFO stack. SP is cleared to 0000H during reset.

Program Counter (PC)

The Program Counter (PC) contains the address of the instruction to be executed and is automatically updated after each instruction fetch. PC is cleared to 0000H during reset.

Flag Register (F)

The Flag Register stores the logical state reflecting the results of instruction execution. The contents of the Flag Register are used to control program flow and instruction operation.

Flag Register

Bit	7	6	5	4	3	2	1	0
Bit/Field	S	Z	Not Used	H	Not Used	P/V	N	C
R/W	R/W	R/W	?	R/W	?	R/W	R/W	R/W
Reset	0	0	?	0	?	0	0	0

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	S	R/W	0	**Sign.** S stores the state of the most significant bit (bit 7) of the result. This is useful for operations with signed numbers in which values with bit 7 = 1 are interpreted as negative.

Memory Read/Write Cycle timing is the sam as I/O Read/Write Cycle except there are no automatica Wait States (TW), and MREQ is active instead of IORQ.

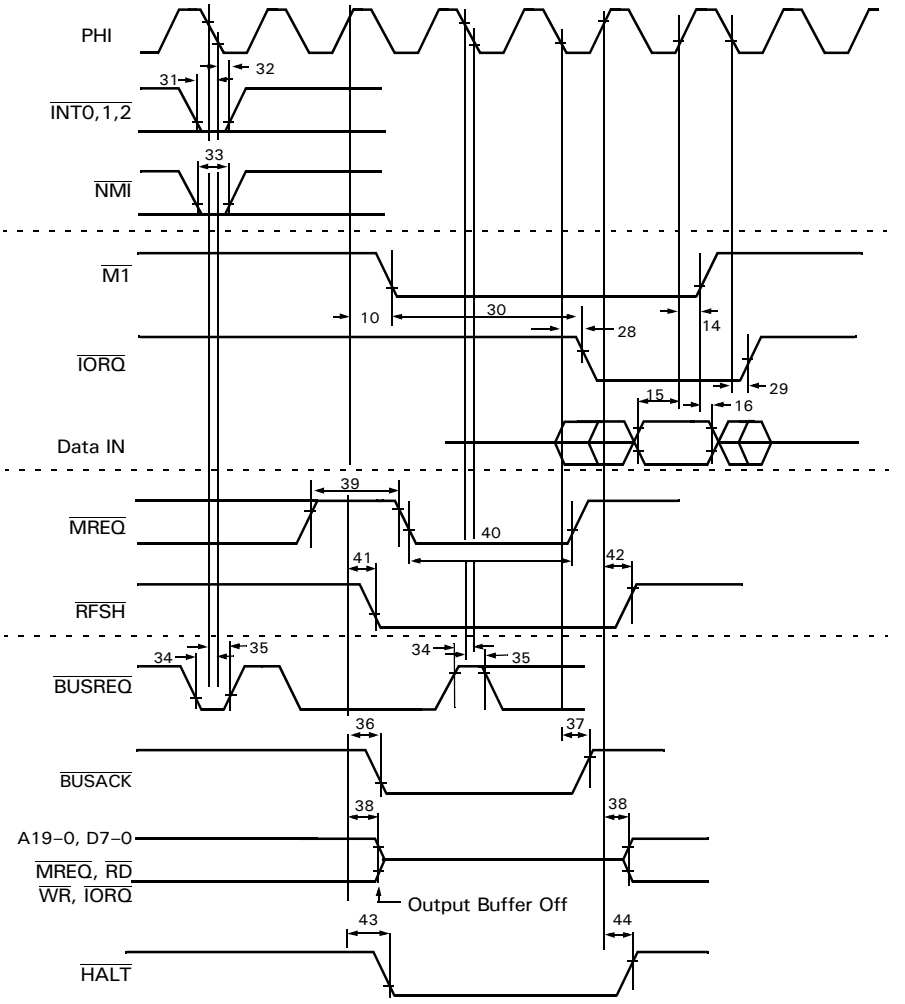

Figure 82. AC Timing Diagram 2

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
DEC	DEC g	00 g 101				S/D				1	4	gr-1→gr	↑	↑	↑	V	S	•
	DEC (HL)	00 110 101					S/D			1	10	$(HL)_M$-1→$(HL)_M$	↑	↑	↑	V	S	•
	DEC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$-I→	↑	↑	↑	V	S	•
		00 110 101										$(IX + d))_M$						
		<d>																
	DEC (IY + d)	11 111 101			S/D					3	18	$(IY + d)_M$-1→	↑	↑	↑	V	S	•
		00 1101 01										$(IY + d)_M$						
		<d>																
INC	INC g	00 g 100				S/D				1	4	gr + I→gr	↑	↑	↑	V	R	•
	INC (HL)	00 110 100					S/D			1	10	$(HL)_M$ + I→$(HL)_M$	↑	↑	↑	V	R	•
	INC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$ + 1→	↑	↑	↑	V	R	•
		00 110 100										$(1X + d))_M$						
		<d>																
	INC (IY + d)	11 111 101			S/D					3	18	(IY + d)v + 1→	↑	↑	↑	V	R	•
		00 110 100										(IY + d)v						
		<d>																
MULT	MLT ww**	11 101 101				S/D				2	17	wwHr→wwLr→wwI	•	•	•	•	•	•
		01 WWI 100																
NEGATE	NEG	11 101 101						S/D		2	6	0-Ar→Ar	↑	↑	↑	Y	S	↑
		01 000 100																

DATA TRANSFER INSTRUCTIONS

Table 41. 8-Bit Load

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Load 8-Bit Data	LD A,I	11 101 101 01 010 111						S/D		2	6	1r→Ar	↑	↑	R	IEF2	R	•
	LD A,R	11 101 101 01 011 111						S/D		2	6	Rr→Ar	↑	↑	R	IEF2	R	•
	LD A,(BC)	00 001 010					S	D		1	6	$(BC)_M$→Ar	•	•	•	•	•	•
	LD A,(DE)	00 011 010					S	D		1	6	$(DE)_M$→Ar	•	•	•	•	•	•
	LD A,(mn)	00 111 010 <n> <m>		S				D		3	12	$(mn)_M$→Ar	•	•	•	•	•	•
	LD L,A	11 101 101 01 000 111						S/D		2	6	Ar→Ir	•	•	•	•	•	•
	LD R,A	11 101 101 01 001 111						S/D		2	6	Ar→Rr	•	•	•	•	•	•
	LD (BC),A	00 000 010					D	S		1	7	Ar→$(BC)_M$	•	•	•	•	•	•
	LD(DE),A	00 010 010					D	S		1	7	Ar→$(DE)_M$	•	•	•	•	•	•
	LD (mn),A	00 110 010 <n> <m>		D				S		3	13	Ar→$(mn)_M$	•	•	•	•	•	•
	LD gg'	01 g g'				S/D				1	4	gr'→gr	•	•	•	•	•	•
	LD g,(HL)	01 g 110				D	S			1	6	$(HL)_M$→gr	•	•	•	•	•	•
	LD g,m	00 g 110 <m>	S			D				2	6	m→gr	•	•	•	•	•	•
	LD g,(IX + d)	11 011 101 01 g 110 <d>			S	D				3	14	$(IX + d)_M$gr	•	•	•	•	•	•
	LD g,(IY + d)	11 111 101 01 g 110 <d>			S	D				3	14	$(IY + d)_M$→gr	•	•	•	•	•	•
	LD (HL),m	00 110 110 <m>	S				D			2	9	m→$(HL)_M$	•	•	•	•	•	•

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
CPI CPD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4 ~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R \neq 0$ and $Ar = (HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC8	TiTiTi TiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R=0$ or $Ar=(HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
DAA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
DI*1	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
* 1 Interrupt request is not sampled.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
OUT (m),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	m to A0~A7 A to A8~A15	A	1	0	1	0	1	1	1
OUT (C),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	BC	g	1	0	1	0	1	1	1
OUT0 (m),g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	m to A0~A7 00H to A8~A15	g	1	0	1	0	1	1	1

INTERRUPTS

Table 52. Interrupts

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{NMI}$	MC1	T1T2T3	Next Op Code Address (PC)		0	1	0	1	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (RST Inserted)	MC1	T1T2TW TWT3	Next Op Code Address	1st(PC) Op Code	1	1	1	0	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (Call Inserted)	MC1	T1T2Tw TWT3	Next Op Code Address (PC)	1st Op Code	1	1	1	0	0	1	0
	MC2	T1T2T3	PC	n	0	1	0	1	1	1	1
	MC3	T1T2T3	PC+1	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PC+2(H)	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PC+2(L)	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 1	MC1	T1T2TW TWT3	Next Op Code Address (PC)		1	1	1	0	0	1	0
	MC2	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC3	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1

Note: If Bus Request and Refresh Request occur simultaneously, Bus Request is accepted but Refresh Request is cleared.

OPERATION MODE TRANSITION