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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	8MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018008vsc00tr

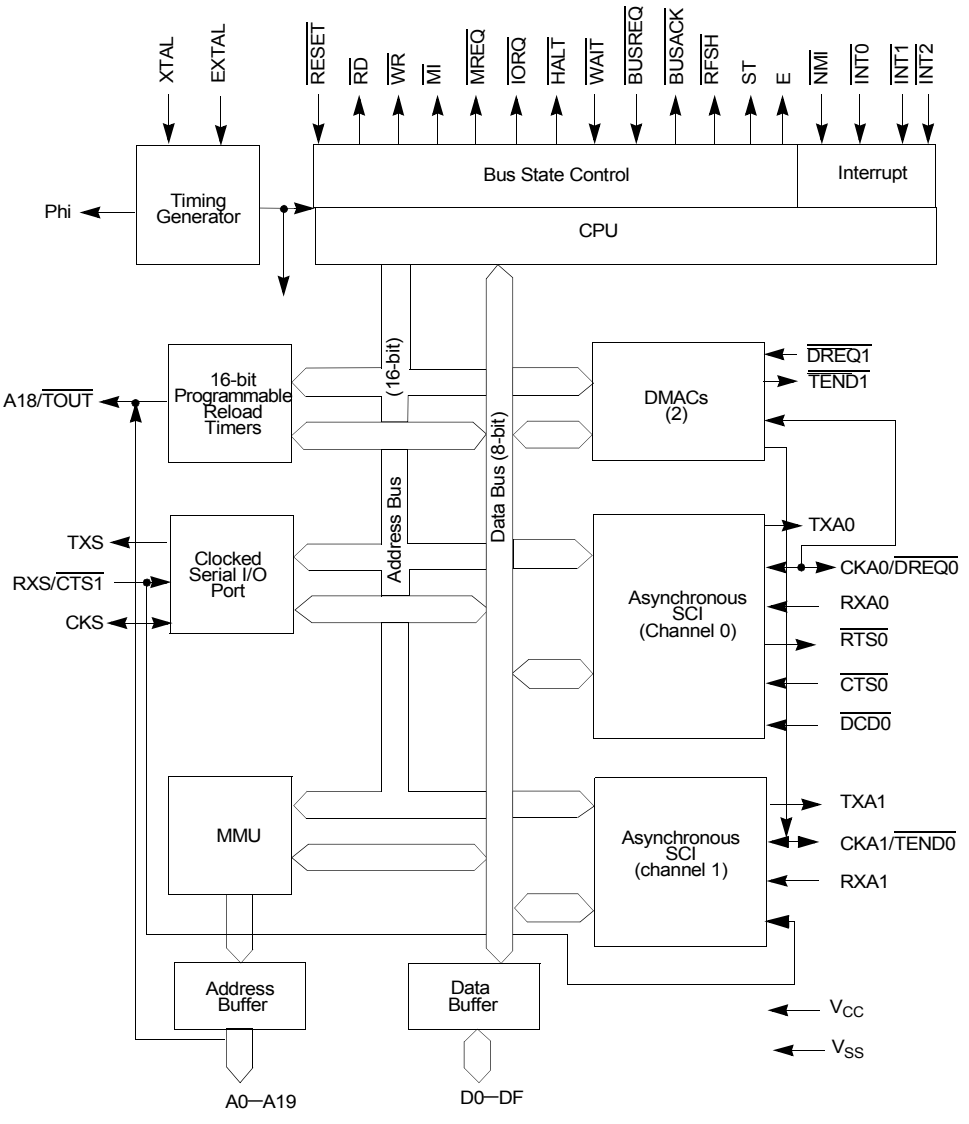


Figure 4. Z80180/Z8S180/Z8L180 Block Diagram

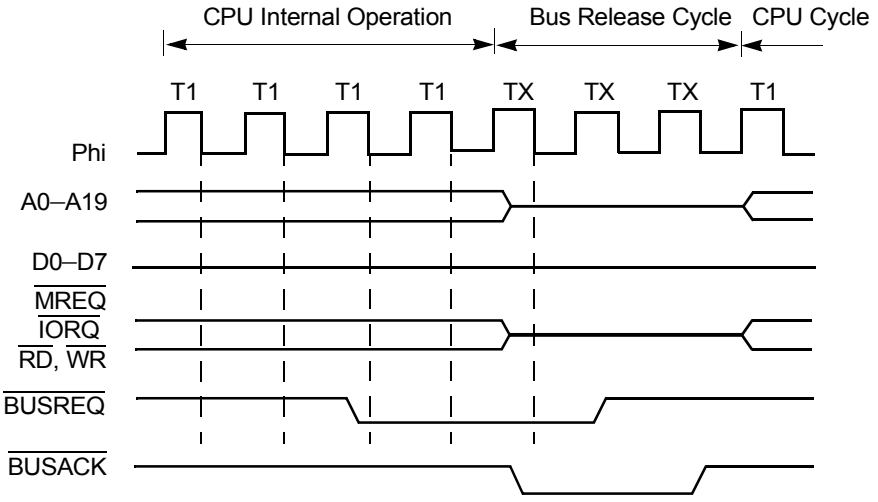


Figure 17. Bus Exchange Timing During CPU Internal Operation

Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

Note: $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

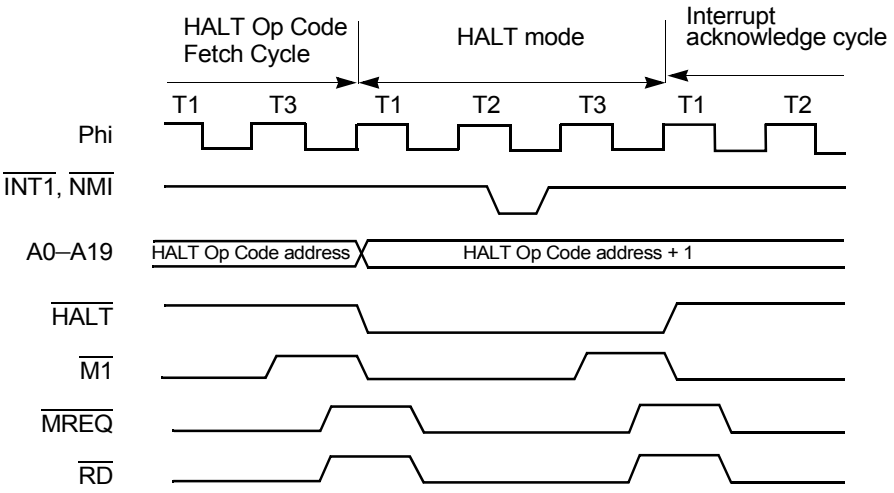


Figure 20. HALT Timing Diagram

SLEEP Mode

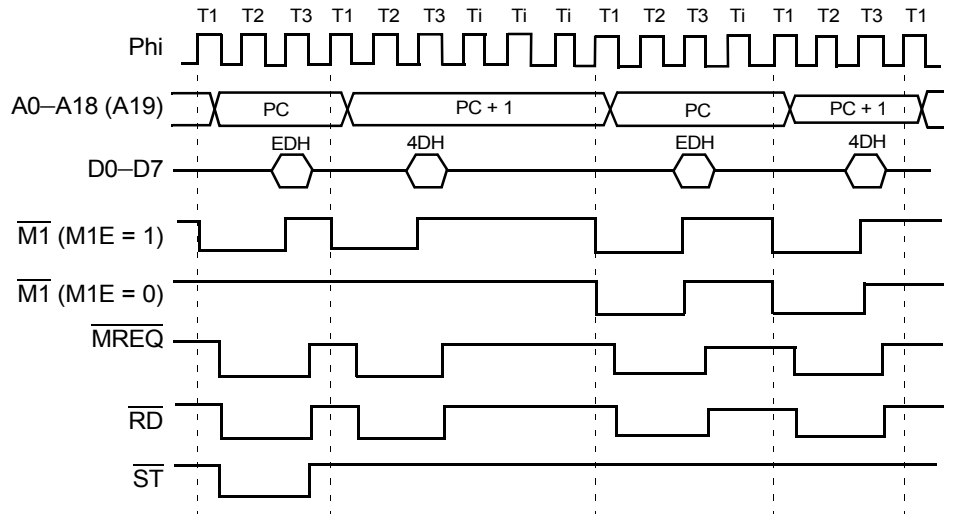
SLEEP mode is entered by execution of the 2-byte SLP instruction. SLEEP mode contains the following characteristics:

- The internal CPU clock stops, reducing power consumption
- The internal crystal oscillator does not stop
- Internal and external interrupt inputs can be received
- DRAM refresh cycles stop
- I/O operations using on-chip peripherals continue
- The internal DMAC stop
- $\overline{\text{BUSREQ}}$ can be received and acknowledged
- Address outputs go High and all other control signal outputs become inactive High

Return from Subroutine (RETI) Instruction Sequence

When the EDH/4DH sequence is fetched by the Z8X180, it is recognized as the RETI instruction sequence. The Z8X180 then refetches the RETI instruction with four T-states in the EDH cycle allowing the Z80 peripherals time to decode that cycle (See Figure 42). This procedure allows the internal interrupt structure of the peripheral to properly decode the instruction and behave accordingly.

The M1E bit of the Operation Mode Control Register (OMCR) must be set to 0 so that $\overline{M1}$ signal is active only during the refetch of the RETI instruction sequence. This condition is the desired operation when Z80 peripherals are connected to the Z8018X.



Note: RETI machine cycles 9 and 10 not shown.

Figure 42. RETI Instruction Sequence

The RETI instruction takes 22 T-states and 10 machine cycles. Table 10 lists the conditions of all the control signals during this sequence for the

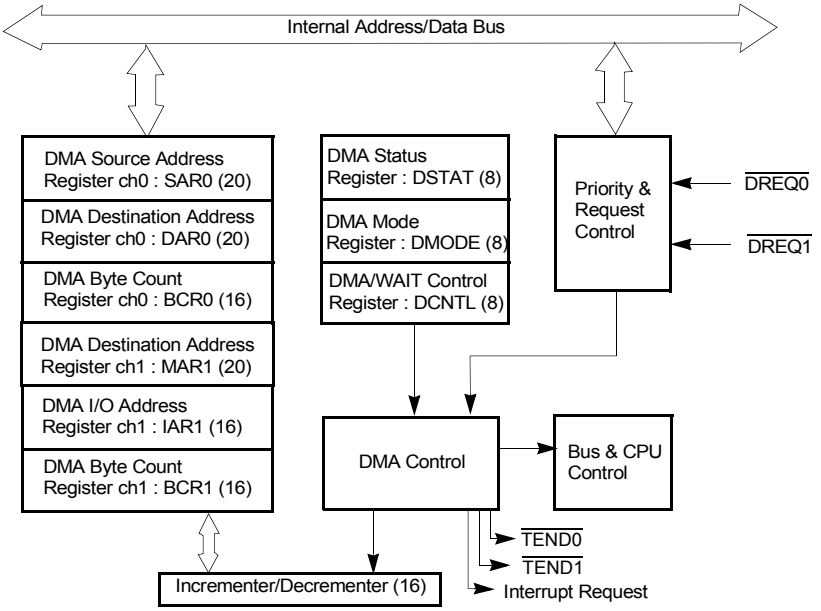


Figure 45. DMAC Block Diagram

DMAC Register Description

DMA Source Address Register Channel 0 (SAR0 I/O Address = 20H to 22H)

Specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O.

2^ss depends on the three least significant bits of the CNTLB register, as described in Table 21.

Table 21. 2^ss Values

ss2	ss1	ss0	2^ss
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	External Clock from CKA0

The ASCIs require a 50% duty cycle when CKA is used as an input. Minimum High and Low times on CKA0 are typical of most CMOS devices.

RDRF is set, and if enabled, an Rx Interrupt or DMA REquest is generated when the receiver transfers a character from the Rx Shift Register to the RX FIFO. The FIFO provides a margin against overruns. When the is more than one character in the FIFO, and software or a DMA channel reads a character, RDRF either remains set or is cleared and then immediately set again. For example, if a receive interrupt service routine does not real all the characters in the RxFIFO, RDRF and the interrupt request remain asserted.

The Rx DMA request is disabled when any of the error flags PE or FE or OVRN are set, so that software can identify with which character the problem is associated.

If Bit 7, RDRF Interrupt Inhibit, is set to 1, the ASCI does not request a Receive interrupt when its RDRF flag is 1. Set this bit when programming a DMA channel to handle the receive data from an ASCI. The other

control register. The PRT input clock for both channels is equal to the system clock divided by 20.

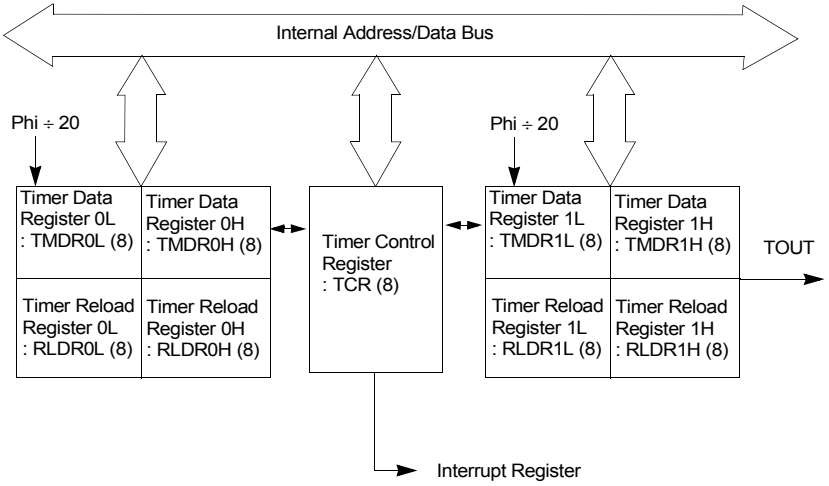


Figure 63. PRT Block Diagram

PRT Register Description

Timer Data Register (TMDR: I/O Address - CH0: 0CH, 0DH; CH1: 15H, 14H). PRT0 and PRT1 each contain 16-bit timer Data Registers (TMDR). TMDR0 and TMDR1 are each accessed as low and high byte registers (TMDR0H, TMDR0L and TMDR1H, TMDR1L). During RESET, TMDR0 and TMDR1 are set to FFFFH.

TMDR is decremented once every twenty clocks. When TMDR counts down to 0, it is automatically reloaded with the value contained in the Reload Register (RLDR).

TMDR is read and written by software using the following procedures. The read procedure uses a PRT internal temporary storage register to

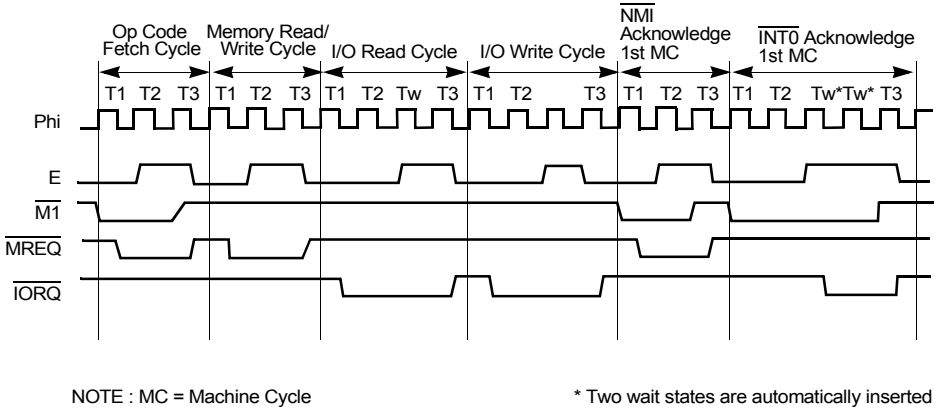


Figure 67. E Clock Timing Diagram (During Read/Write Cycle and Interrupt Acknowledge Cycle

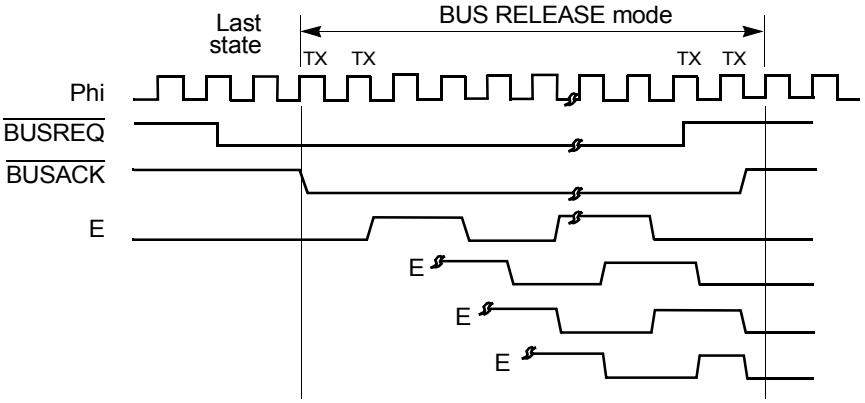


Figure 68. E Clock Timing in BUS RELEASE Mode

Memory Read/Write Cycle timing is the sam as I/O Read/Write Cycle except there are no automatica Wait States (TW), and MREQ is active instead of IORQ.

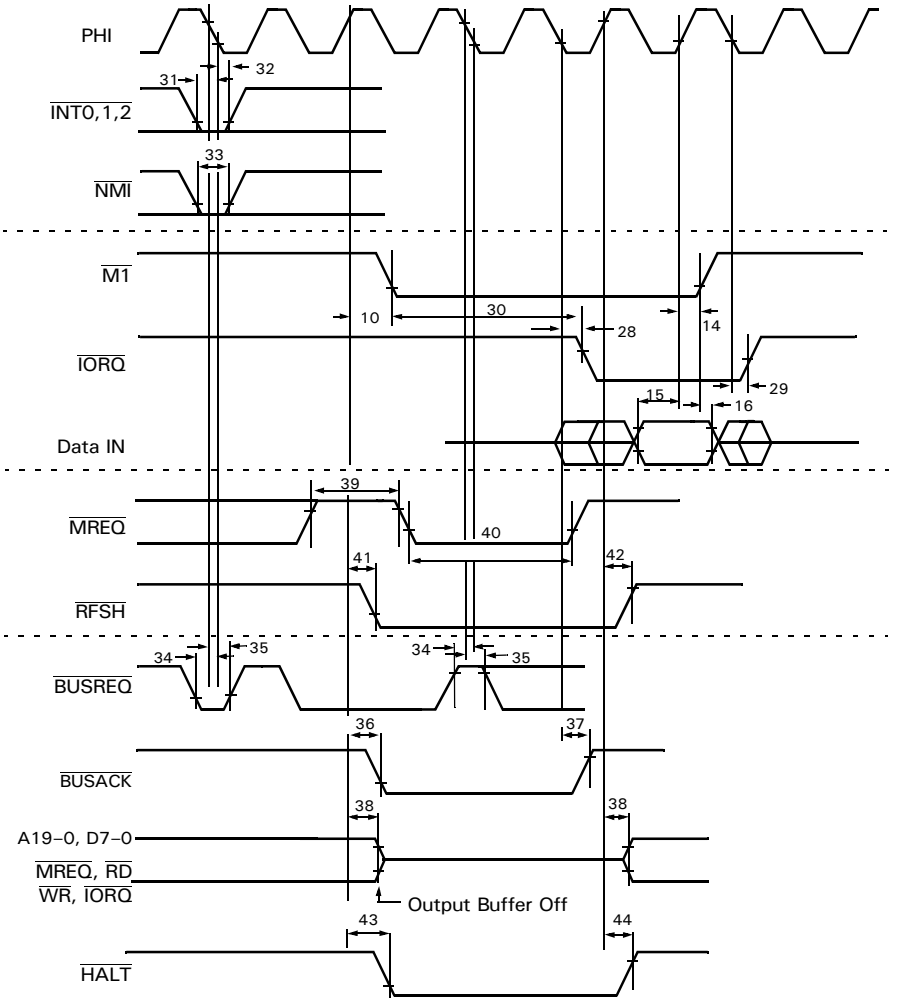


Figure 82. AC Timing Diagram 2

STANDARD TEST CONDITIONS

The previous DC Characteristics and Capacitance sections apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

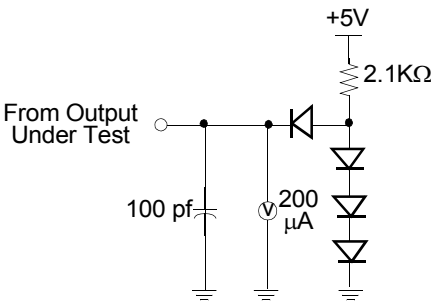


Figure 93. Test Setup

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
DEC	DEC g	00 g 101				S/D				1	4	gr-1→gr	↑	↑	↑	V	S	•
	DEC (HL)	00 110 101					S/D			1	10	$(HL)_M$-1→$(HL)_M$	↑	↑	↑	V	S	•
	DEC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$-I→	↑	↑	↑	V	S	•
		00 110 101										$(IX + d))_M$						
		<d>																
	DEC (IY + d)	11 111 101			S/D					3	18	$(IY + d)_M$-1→	↑	↑	↑	V	S	•
		00 1101 01										$(IY + d)_M$						
		<d>																
INC	INC g	00 g 100				S/D				1	4	gr + I→gr	↑	↑	↑	V	R	•
	INC (HL)	00 110 100					S/D			1	10	$(HL)_M$ + I→$(HL)_M$	↑	↑	↑	V	R	•
	INC (IX + d)	11 011 101			S/D					3	18	$(IX + d))_M$ + 1→	↑	↑	↑	V	R	•
		00 110 100										$(1X + d))_M$						
		<d>																
	INC (IY + d)	11 111 101			S/D					3	18	(IY + d)v + 1→	↑	↑	↑	V	R	•
		00 110 100										(IY + d)v						
		<d>																
MULT	MLT ww**	11 101 101				S/D				2	17	wwHr→wwLr→wwI	•	•	•	•	•	•
		01 WWI 100																
NEGATE	NEG	11 101 101						S/D		2	6	0-Ar→Ar	↑	↑	↑	Y	S	↑
		01 000 100																

Table 41. 8-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 8-Bit Data	LD (IX + d),m	11 011 101 00 110 110 <d>	S		D					4	15	$m \rightarrow (IX + d)_M$	•	•	•	•	•	•
	LD (IY + d),m	11 111 101 01 110 g <d> <m>	S		D					4	15	$m \rightarrow (IY + d)_M$	•	•	•	•	•	•
	LD (HL),g	01 110 g				S	D			1	7	$gr \rightarrow (HL)_M$	•	•	•	•	•	•
	LD (IX + d),g	11 011 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IX+d)_M$	•	•	•	•	•	•
	LD (IY + d),g	11 111 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IY + d)_M$	•	•	•	•	•	•
(1) In the case of R1 and Z Mask, interrupts are not sampled at the end of LD A, I or LD A,R.																		

Table 42. 16-Bit Load

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 16-Bit Data	LD ww,mn	00 ww0 001 <n> <m>	S			D				3	9	$mn \rightarrow ww_R$	•	•	•	•	•	•
	LD IX,mn	11 011 101 00 100 001 <n> <m>	S					D		4	12	$mn \rightarrow IX_R$	•	•	•	•	•	•

Table 42. 16-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Load 16-bit Data	LD (mn),HL	00 100 010 <n> <m>		D				S		3	16	Hr→(mn + 1)$_M$ Lr→(mn)$_M$	•	•	•	•	•	•
	LD (mn),IX	11 011 101 00 100 010 <n> <m>		D				S		4	19	IXHr-(mn + 1)$_M$ IXLr→(mn)$_M$	•	•	•	•	•	•
	LD (mn),IY	11 111 101 00 100 010 <n> <m>		D				S		4	19	IYHr→(mn + 1)$_M$ IYLr→(mn)$_M$	•	•	•	•	•	•

Table 43. Block Transfer

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Block Transfer Search Data	CPD	11 101 101 10 101 001					S	S		2	12	Ar = (HL)$_M$ BC$_R$-1→BC$_R$ HL$_R$-1→HL$_R$	↑	(3) ↑	↑	(2) ↑ (3)	S	•
	CPDR	11 101 101 10 111 001					S	S		2	14 12	BC$_R$ ≠ 0 Ar ≠ (HL)$_M$ BC$_R$ = 0 or Ar = (HL)$_M$ Q Ar-(HL)$_R$ BC$_R$-1-BC$_R$ HL$_R$-1→HL$_R$ Repeat Q until Ar = (HL)$_M$ or BC$_R$ = 0	↑	↑ (3)	↑	(2) ↑ (2)	S	•

Table 50. 2nd Op Code Map Instruction Format: ED XX

						ww (L0 = ALL)												
						BC	DE	HL	SP									
		G (L0 = 0~7)																
		B	D	H		B	D	H										
HI / LO		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	IN0 g, (m)				IN g, (C)						LDI	LDIR					0
0001	1	OUT0 (m),g				OUT (C),g						CPI	CPIR					1
0010	2					SBC HL, ww						INI	INIR					2
0011	3					LD (mn), ww				OTIM	OTIM R	OUTI	OTIR					3
0100	4	TST g			TST (HL)	NEG		TST m	TSTIO m									4
0101	5					RETN												5
0110	6					IM 0	IM 1		SLP									6
0111	7					LD I,A	LD A,I	RRD										7
1000	8	IN0 g, (m)				IN g, (C)						LDD	LDDR					8
1001	9	OUT0 (m), g				OUT (C) , g						CPD	CPDR					9
1010	A					ADC HL,ww						IND	INDR					A
1011	B					LD ww, (mn)				OTD M	OTD MR	OUTD	OTDR					B
1100	C	TST g				MLT ww												C
1101	D					RETI												D
1110	E						IM 2											E
1111	F					LDR, A	LD A,R	RLD										F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
		C	E	L	A	C	E	L	A									
		g (L0 = 8~F)																

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
INC (IX+ d) INC (IY+d) DEC (IX+d) DEC (IY+d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC5	TiTi	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	X+ d IY+ d	DATA	0	1	0	1	1	1	1
	MC7	T1	*	Z	1	1	1	1	1	1	1
	MC8	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
INC ww DEC ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	t	1	1	1	1
INC IX INC IY DEC IX DEC IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
IN A,(m)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	T1T2T3	m to A0~A7 A to A8~A15	DATA	0	1	1	0	1	1	1

Table 52. Interrupts (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{INT0}$ Mode 2	MC1	T1T2TW TWT3	Next Op Code Address (PC)	Vector	1	1	1	0	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1		1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3 T1T2,TW	I, Vector+1	DATA	0	1	0	1	1	1	1
$\overline{INT1}$ $\overline{INT2}$ Internal Interrupts	MC1	T1T2,TW TWT3	Next Op Code Address (PC)		1	1	1	1	1	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC4	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC5	T1T2T3	I, Vector	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	I, Vector+1	DATA	0	1	0	1	1	1	1

Note: If Bus Request and Refresh Request occur simultaneously, Bus Request is accepted but Refresh Request is cleared.

OPERATION MODE TRANSITION

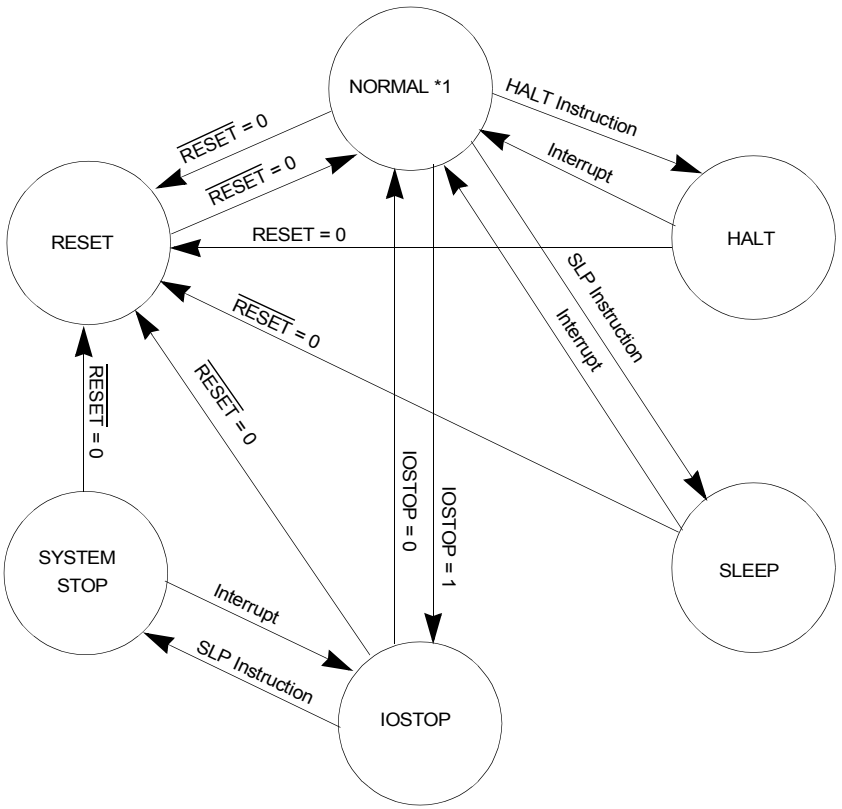


Table 55. Pin Outputs in Each Operating Mode (Continued)

Mode		$\overline{M1}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{RD}$	$\overline{WR}$	$\overline{RFSH}$	$\overline{HALT}$	$\overline{BUSACK}$	ST	Address BUS	Data BUS
Internal DMA	Memory Read	1	0	1	0	1	1	*	1	0	A	IN
	Memory Write	1	0	1	1	0	1	*	1	0	A	OUT
	I/O Read	1	1	0	0	1	1	*	1	0	A	IN
	I/O Write	1	1	0	1	0	1	*	1	0	A	OUT
RESET		1	1	1	1	1	1	1	1	1	Z	IN

- 1 : High
- 0 : Low
- A : Programmable
- Z : High Impedance
- IN : Input
- OUT : Output
- * : Invalid

PIN STATUS

Tables 56 describes the status of each ping during RESET and LOW POWER OPERATION modes.

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Control Register B Channel 0:	CNTLB0	0	2	

bit	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
during RESET	invalid	0	*	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Source and Speed Select
Divide Ratio
Parity Even or Odd
Clear to send/Prescale
Multi Processor
Multi Processor Bit Transmit

* $\overline{CTS}$: Depending on the condition 0f $\overline{CTS}$ Pin.
PS: Cleared to 0.

ASCI Control Register B Channel 1:	CNTLB1	0	3

bit	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
during RESET	invalid	0	0	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Source and Speed Select
Divide Ratio
Parity Even or Odd
Clear to Send/Prescale
Multi Processor
Multi Processor Bit Transmit

General divide ratio	PS=0 (divide ratio=10)		PS=1 (divide ratio=30)	
SS2 1 0	DR=0 (X 16)	DR=1 (X 64)	DR=0 (X 16)	DR=1 (X 64)
0 0 0	$\phi \div 160$	$\phi \div 640$	$\phi \div 480$	$\phi \div 1920$
0 0 1	$\div 320$	$\div 1280$	$\div 960$	$\div 3840$
0 1 0	$\div 640$	$\div 2560$	$\div 1920$	$\div 7680$
0 1 1	$\div 1280$	$\div 5120$	$\div 3840$	$\div 15360$
1 0 0	$\div 2560$	$\div 10240$	$\div 7680$	$\div 30720$
1 0 1	$\div 5120$	$\div 20480$	$\div 15360$	$\div 61440$
1 1 0	$\div 10240$	$\div 40960$	$\div 30720$	$\div 122880$
1 1 1	External clock (frequency $< \phi \div 40$)			

A

B

C