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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 8MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018008vsg |

# Table of Contents

$\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, during this cycle neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become Active.

**$\overline{\text{IORQ}}$.** *I/O Request (Output, Active Low, 3-state).* $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

**$\overline{\text{M1}}$.** *Machine Cycle 1 (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the Op Code fetch cycle of an instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

**$\overline{\text{MREQ}}$.** *Memory Request (Output, Active Low, 3-state).* $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the $\overline{\text{ME}}$ signal of the Z64180.

**$\overline{\text{NMI}}$.** *Non-maskable Interrupt (Input, negative edge triggered).* $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location `0066H`.

**$\overline{\text{RD}}$.** *Read (Output active Low, 3-state).* $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device must use this signal to gate data onto the CPU data bus.

**$\overline{\text{RFSH}}$.** *Refresh (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{RFSH}}$ indicates that the current CPU machine cycle and the contents of the address bus must be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7–A0) contain the refresh address.

This signal is analogous to the $\overline{\text{REF}}$ signal of the Z64180.

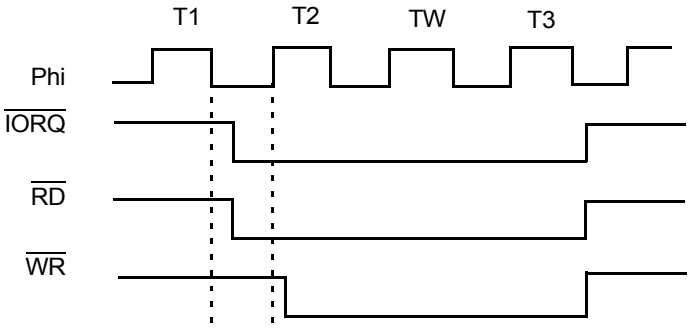



**Figure 7. I/O Read and Write Cycles with $\overline{IOC}$ = 1 Timing Diagram**

When $\overline{IOC}$ is 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing required by the Z80 family of peripherals. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. This timing allows the Z8X180 to satisfy the setup times required by the Z80 peripherals on those two signals (Figure ).

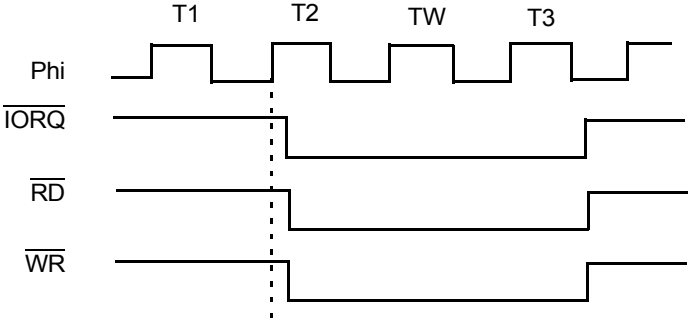



**Figure 8. I/O Read and Write cycles with IOC = 0 Timing Diagram**

For the remainder of this document, assume that M1E is 0 and $\overline{IOC}$ is 0.

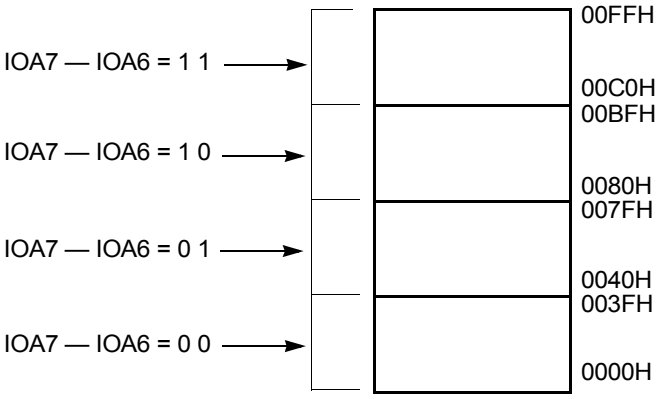



**Figure 22. I/O Address Relocation**

## Internal I/O Registers Address Map

The internal I/O register addresses are described in Table 6 and Table 7. These addresses are relative to the 64-byte boundary base address specified in ICR.

### I/O Addressing Notes

The internal I/O register addresses are located in the I/O address space from `0000H` to `00FFH` (16-bit I/O addresses). Thus, to access the internal I/O registers (using I/O instructions), the high-order 8 bits of the 16-bit I/O address must be `0`.

The conventional I/O instructions (OUT (m), A/IN A, (m) / OUTI/INI, for example) place the contents of a CPU register on the high-order 8 bits of the address bus, and thus may be difficult to use for accessing internal I/O registers.

For efficient internal I/O register access, a number of new instructions have been added, which force the high-order 8 bits of the 16-bit I/O

**Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)**

| | Register | Mnemonic | Address | | |
|---|---|---|---|---|---|
| | | | Binary | Hex | Page |
| DMA | DMA Source Address Register Ch 0L | SAR0L | XX100000 | 20H | 93 |
| | DMA Source Address Register Ch 0H | SAR0H | XX100001 | 21H | 93 |
| | DMA Source Address Register Ch 0B | SAR0B | XX100010 | 22H | 93 |
| | DMA Destination Address Register Ch 0L | DAR0L | XX100011 | 23H | 94 |
| | DMA Destination Address Register Ch 0H | DAR0H | XX100100 | 24H | 94 |
| | DMA Destination Address Register Ch 0B | DAR0B | XX100101 | 25H | 94 |
| | DMA Byte Count Register Ch 0L | BCR0L | XX100110 | 26H | 94 |
| | DMA Byte Count Register Ch 0H | BCR0H | XX100111 | 27H | 94 |
| | DMA Memory Address Register Ch 1L | MAR1L | XX101000 | 28H | 94 |
| | DMA Memory Address Register Ch 1H | MAR1H | XX101001 | 29H | 94 |
| | DMA Memory Address Register Ch 1B | MAR1B | XX101010 | 2AH | 94 |
| | DMA I/O Address Register Ch 1L | IAR1L | XX101011 | 2BH | 102 |
| | DMA I/O Address Register Ch 1H | IAR1H | XX101100 | 2CH | 102 |
| | DMA I/O Address Register Ch 1 | IAR1B | XX101101 | 2DH | 94 |
| | DMA Byte Count Register Ch 1L | BCR1L | XX101110 | 2EH | 94 |
| | DMA Byte Count Register Ch 1H | BCR1H | XX101111 | 2FH | 94 |
| | DMA Status Register | DSTAT | XX110000 | 30H | 95 |
| | DMA Mode Register | DMODE | XX110001 | 31H | 97 |
| | DMA/WAIT Control Register | DCNTL | XX110010 | 32H | 101 |

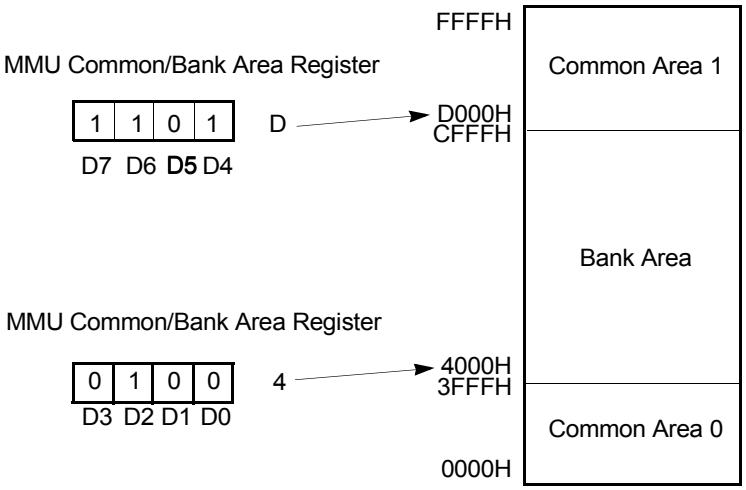



**Figure 28. Logical Space Configuration (Example)**

Refresh cycles may be programmed to be either two or three clock cycles in duration by programming the REFW (Refresh Wait) bit in the Refresh Control Register (RCR). The external $\overline{\text{WAIT}}$ input and the internal Wait State generator are not effective during refresh.

Figure 44 depicts the timing of a refresh cycle with a refresh wait (TRW) cycle.

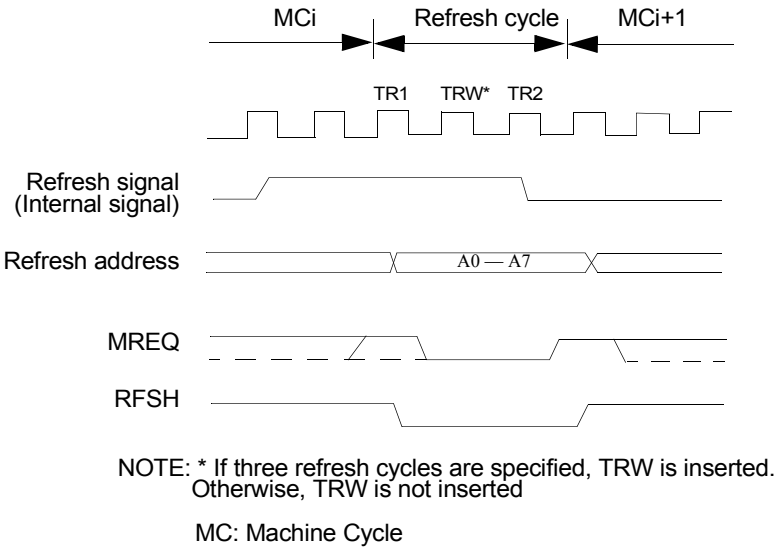



**Figure 44. Refresh Cycle Timing Diagram**

**Table 14. Transfer Mode Combinations**

| DM1 | DM0 | SM1 | SM0 | Transfer Mode | Increment/Decrement |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | Memory to I/O | SAR0+1, DAR0 fixed |
| 1 | 1 | 0 | 1 | Memory to I/O | SAR0-1, DAR0 fixed |
| 1 | 1 | 1 | 0 | Reserved | |
| 1 | 1 | 1 | 1 | Reserved | |
| Note: *: includes memory mapped I/O. | | | | | |

## DMA/WAIT Control Register (DCNTL)

DCNTL controls the insertion of Wait States into DMAC (and CPU) accesses of memory or I/O Also, the DMA request mode for each DREQ $\overline{\text{DREQ}}$0 and $\overline{\text{DREQ}}$1) input is defined as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

| Bit Position | Bit/Field | R/W | Value | Description |
|---|---|---|---|---|
| 5 | $\overline{\text{CTS}}$/PS | R/W | | **Clear to Send/Prescale** — When read, $\overline{\text{CTS}}$/PS reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}$/PS is read as 1. When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0). For channel 1, the $\overline{\text{CTS1}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}$/PS is only valid when read if the channel 1 CTS1E bit is 1 and the CST1 input pin function is selected. The read data of $\overline{\text{CTS}}$/PS is not affected by RESET.<br>When written, CT /PS specifies the baud rate generator prescale factor. If $\overline{\text{CTS}}$/PS is set to 1, the system clock is prescaled by 30 while if $\overline{\text{CTS}}$/PS is cleared to 0, the system clock is prescaled by 10.CTS/PS is cleared to 0 during RESET. |
| 4 | PEO | R/W | | **Parity Even Odd** — PE0 selects even or odd parity. PE0 does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PE0 is cleared to 0, even parity is selected. If PE0 is set to 1, odd parity is selected.PE0 is cleared to 0 during RESET. |
| 3 | DR | R/W | | **Divide Ratio** — DR specifies the divider used to obtain baud rate from the data sampling clock If DR is reset to 0, divide by 16 is used, while if DR is set to 1, divide by 64 is used. DR is cleared to 0 during RESET. |
| 2–0 | SS2–0 | R/W | | **Source/Speed Select** — Specifies the data clock source (internal or external) and baud rate prescale factor. SS2, SS1, and SS0 are all set to 1 during RESET. Table 18 describes the divide ratio corresponding to SS2, SS1 and SS0 |

The external ASCI channel 0 data clock pins are multiplexed with DMA control lines (CKA0/$\overline{\text{DREQ}}$ and CKA1/$\overline{\text{TEND0}}$). During RESET, these

### ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

### ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

### ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

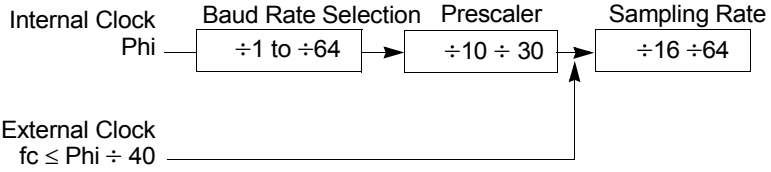



**Figure 56. ASCI Clock**

Timer Reload Register Channel 0L (RLDR0L: 0EH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit/Field | Timer Reload Data | | | | | | | |
| R/W | R/W | | | | | | | |
| Reset | 0 | | | | | | | |
| Note: R = Read W = Write X = Indeterminate ? = Not Applicable | | | | | | | | |

Timer Reload Register Channel 0H (RLDR0L: 0FH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit/Field | Timer Reload Data | | | | | | | |
| R/W | R/W | | | | | | | |
| Reset | 0 | | | | | | | |
| Note: R = Read W = Write X = Indeterminate ? = Not Applicable | | | | | | | | |

Timer Data Register 1L (TMDR1L: 14H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit/Field | Timer Data | | | | | | | |
| R/W | R/W | | | | | | | |
| Reset | 0 | | | | | | | |
| Note: R = Read W = Write X = Indeterminate ? = Not Applicable | | | | | | | | |

Timer Data Register 1H (TMDR1H: 15H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit/Field | Timer Data | | | | | | | |
| R/W | R/W | | | | | | | |
| Reset | 0 | | | | | | | |
| Note: R = Read W = Write X = Indeterminate ? = Not Applicable | | | | | | | | |

These devices require connection with the Z8X180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z8X180 clock rate. Table 24, and Figure 67 through Figure 70 define E clock output timing.

Wait States are inserted in Op Code fetch, memory read/write, and I/O read/write cycles which extend the duration of E clock output High. During I/O read/write cycles with no Wait States (only occurs during on-chip I/O register accesses), E does not go High.

**Table 24. E Clock Timing in Each Condition**

| **Condition** | **Duration of E Clock Output High** | |
|---|---|---|
| Op Code Fetch Cycle<br>Memory Read/Write Cycle | T2 rise - T3 fall | (1.5 Phi + nw x Phi) |
| I/O read Cycle | 1st Tw rise - T3 fall | (0.5Phi + nw x Phi) |
| I/O Write Cycle | 1st Tw rise - T3 rise | $In_w$ x Phi) |
| $\overline{NMI}$ Acknowledge 1st MC | T2 rise - T3 fall | (1.5 Phi) |
| $\overline{INT0}$ Acknowledge 1st MC | 1st Tw rise - T3 fall | (0.50 + nw x Phi) |
| BUS RELEASE mode<br>SLEEP mode<br>SYSTEM STOP mode | Phi fall - Phi fall | (2 Phi or 1 Phi) |
| Note: nw = the number of Wait States; MC: Machine Cycle | | |

### MLT- Multiply

The MLT performs unsigned multiplication on two 8-bit numbers yielding a 16-bit result. MLT may specify BC, DE, HL, or SP registers. The 8-bit operands are loaded into each half of the 16-bit register and the 16-bit result is returned in that register.

### OTIM, OTIMR, OTDM, OTDMR - Block I/O

The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR, respectively. The B register is decremented. The OTIMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as Z80180 on-chip I/O) initialization. When I/O is accessed, 00H is output in high-order bits of address automatically.

### TSTIO m - Test I/O Port

The contents of the I/O port addressed by C are ANDed with immediately specified 8-bit data and the status flags are updated. The I/O port contents are not written (non-destructive AND). When I/O is accessed, `00H` is output in higher bits of address automatically.

### TST g - Test Register

Perform an `AND` instruction on the contents of the specified register with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive `AND`).

### TST m - Test Immediate

Perform an `AND` instruction on the contents of the immediately specified 8-bit data with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive `AND`).

# DATA MANIPULATION INSTRUCTIONS

**Table 38. Arithmetic and Logical Instructions (8-bit)**

| Operation Name | Mnemonics | Op Code | Addressing | | | | | | | Bytes | States | Operation | Flags | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Immed | Ext | Ind | Reg | Regl | Imp | Rel | | | | 7 | 6 | 4 | 2 | 1 | 0 |
| | | | | | | | | | | | | | S | Z | H | P/V | N | C |
| ADD | ADD A,g | 10 000 g | | | | S | | D | | 1 | 4 | Ar + gr→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADD A, (HL) | 10 000 110 | | | | | S | D | | 1 | 6 | Ar + $(HL)_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADD A, m | 11 000 110 | S | | | | | D | | 2 | 6 | Ar + m→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | <m> | | | | | | | | | | | | | | | | |
| | ADD A,(IX + d) | 11 011 101 | | | S | | | D | | 3 | 14 | Ar + $(IX + d)_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 000 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| | ADD A,(IY + d) | 11 111 101 | | | S | | | D | | 3 | 14 | Ar + $(IY + d))_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 000 I10 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| ADC | ADC A,g | 10 001 g | | | | S | | D | | 1 | 4 | Ar + gr + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADC A,(HL) | 10 001 110 | | | | | S | D | | 1 | 6 | Ar + $(HL)_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADC A,m | 11 001 110 | S | | | | | D | | 2 | 6 | Ar + m + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | <m> | | | | | | | | | | | | | | | | |
| | ADC A,(IX + d) | 11 011 101 | | | S | | | D | | 3 | 14 | Ar + $(IX + d))_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 001 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| | ADC A,(IY + d) | 11 111 101 | | | S | | | D | | 3 | 14 | Ar + $(IY + d))_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 001 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |

# Special Control Instructions

**Table 47. Special Control Instructions**

| Operation Name | Mnemonics | Op Code | Addressing | | | | | | | Bytes | States | Operation | Flags | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Immed | Ext | Ind | Reg | Regi | Imp | Rel | | | | 7 | 6 | 4 | 2 | 1 | 0 |
| | | | | | | | | | | | | | S | Z | H | P/V | N | C |
| Special Function | DAA | 00 100 111 | | | | | | S/D | | 1 | 4 | Decimal Adjust Accumulator | ↑ | ↑ | ↑ | P | • | ↑ |
| Carry Control | CCF | 00 111 111 | | | | | | | | 1 | 3 | $\overline{C}$→C | • | • | R | • | R | ↑ |
| | SCF | 00 110 111 | | | | | | | | 1 | 3 | 1→C | • | • | R | • | R | S |
| CPU Control | DI | 11 110 011 | | | | | | | | 1 | 3 | 0→IEF1,0→IEF2 (7) | • | • | • | • | • | • |
| | EI | 11 111 011 | | | | | | | | 1 | 3 | 1→IEF1,1→IEF2 (7) | • | • | • | • | • | • |
| | HALT | 01 110 110 | | | | | | | | 1 | 3 | CPU halted | • | • | • | • | • | • |
| | IM0 | 11 101 101 | | | | | | | | 2 | 6 | Interrupt | • | • | • | • | • | • |
| | | 01 000 110 | | | | | | | | | | Mode 0 | | | | | | |
| | IM1 | 11 101 101 | | | | | | | | 2 | 6 | Interrupt | • | • | • | • | • | • |
| | | 01 010 110 | | | | | | | | | | Mode 1 | | | | | | |
| | IM2 | 11 101 101 | | | | | | | | 2 | 6 | Interrupt | • | • | • | • | • | • |
| | | 01 011 110 | | | | | | | | | | Mode 2 | | | | | | |
| | NOP | 00 000 000 | | | | | | | | 1 | 3 | No operation | • | • | • | • | • | • |
| | SLP** | 11 101 101 | | | | | | | | 2 | 8 | Sleep | • | • | • | • | • | • |
| | | 01 110 110 | | | | | | | | | | | | | | | | |

7) Interrupts are not sampled at the end of DI or EI.

# *Bus Control Signal Conditions*

## BUS AND CONTROL SIGNAL CONDITION IN EACH MACHINE CYCLE

* (ADDRESS) invalid

Z (DATA) high impedance.

** added new instructions to Z80

**Table 51. Bus and Control Signal Condition in Each Machine Cycle**

| Instruction | Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADD HL,ww | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 ~MC5 | TiTiTiTi | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ADD IX,xx ADD IY,yy | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 ~MC6 | TiTiTiTi | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ADC HL,ww SBC HL,ww | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 ~MC6 | TiTiTiTi | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

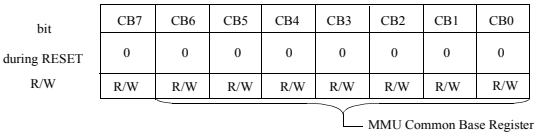
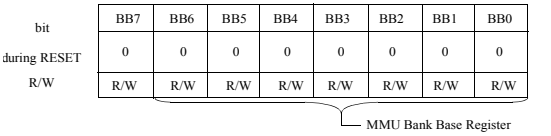
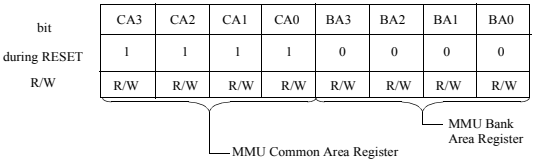
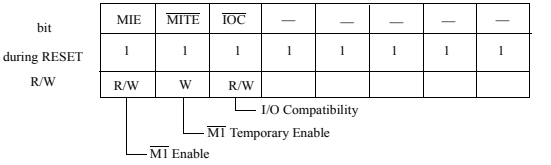
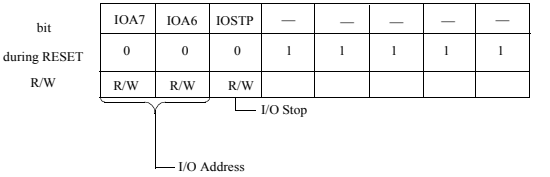
**Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)**

| Instruction | Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TST g** | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 | Ti | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TST m** | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 | T1T2T3 | 1st operand Address | m | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| TST (HL)** | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 2 | 0 | 2 | 0 | 2 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 | Ti | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | MC4 | T1T23 | HL | Data | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)**

| Symbol | Pin Function | Pin Status in Each Operation Mode | | | |
|---|---|---|---|---|---|
| | | RESET | SLEEP | IOSTOP | SYSTEM STOP |
| | CKA0 (External Clock Mode) | Z | IN (A) | IN (N) | IN (N) |
| | $\overline{\text{DREQ0}}$ | Z | IN (N) | IN (A) | IN (N) |
| TXA1 | — | 1 | OUT | H | H |
| RXA1 | — | IN (N) | IN (A) | IN (N) | IN (N) |
| CKA1/$\overline{\text{TEND0}}$ | CKA1 (Internal Clock Mode) | Z | OUT | Z | Z |
| | CKA1 (External Clock Mode) | Z | IN (A) | IN (N) | IN (N) |
| | $\overline{\text{TEND0}}$ | Z | 1 | OUT | 1 |
| TXS | — | 1 | OUT | H | H |
| RXS/$\overline{\text{CTS}}_1$ | RXS | IN (N) | IN (A) | IN (N) | IN (N) |
| | $\overline{\text{CTS1}}$ | IN (N) | IN (A) | IN (N) | IN (N) |
| CKS | CKS (Internal Clock Mode) | Z | OUT | 1 | 1 |
| | CKS (External Clock Mode) | Z | IN (A) | Z | Z |
| $\overline{\text{DREQ}}_1$ | — | IN (N) | IN (N) | IN (A) | IN (N) |
| $\overline{\text{TEND}}_1$ | — | 1 | 1 | OUT | 1 |
| $\overline{\text{HALT}}$ | — | 1 | 0 | OUT | 0 |
| $\overline{\text{RFSH}}$ | — | 1 | 1 | OUT | 1 |
| $\overline{\text{IORQ}}$ | — | 1 | 1 | OUT | 1 |

**Table 57. Internal I/O Registers (Continued)**

| Register | Mnemonics | Address | | Remarks |
|---|---|---|---|---|
| MMU Common Base Register: | CBR | 3 | 8 |  |
| MMU Bank Base Register | BBR | 3 | 9 |  |
| MMU Common/Bank Register | CBAR | 3 | A |  |
| Operation Mode Control Register | OMCR | 3 | E |  |
| I/O Control Register: | ICR | 3 | F |  |