Zilog - Z8018010FEC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010fec

Sections

Z8018X MPU Operation

Presents features, a general description, pins descriptions, block diagrams, registers, and details of operating modes for the Z8018x MPUs.

Software Architecture

Provides instruction sets and CPU registers for the Z8018x MPUs.

DC Characteristics

Presents the DC parameters and absolute maximum ratings for the Z8X180 MPUs.

AC Characteristics

Presents the AC parameters for the Z8018x MPUs.

Timing Diagrams

Contains timing diagrams and standard test conditions for the Z8018x MPUs.

Appendices

The appendixes in this manual provide additional information applicable to the Z8018x family of ZiLOG MPUs:

- Instruction set
- Instruction summary table
- Op Code map
- Bus Control signal conditions in each machine cycle and interrupt conditions
- Operating mode summary
- Status signals
- I/O registers and ordering information

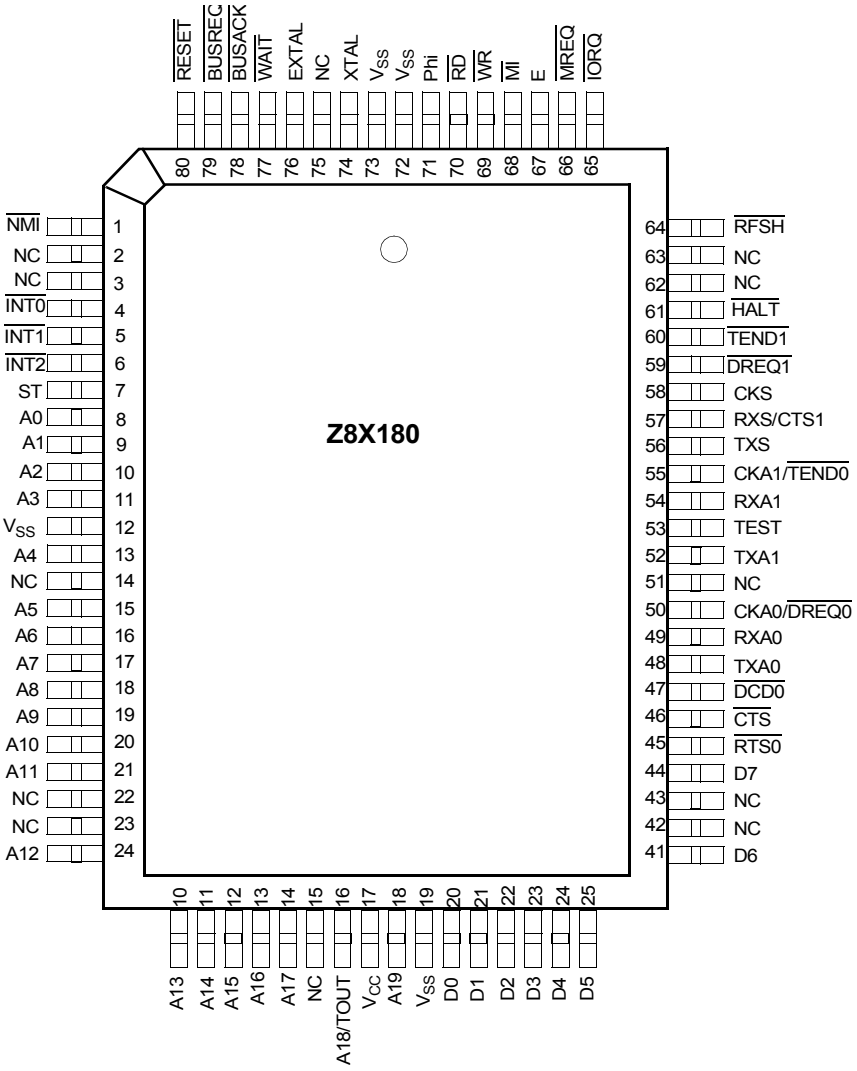


Figure 3. 80-Pin QFP

- Programmable Reload Timers (PRT, 2 channels)
- Clock Serial I/O (CSIO) channel.

Other Z8X180 family members (such as Z80183, Z80S183, Z80185/195) feature, in addition to these blocks, additional peripherals and are covered in their associated Product Specification

Clock Generator

This logic generates the system clock from either an external crystal or clock input. The external clock is divided by two and provided to both internal and external devices.

Bus State Controller

This logic performs all of the status and bus control activity associated with both the CPU and some on-chip peripherals. This includes Wait State timing, RESET cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller

This block monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To remain compatible with the Z80 CPU, three different interrupt modes are supported.

Memory Management Unit

The MMU allows the user to map the memory used by the CPU (logically only 64K) into the 1MB addressing range supported by the Z8X180. The organization of the MMU object code features compatibility with the Z80 CPU while offering access to an extended memory space. This capability is accomplished by using an effective *common area - banked area* scheme.

Wait States (TW) are inserted as previously described for Op Code fetch cycles. Figure 11 illustrates the read/write timing without Wait States (Tw), while Figure 12 illustrates read/write timing with Wait States (TW).

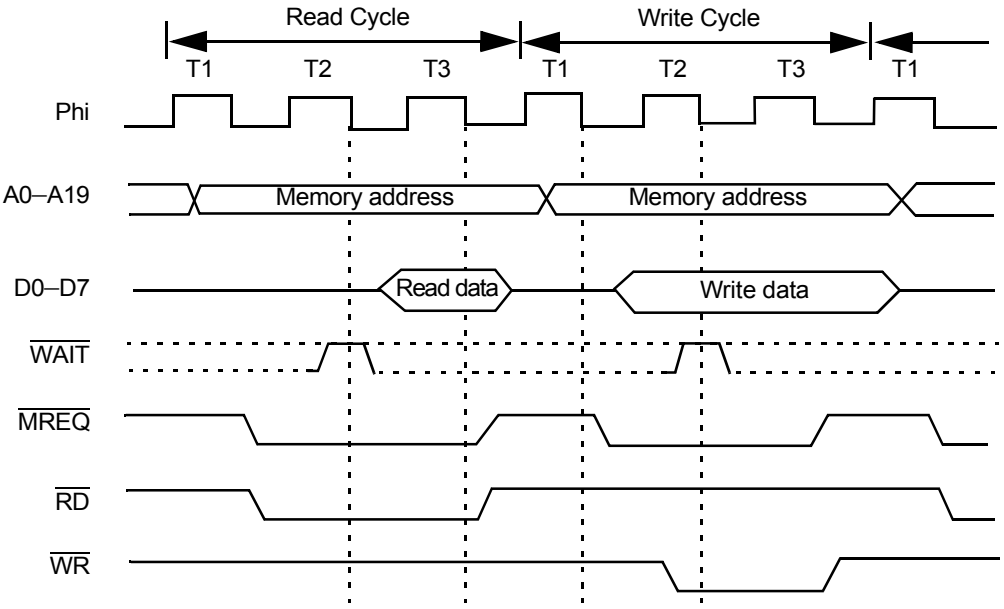


Figure 11. Memory Read/Write (without Wait State) Timing Diagram

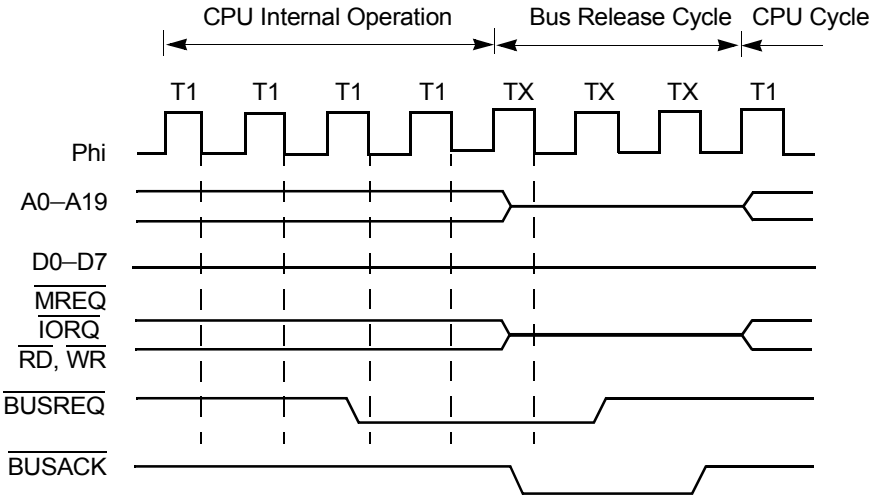


Figure 17. Bus Exchange Timing During CPU Internal Operation

Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

Note: $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

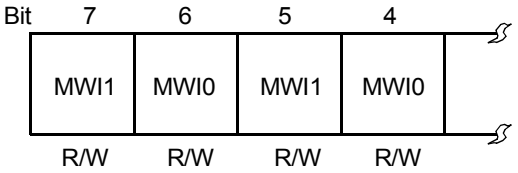


Figure 19. Memory and I/O Wait State Insertion (DCNTL – DMA/Wait Control Register)

The number of Wait States (TW) inserted in a specific cycle is the maximum of the number requested by the $\overline{\text{WAIT}}$ input, and the number automatically generated by the on-chip Wait State generator.

Bit 7, 6: MWI1 MWI0, (Memory Wait Insertion)

For CPU and DMAC cycles which access memory (including memory mapped I/O), zero to three Wait States may be automatically inserted depending on the programmed value in MWI1 and MWI0 as depicted in Table 3

Table 3. Memory Wait States

MW11	MWI0	The Number of Wait States
0	0	0
0	1	1
1	0	2
1	1	3

Bit 5, 4: IWI1, IWI0 (I/O Wait Insertion)

For CPU and DMA cycles which access external I/O (and interrupt acknowledge cycles), one to six Wait States (TW) may be automatically

cycle is extended to 4 clocks by automatic insertion of one internal Ti state.

DMAC Channel Priority

For simultaneous $\overline{\text{DREQ0}}$ and $\overline{\text{DREQ1}}$ requests, channel 0 has priority over channel 1. When channel 0 is performing a memory to/from memory transfer, channel 1 cannot operate until the channel 0 operation has terminated. If channel 1 is operating, channel 0 cannot operate until channel 1 releases control of the bus.

DMAC and BUSREQ, BUSACK

The $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$ inputs allow another bus master to take control of the Z8X180 bus. $\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$ take priority over the on-chip DMAC and suspends DMAC operation. The DMAC releases the bus to the external bus master at the breakpoint of the DMAC memory or I/O access. Since a single byte DMAC transfer requires a read and a write cycle, it is possible for the DMAC to be suspended after the DMAC read, but before the DMAC write. Hence, when the external master releases the Z8X180 bus ($\overline{\text{BUSREQ}}$ High), the on-chip DMAC correctly continues the suspended DMA operation.

Bit Position	Bit/Field	R/W	Value	Description
0	Send Break	R/W	0 1	Normal Xmit Drive TXA Low

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

ASCI1 Extension Control Register (I/O Address: 13H) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF Int Inhibit	Reserved		X1 Bit Clk ASCI1	BRG1 Mode	Break Feature Enable	Break Detect (RO)	Send Break
R/W	R/W	?		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF Interrupt Inhibit	R/W	0 1	RDRF Interrupt Inhibit On RDRF Interrupt Inhibit Off
6–5	Reserved	?	0	Reserved. Must be 0
4	X1 Bit Clk ASCI1	R/W	0 1	CKA1 /16 or /64 CKA1 is bit clock
3	BRG1 Mode	R/W	0 1	As S180 Enable 16-bit BRG counter

control register. The PRT input clock for both channels is equal to the system clock divided by 20.

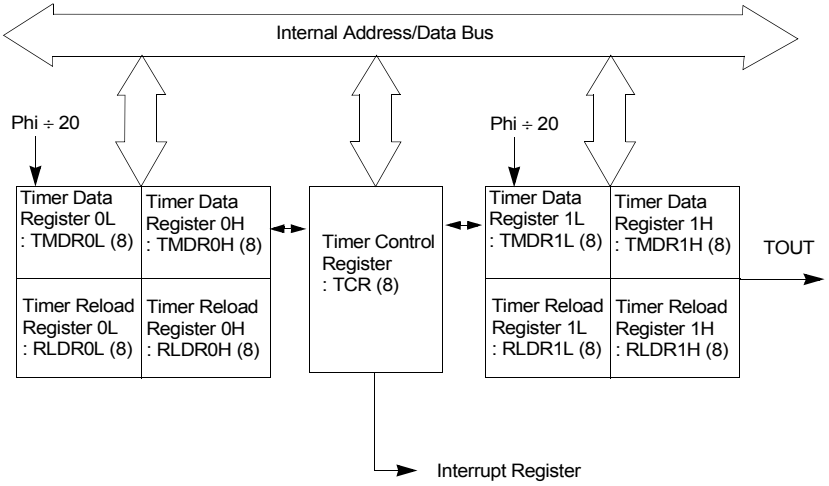


Figure 63. PRT Block Diagram

PRT Register Description

Timer Data Register (TMDR: I/O Address - CH0: 0CH, 0DH; CH1: 15H, 14H). PRT0 and PRT1 each contain 16-bit timer Data Registers (TMDR). TMDR0 and TMDR1 are each accessed as low and high byte registers (TMDR0H, TMDR0L and TMDR1H, TMDR1L). During RESET, TMDR0 and TMDR1 are set to FFFFH.

TMDR is decremented once every twenty clocks. When TMDR counts down to 0, it is automatically reloaded with the value contained in the Reload Register (RLDR).

TMDR is read and written by software using the following procedures. The read procedure uses a PRT internal temporary storage register to

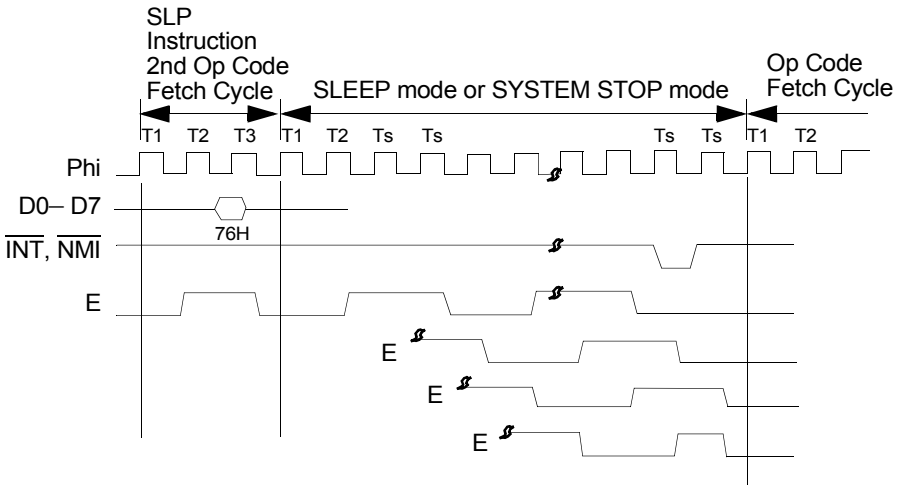


Figure 69. E Clock Timing in SLEEP Mode and SYSTEM STOP Mode

On-Chip Clock Generator

The Z8X180 contains a crystal oscillator and system clock generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock is equal to one-half the input clock. For example, a crystal or external clock input of 8 MHz corresponds with a system clock rate of 4 MHz.

Z8S180 and Z8L180-class processors also have the ability to run at X1 and X2 input clock.

Table 25 describes the AT cut crystal characteristics (Co, Rs) and the load capacitance (CL1, CL2) required for various frequencies of Z8X180 operation.

MLT- Multiply

The MLT performs unsigned multiplication on two 8-bit numbers yielding a 16-bit result. MLT may specify BC, DE, HL, or SP registers. The 8-bit operands are loaded into each half of the 16-bit register and the 16-bit result is returned in that register.

OTIM, OTIMR, OTDM, OTDMR - Block I/O

The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR, respectively. The B register is decremented. The OTIMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as Z80180 on-chip I/O) initialization. When I/O is accessed, 00H is output in high-order bits of address automatically.

TSTIO m - Test I/O Port

The contents of the I/O port addressed by C are ANDed with immediately specified 8-bit data and the status flags are updated. The I/O port contents are not written (non-destructive AND). When I/O is accessed, `00H` is output in higher bits of address automatically.

TST g - Test Register

Perform an `AND` instruction on the contents of the specified register with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive `AND`).

TST m - Test Immediate

Perform an `AND` instruction on the contents of the immediately specified 8-bit data with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive `AND`).

Figure 74 depicts CPU register configurations.

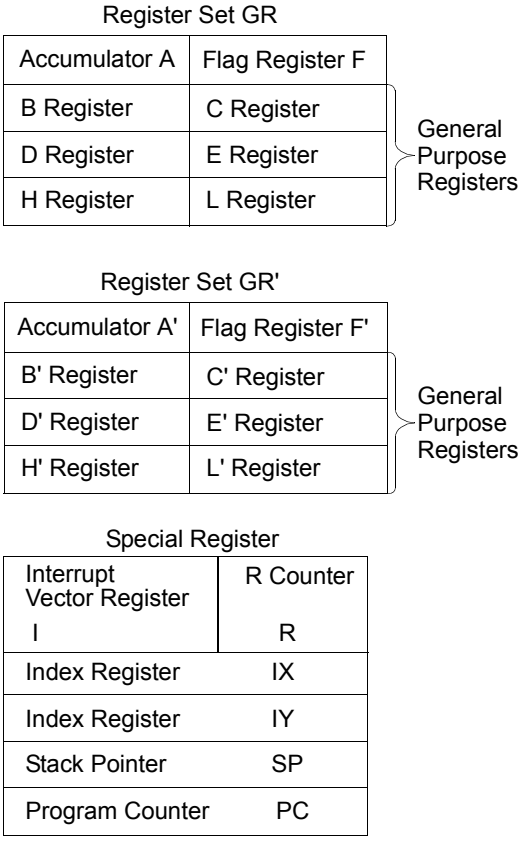


Figure 74. CPU Register Configurations

Accumulator (A, A')

The Accumulator (A) is the primary register used for many arithmetic, logical, and I/O instructions.

8-bit Register

g or g field '	Register
0	B
0 0 1	C
0 1 0	D
0 1 1	E
1 0 0	H
1 0 1	L
1 1 0	—
1 1 1	A

ww field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	S P

xx field	Register
0 0	B C
0 1	D E
1 0	I X
1 1	S P

16-bit Register

zz field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	A F

yy field	Register
0 0	B C
0 1	D E
1 0	I Y
1 1	S P

Suffixed H and L ww,xx,yy,zz (ex. wwH,IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

Figure 75. Register Direct — Bit Field Definitions

Register Indirect (REG)

The memory operand address is contained in one of the 16-bit General Purpose Registers (BC, DE, and HL) as illustrated in Figure 76.

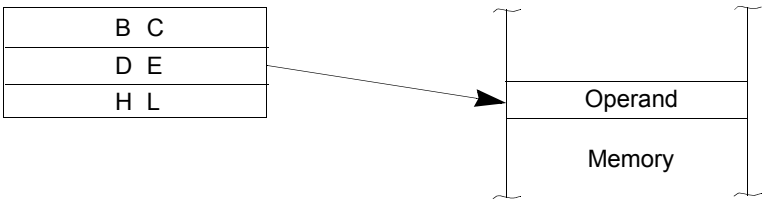
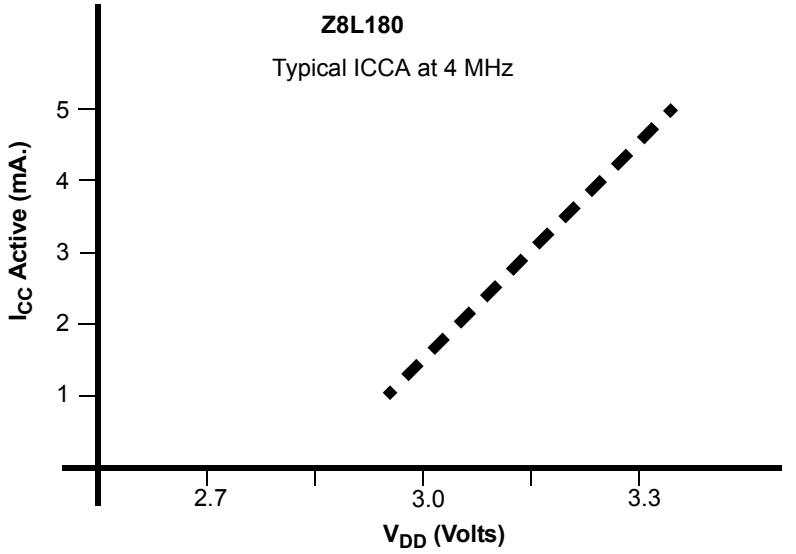


Figure 76. Register Indirect Addressing


Z8L180
Typical ICCA at 4 MHz
I_{CC} Active (mA.)
5
4
3
2
1
2.7
3.0
3.3
V_{DD} (Volts)

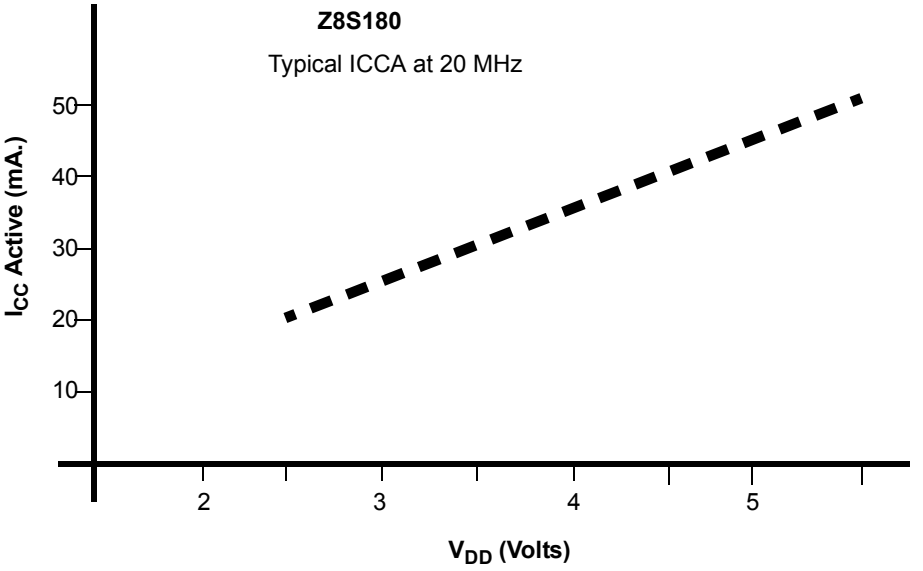

Z8S180
Typical ICCA at 20 MHz
I_{CC} Active (mA.)
50
40
30
20
10
2
3
4
5
V_{DD} (Volts)

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
12	t_{MED2}	PHI Fall to $\overline{MREQ}$ Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to $\overline{RD}$ Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to $\overline{WR}$ Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to $\overline{WR}$ Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to $\overline{WR}$ Rise Delay	—	25	—	15	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		$\overline{WR}$ Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from $\overline{WR}$ Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0	—	25	—	15	
29	t_{IOD2}	PHI Fall to $\overline{IORQ}$ Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	125	—	80	—	ns

MISCELLANEOUS

Table 37 lists the operations mnemonics.

Table 37. Operations Mnemonics

$( )_M$	Data in the memory address
$( )_I$	Data in the I/O address
m or n	8-bit data
mn	16-bit data
r	8-bit register
R	16-bit register
$b.( )_M$	A content of bit b in the memory address
b.gr	A content of bit b in the register gr
d or j	8-bit signed displacement
S	Source
D	Destination
•	AND operation
+	OR operation
⊕	EXCLUSIVE OR operation
**	Added new instructions to Z80

Table 46. I/O Instructions

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
INPUT	IN A,(m)	11 011 011 <m>						D	S	2	9	(Am)1,→Ar m→A0~A7 Ar→A8~A16	•	•	•	•	•	•
	IN g,(C)	11 101 101 01 g 000				D			S	2	9	(BC)1→gr g = 110 : Only the flags change Cr→A0~A7 Br→A8~16	↑	↑	R	P	R	•
	IN0 g,(m)**	11 101 101 00 g 000 <m>				D			S	3	12	(00m)g→gr g = 110 : Only the flags change m→A0~A7 (00)→A8~A16	↑	↑ (5)	R	P	R (6)	•
	IND	11 101 101 10 101 010					D		S	2	12	$(BC)_M \rightarrow (HL)_M$ HI2→1→HI2 Br→1→Br Cr→A0~A7	X	↑	X	X	↑ (6)	X
	INDR	11 101 101 10 111 010					D		S	2	14 (Br ≠ 0) 12 (BR = 0)	Q $(BC)1 \rightarrow (HL)_M$ HL2→1→HL8 Br-1→Br Repeat Q until Br = 0 Cr→A0~A7 Br→A8~A16	X	S (5)	X	X	↑ (6)	X
	INI	11 101 101 10 100 010					D		S	2	12	$(BC)1 \rightarrow (HL)_M$ $HL_R + 1 \rightarrow HL_R$ Br-1→Br Cr→A0~A7 Br→A8~A16	X	↑	X	X	↑ (6)	X

MNEMONICS	Bytes	Machine Cycles	States
LD (DE),A	1	3	7
LD ww,mn	3	3	9
LD ww,(mn)	4	6	18
LDDR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$
LD (HL),m	2	3	9
LD HL,(mn)	3	5	15
LD (HL),g	1	3	7
LDI	2	4	12
LDI,A	2	2	6
LDIR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$)
LD IX,mn	4	4	12
LID IX,(mn)	4	6	18
LD (IX+d),m	4	5	15
LD (IX+ d),g	3	7	15
LD IY,mn	4	4	12
LD IY,(mn)	4	6	18
LD (IY+d),m	4	5	15
LD (IY+d),g	3	7	15
LD (mn),A	3	5	13
LD (mn),ww	4	7	19
LD (mn),HL	3	6	16
LD (mn),IX	4	7	19
LD (mn),IY	4	7	19
LD R,A	2	2	6
LD g,(HL)	1	2	6
LD g,(IX+d)	3	6	14
LD g,(IY+d)	3	6	14
LD g,m	2	2	6

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (IX+d),m LD (IY+d),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
LD A, (BC) LD A, (DE)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	BC DE	DATA	0	1	0	1	1	1	1
LD A,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
LD (BC),A LD (DE),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	BC DE	A	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (mn),IX LD (mn),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	IXL IYL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	IXH IYH	1	0	0	1	1	1	1
LD SP, HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
LD SP,IX LD SP,IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
LDI LDD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1