Zilog - Z8018010FEC00TR Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010fec00tr

MANUAL OBJECTIVES

This user manual describes the features of the Z8018x MPUs.This manual provides basic programming information for the Z80180/Z8S180/ Z8L180. These cores and base peripheral sets are used in a large family of ZiLOG products. Below is a list of ZiLOG products that use this class of processor, along with the associated processor family. This document is also the core user manual for the following products:

Part	Family
Z80180	Z80180
Z8S180	Z8S180
Z8L180	Z8L180
Z80181	Z80180
Z80182	Z80180, Z8S180*
Z80S183	Z8S180
Z80185/195	Z8S180
Z80189	Z8S180

* Part number-dependant

Intended Audience

This manual is written for those who program the Z8018x.

Manual Organization

The Z8018x User Manual is divided into five sections, seven appendices, and an index.

To avoid address conflicts with external I/O, the Z8X180 internal I/O addresses can be relocated on 64-byte boundaries within the bottom 256 bytes of the 64KB I/O address space.

I/O Control Register (ICR)

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode.

I/O Control Register (ICR: 3FH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	IOA7	IOA6	IOSTP	—	—	—	—	—
R/W	R/W	R/W	R/W					
Reset	0	0	0					

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–6	IOA7:6	R/W		IOA7 and IOA6 relocate internal I/O as depicted in Figure . The high-order 8 bits of 16-bit internal I/O addresses are always 0. IOA7 and IOA6 are cleared to 0 during RESET.
5	IOSTP	R/W		IOSTOP mode is enabled when IOSTP is set to 1. Normal. I/O operation resumes when IOSTP is reset to 0.

Clock Multiplier Register (CMR: 1EH) (Z8S180/L180-Class Processors Only)

Bit	7	6						0
Bit/Field	X2	Reserved						
R/W	R/W	?						
Reset	0	1						

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	X2 Clock Multiplier Mode	R/W		X2 Clock Multiplier Mode
			0	Disable
			1	Enable
6–0	Reserved	?	?	Reserved

MMU Bank Base Register (BBR)

BBR specifies the base address (on 4KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register (BBR: 39H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–0	BB7–0	R/W		BBR specifies the base address (on 4KB boundaries) used to generate a 20-bit physical address for Bank Area accesses.

Physical Address Translation

Figure 29 illustrates the way in which physical addresses are generated based on the contents of CBAR, CBR and BBR. MMU comparators classify an access by logical area as defined by CBAR. Depending on which of the three potential logical areas (Common Area 1, Bank Area, or Common Area 0) is being accessed, the appropriate 8- or 7-bit base address is added to the high-order 4 bits of the logical address, yielding a 19- or 20-bit physical address. CBR is associated with Common Area 1 accesses. Common Area 0, if defined, is always based at physical address 00000H.

disabling all maskable interrupts. The interrupt service routine normally terminates with the EI (Enable Interrupts) instruction followed by the RETI (Return from Interrupt) instruction, to reenable the interrupts. Figure 37 depicts the use of $\overline{\text{INT0}}$ (Mode 1) and RETI for the Mode 1 interrupt sequence.

Figure 37. INT0 Mode 1 Interrupt Sequence

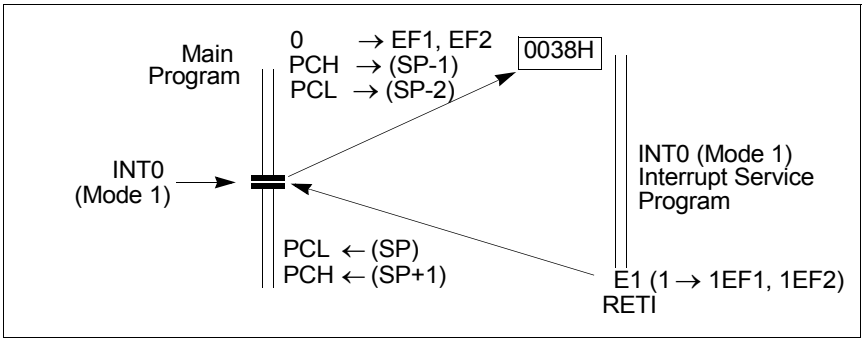

Figure 38 illustrates $\overline{\text{INT0}}$ Mode 1 Timing.

also the interrupt response sequence used for all internal interrupts (except TRAP).

As depicted in Figure 41, the low-order byte of the vector table address has the most significant three bits of the software programmable IL register while the least significant five bits are a unique fixed value for each interrupt ($\overline{INT1}$, $\overline{INT2}$ and internal) source:

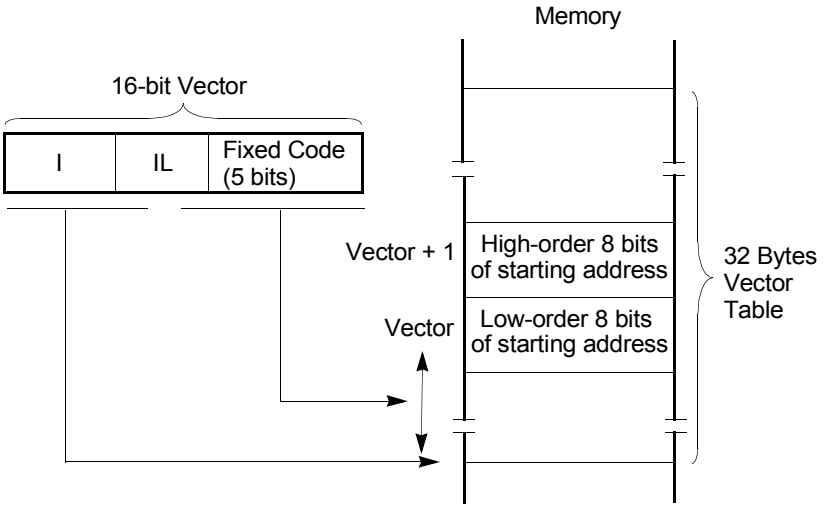

Figure 41. $\overline{INT1}$, $\overline{INT2}$ Vector Acquisition

$\overline{INT1}$ and $\overline{INT2}$ are globally masked by IEF1 is `0`. Each is also individually maskable by respectively clearing the ITE1 and ITE2 (bits 1,2) of the INT/TRAP control register to `0`.

During RESET, IEF1, ITE1 and ITE2 bits are reset to `0`.

Internal Interrupts

Internal interrupts (except TRAP) use the same vectored response mode as $\overline{INT1}$ and $\overline{INT2}$. Internal interrupts are globally masked by IEF1 is `0`. Individual internal interrupts are enabled/disabled by programming each

Z8X180. Figure 43 illustrates the INT1, INT2 and internal interrupts timing.

Table 10. RETI Control Signal States

Machine Cycle	States	Address	Data	$\overline{MI}$							
				$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1E=1}$	$\overline{M1E=0}$	$\overline{HALT}$	ST
1	T1-T3	1st Op Code	EDH	0	1	0	1	0	1	1	0
2	TI-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
3	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
4	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
5	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
6	T1-T3	1st Op Code	EDH	0	1	0	1	0	0	1	1
7	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
8	T1-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
9	T1-T3	SP	data	0	1	0	1	1	1	1	1
10	T1-T3	SP+1	data	0	1	0	1	1	1	1	1

IOC affects the IORQ/RD signals. M1E affects the assertion of M1. One state also reflects a 1 while the other reflects a 0

Bit Position	Bit/Field	R/W	Value	Description
3–2	SM1:0	W		**Source Mode Channel** — Specifies whether the source for channel 0 transfers is memory, I/O, or memory mapped I/O and the corresponding address modifier. Reference Table 13.
1	MMOD	R/W		**DMA Memory Mode Channel 0** — When channel 0 is configured for memory to/from memory transfers, the external $\overline{\text{DREQ}}$0 input is not used to control the transfer timing. Instead, two automatic transfer timing modes are selectable - BURST (MMOD is 1) and CYCLE STEAL (MMOD is 0). For BURST memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as shown by the byte count register is 0). In CYCLE STEAL mode, the CPU is given a cycle for each DMA byte transfer cycle until the transfer is completed. For channel 0 DMA with I/O source or destination, the $\overline{\text{DREQ}}$0 input times the transfer and thus MMOD is ignored.

Table 12. Channel 0 Destination

DM1	DM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Memory to I/O (Memory Mapped I/O) — Channel 0

For memory to/from I/O (and memory to/from memory mapped I/O) the $\overline{\text{DREQ0}}$ input is used to time the DMA transfers. In addition, the $\overline{\text{TEND0}}$ (Transfer End) output is used to indicate the last (byte count register BCR0 = 00H) transfer.

The $\overline{\text{DREQ0}}$ input can be programmed as level- or edge-sensitive.

When level-sense is programmed, the DMA operation begins when $\overline{\text{DREQ0}}$ is sampled Low. If $\overline{\text{DREQ0}}$ is sampled High, after the next DMA byte transfer, control is relinquished to the Z8X180 CPU. As illustrated in Figure 47, $\overline{\text{DREQ0}}$ is sampled at the rising edge of the clock cycle prior to T3, (that is, either T2 or Tw).

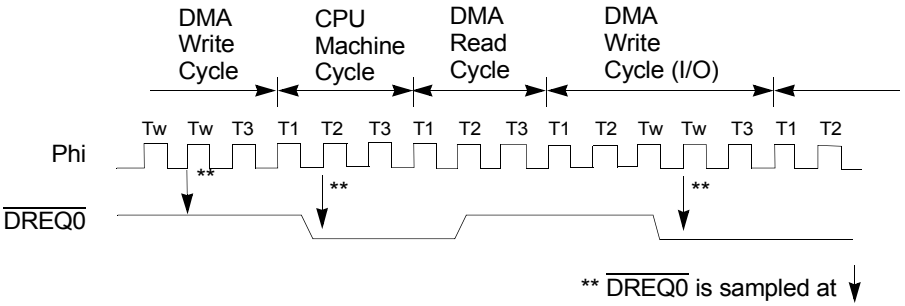

Figure 47. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Level-Sense

When edge-sense is programmed, DMA operation begins at the falling edge of $\overline{\text{DREQ0}}$ If another falling edge is detected before the rising edge of the clock prior to T3 during DMA write cycle (that is T2 or Tw), the DMAC continues operating. If an edge is not detected, the CPU is given control after the current byte DMA transfer completes. The CPU continues operating until a $\overline{\text{DREQ0}}$ falling edge is detected before the

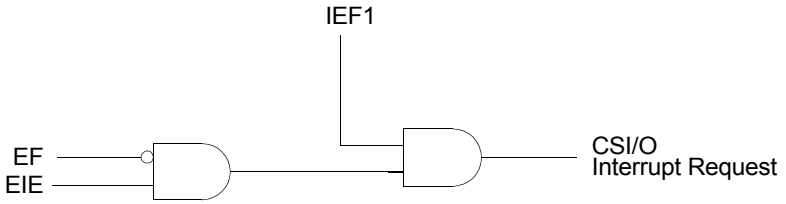

Figure 58. CSI/O Interrupt Request Generation

CSI/O Operation

The CSI/O is operated using status polling or interrupt driven algorithms.

- Transmit–Polling
  a. Poll the TE bit in CNTR until TE = 0.
  b. Write the transmit data into TRDR.
  c. Set the TE bit in CNTR to 1.
  d. Repeat steps 1 to 3 for each transmit data byte.
- Transmit–Interrupts
  a. Poll the TE bit in CNTR until TE = 0.
  b. Write the first transmit data byte into TRDR.
  c. Set the TE and EIE bits in CNTR to 1.
  d. When the transmit interrupt occurs, write the next transmit data byte into TRDR.
  e. Set the TE bit in CNTR to 1.
  f. Repeat steps 4 and 5 for each transmit data byte.
- Receive –Polling
  a. Poll the RE bit in CNTR until RE = 0.
  b. Set the RE bit in CNTR to 1.

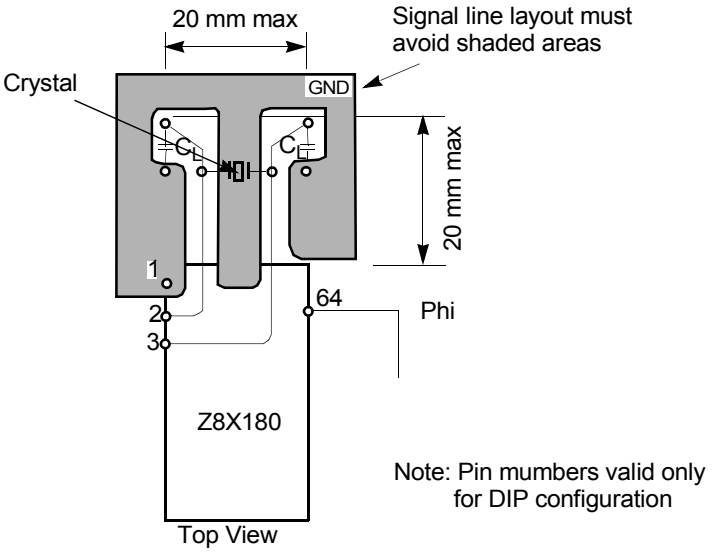

Figure 73. Example of Board Design

Circuit Board design should observe the following parameters.

- Locate the crystal and load capacitors as close to the IC as physically possible to reduce noise.
- Signal lines must not run parallel to the clock oscillator inputs. In particular, the clock input circuitry and the system clock output (pin 64) must be separated as much as possible.
- V_{CC} power lines must be separated from the clock oscillator input circuitry.
- Resistivity between XTAL or EXTAL and the other pins must be greater than 10M ohms.

Signal line layout must avoid areas marked with the shaded area of Figure 73.

Figure 74 depicts CPU register configurations.

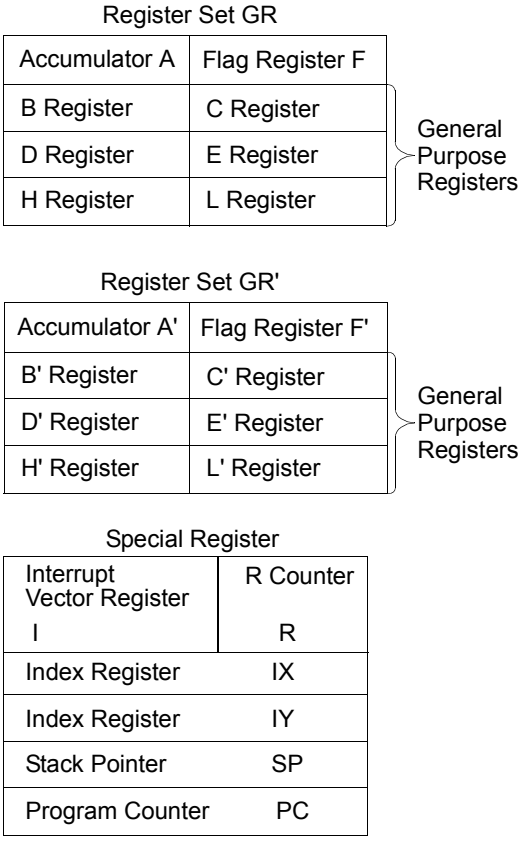

Figure 74. CPU Register Configurations

Accumulator (A, A')

The Accumulator (A) is the primary register used for many arithmetic, logical, and I/O instructions.

Table 40. Arithmetic Instructions (16-bit)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
ADD	ADD HL,ww	00 ww1 001				S		D		1	7	$HL_R + ww_R \rightarrow HL_R$	•	•	X	•	R	↑
	ADD IX,xx	11 011 101 00 xx1 001				S		D		2	10	$IX_R + xx_R \rightarrow {}^*IX_R$	•	•	X	•	R	↑
	ADD IY,yy	11 111 101 00 yy1 001				S		D		2	10	$IY_R + yy_R \rightarrow IY_R$	•	•	X	•	R	↑
ADC	ADC HL,ww	11 101 101 01 ww1 010				S		D		2	10	$HL_R + ww_R + c \rightarrow HL_R$	↑	↑	X	V	R	↑
DEC	DEC ww	00 ww1 011				S/D				1	4	$ww_R - 1 \rightarrow \bullet ww_R$	•	•	•	•	•	•
	DEC IX	11 011 101 00 101 011						S/D		2	7	$1X_R - 1 \rightarrow IX_R$	•	•	•	•	•	•
	DEC IY	11 111 101 00 101 011						S/D		2	7	$1Y_R - 1 \rightarrow IY_R$	•	•	•	•	•	•
INC	INC ww	00 ww 0011				S/D				1	4	$ww_R + 1 \rightarrow ww_R$	•	•	•	•	•	•
	INC IX	11 011 101 00 100 011						S/D		2	7	$1X_R + 1 \rightarrow IX_R$	•	•	•	•	•	•
	INC IY	11 111 101 00 100 011						S/D		2	7	$1Y_R + 1 \rightarrow IY_R$	•	•	•	•	•	•
SBC	SBC HL ww	11 101 101 01 ww0 010				S		D		2	10	$HL_R - ww_R - c \rightarrow HL_R$	↑	↑	X	V	S	↑

Instruction Summary

** : Added new instructions to Z80

MNEMONICS	Bytes	Machine Cycles	States
ADC A,m	2	2	6
ADC A,g	1	2	4
ADC A, (HL)	1	2	6
ADC A, (IX+d)	3	6	14
ADC A, (IY+d)	3	6	14
ADD A,m	2	2	6
ADD A,g	1	2	4
ADD A, (HL)	1	2	6
ADD A, (IX+d)	3	6	14
ADD A, (IY+d)	3	6	14
ADC HL,ww	2	6	10
ADD HL,ww	1	5	7
ADD IX,xx	2	6	10
ADD IY,yy	2	6	10
AND m	2	2	6
AND g	1	2	4
AND (HL)	1	2	6
AND (IX+d)	3	6	14
AND (IY+d)	3	6	14
BIT b, HU	2	3	9
BIT b, (IX+d)	4	5	15
BIT b, (IY+d)	4	5	15
BIT b,g	2	2	6
CALL f,mn	3	2	6 (If condition is false)

MNEMONICS	Bytes	Machine Cycles	States
LD (DE),A	1	3	7
LD ww,mn	3	3	9
LD ww,(mn)	4	6	18
LDDR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$
LD (HL),m	2	3	9
LD HL,(mn)	3	5	15
LD (HL),g	1	3	7
LDI	2	4	12
LDI,A	2	2	6
LDIR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$)
LD IX,mn	4	4	12
LID IX,(mn)	4	6	18
LD (IX+d),m	4	5	15
LD (IX+ d),g	3	7	15
LD IY,mn	4	4	12
LD IY,(mn)	4	6	18
LD (IY+d),m	4	5	15
LD (IY+d),g	3	7	15
LD (mn),A	3	5	13
LD (mn),ww	4	7	19
LD (mn),HL	3	6	16
LD (mn),IX	4	7	19
LD (mn),IY	4	7	19
LD R,A	2	2	6
LD g,(HL)	1	2	6
LD g,(IX+d)	3	6	14
LD g,(IY+d)	3	6	14
LD g,m	2	2	6

MNEMONICS	Bytes	Machine Cycles	States
PUSH IX	2	6	14
PUSH IY	2	6	14
PUSH zz	1	5	11
RES b,(HL)	2	5	13
RES b,(IX+d)	4	7	19
RES b,(IY+d)	4	7	19
RES b,g	2	3	7
RET	1	3	9
RET f	1	3	5
			(If condition is false)
	1	4	10
			(If condition is true)
RETI	2	4 (R0, R1)	12 (R0, R1)
	10 (Z)		22 (Z)
RETN	2	4	12
RLA	1	1	3
RLCA	1	1	3
RLC (HL)	2	5	13
RLC (IX-1-dl	4	7	19
RLC (IY+d)	4	7	19
RLC g	2	3	7
RLD	2	8	16
RL (HL)	2	5	13
RL (IX+d)	4	7	19
RL (IY+d)	4	7	19
RL g	2	3	7
RRA	1	1	3
RRCA	1	1	3
RRC (HL)	2	5	13
RRC (IX+d)	4	7	19

Table 49. 2nd Op Code Map Instruction Format: CB XX

				b (L0 = 0~7)													
				0	2	4	6	0	2	4	6	0	2	4	6		
		HI		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		LO		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
g (HI = ALL)	B	0000	0	RLC g	RL g	SLA g		BIT b,g				RES b,g				SET b,g				0
	C	0001	1																	1
	D	0010	2																	2
	E	0011	3																	3
	H	0100	4																	4
	L	0101	5																	5
	(HL)	0110	6	NOTE 1)	NOTE 1)	NOTE 1)		NOTE1)				NOTE1)				NOTE1)				6
	A	0111	7																	7
	B	1000	8	RRC g	RR g	SRA g	SRL g	BIT b,g				RES b,g				SET b,g				8
	C	1001	9																	9
	D	1010	A																	A
	E	1011	B																	B
	H	1100	C																	C
	L	1101	D																	D
	(HL)	1110	E	NOTE 1)	NOTE 1)	NOTE 1)	NOTE 1)	NOTE1)				NOTE1)				NOTE 1)				E
	A	1111	F																	F
				0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
								1	3	5	7	1	3	5	7	1	3	5	7	
				b (LO = 8 ~ F)																

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LDIR LDDR (If BCR≠0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
	MC5~MC6	TiTi	*	Z	1	1	1	1	1	1	1
LDIR LDDR (If BCR=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	DE	DATA	1	0	0	1	1	1	1
MLT ww**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC13	TiTiTTi TiTiTiTi TiTiTi	*	Z	1	1	1	1	1	1	1
NEG	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
NOP	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RST v	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC3	TiTi	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
SCF	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
SET b,g RES b,g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
SET b. (HL) RES b, (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2ndOp Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Status Channel 0:	STAT0	0	4	

bit	RDRF	OVRN	PE	FE	RIE	$\overline{DCD0}$	TDRE	TIE
during RESET	0	0	0	0	invalid	*	**	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
Data Carrier Detect
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full

** $\overline{CTS_0}$ Pin	TDRE
L	1
H	0

* $\overline{DCD_0}$: Depending on the condition of $\overline{DCD_0}$ Pin.

ASCI Status Channel 1:	STAT1	0	5

bit	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
during RESET	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W	R	R	R/W

Transmit Interrupt Enable
Transmit Data Register Empty
$\overline{CTS1}$ Enable
Receive Interrupt Enable
Framing Error
Parity Error
Overrun Error
Receive Data Register Full