# Zilog - Z8018010FEG Datasheet


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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 10MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 80-BQFP |
| Supplier Device Package | 80-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018010feg |

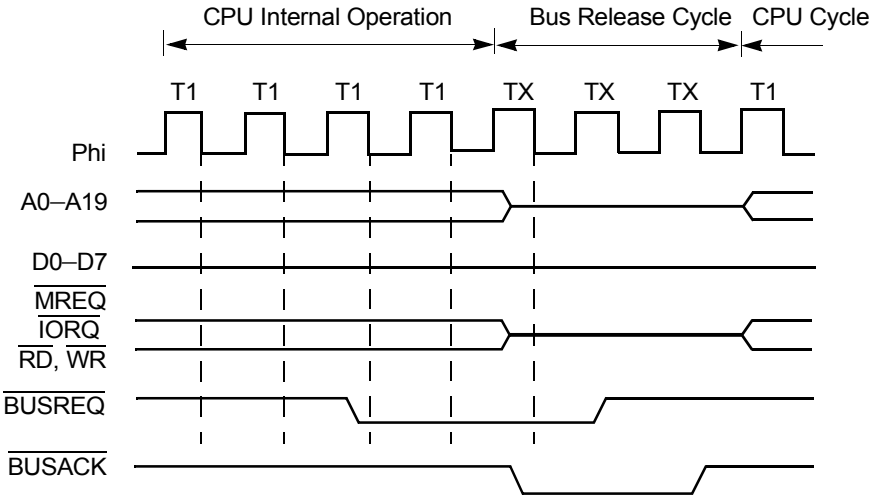


**Figure 17. Bus Exchange Timing During CPU Internal Operation**

## Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

**Note:** $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the $\overline{\text{BUSREQ}}$ does not cause the Z8S180/Z8L180-class processors to exit STANDBY mode.

If STANDBY mode is exited because of a reset or an external interrupt, the Z8S180/Z8L180-class processors remains relinquished from the system bus as long as $\overline{\text{BUSREQ}}$ is active.

## STANDBY Mode EXit with External Interrupts

STANDBY mode can be exited by asserting input $\overline{\text{NMI}}$. The STANDBY mode may also exit by asserting $\overline{\text{INT0}}$. $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$, depending on the conditions specified in the following paragraphs.

$\overline{\text{INT0}}$ wake-up requires assertion throughout duration of clock stabilization time ($2^{17}$ clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180/Z8L180-class processors resume.

- Exit with Non-Maskable Interrupts

  If $\overline{\text{NMI}}$ is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

- Exit with External Maskable Interrupts

  If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H).

If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input does not cause the Z8S180/Z8L180-class processors to exit STANDBY mode. This condition is true regardless of the state of the Global Interrupt Enable Flag IEF1.

except that the $2^{17}$ bit wake-up timer is bypassed. All control signals are asserted eight clock cycles after the exit conditions are gathered.

## STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from $2^{17}$ clock cycles (4 µs at 33 MHz) to $2^{6}$ clock cycles (1.9 µs at 33 MHz). This feature can only be used when providing an oscillator as clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set bits 6 and 3 to `1` and `1`, respectively.
2. Set the I/O STOP bit (bit 5 of ICR, I/O Address = `3FH`) to `1`.
3. Execute the SLEEP instruction

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, using RESET, BUS REQUEST or EXTERNAL INTERRUPTS. The clock and other control signals are recovered sooner than the STANDBY mode.

**Note:** If STANDBY-QUICK RECOVERY is enabled, the user must ensure stable oscillation is obtained within 64 clock cycles

## Internal I/O Registers

The Z8X180 internal I/O Registers occupy 64 I/O addresses (including reserved addresses). These registers access the internal I/O modules (ASCI, CSI/O, PRT) and control functions (DMAC, DRAM refresh, interrupts, wait state generator, MMU and I/O relocation).

**Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)**

| | Register | Mnemonic | Address | | |
|---|---|---|---|---|---|
| | | | Binary | Hex | Page |
| Timer | Data Register Ch 0 L | TMDR0L | XX001100 | 0CH | 159 |
| | Data Register Ch 0 H | TMDR0H | XX001101 | 0DH | 159 |
| | Reload Register Ch 0 L | RLDR0L | XX001110 | 0EH | 159 |
| | Reload Register Ch 0 H | RLDR0H | XX001111 | 0FH | 159 |
| | Timer Control Register | TCR | XX010000 | 10H | 161 |
| | Reserved | | XX010001 | 11H | |
| | Data Register Ch 1 L | TMDR1L | XX010100 | 14H | 160 |
| | Data Register Ch 1 H | TMDR1H | XX010101 | 15H | 160 |
| | Reload Register Ch 1 L | RLDR1L | XX010110 | 16H | 160 |
| | Reload Register Ch 1 H | RLDR1H | XX010111 | 17H | 160 |
| Others | Free Running Counter | FRC | XX011000 | 18H | 172 |
| | Reserved | | XX011001 | 19H | |
| | | | ⇕ | ⇕ | |
| | | | XX011111 | 1DH | |
| | Clock Multiplier Register | CMR | XX011110 | 1EH | 52 |
| | CPU Control Register | CCR | XX011111 | 1FH | 53 |

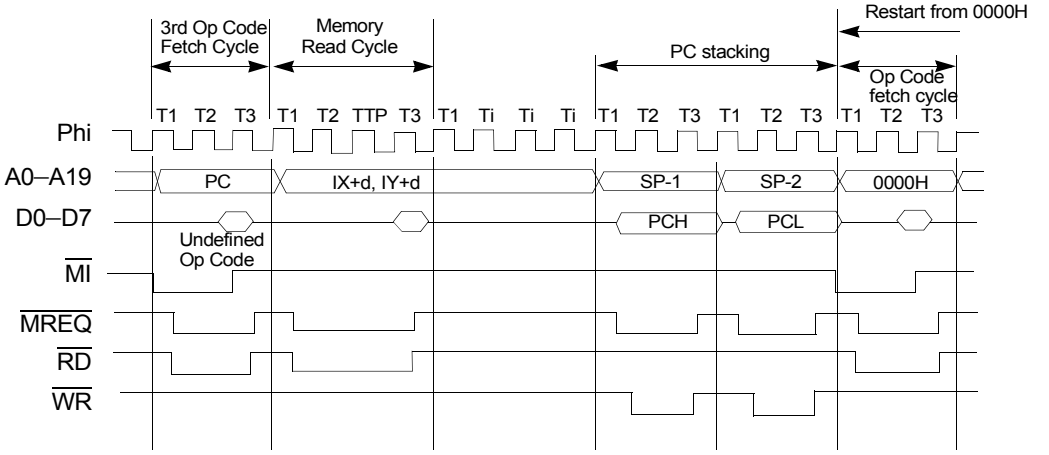


**Figure 33. TRAP Timing - 3rd Op Code Undefined**

### External Interrupts

The Z8X180 features four external hardware interrupt inputs:

- $\overline{\text{NMI}}$–Non-maskable interrupt
- $\overline{\text{INT0}}$–Maskable Interrupt Level 0
- $\overline{\text{INT1}}$–Maskable Interrupt Level 1
- $\overline{\text{INT2}}$–Maskable Interrupt Level 2

$\overline{\text{NMI}}$, $\overline{\text{INT1}}$, and $\overline{\text{INT2}}$ feature fixed interrupt response modes. $\overline{\text{INT0}}$ has 3 different software programmable interrupt response modes—Mode 0, Mode 1 and Mode 2.

### $\overline{\text{NMI}}$ - Non-Maskable Interrupt

The **$\overline{\text{NMI}}$** interrupt input is edge-sensitive and cannot be masked by software. When **$\overline{\text{NMI}}$** is detected, the Z8X180 operates as follows:

**Table 14. Transfer Mode Combinations**

| DM1 | DM0 | SM1 | SM0 | Transfer Mode | Increment/Decrement |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | Memory to I/O | SAR0+1, DAR0 fixed |
| 1 | 1 | 0 | 1 | Memory to I/O | SAR0-1, DAR0 fixed |
| 1 | 1 | 1 | 0 | Reserved | |
| 1 | 1 | 1 | 1 | Reserved | |
| Note: *: includes memory mapped I/O. | | | | | |

## DMA/WAIT Control Register (DCNTL)

DCNTL controls the insertion of Wait States into DMAC (and CPU) accesses of memory or I/O Also, the DMA request mode for each DREQ $\overline{\text{DREQ}}$0 and $\overline{\text{DREQ}}$1) input is defined as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

rising edge of the clock prior to T3 at which time the DMA operation (re)starts. Figure 48 depicts the edge-sense DMA timing.

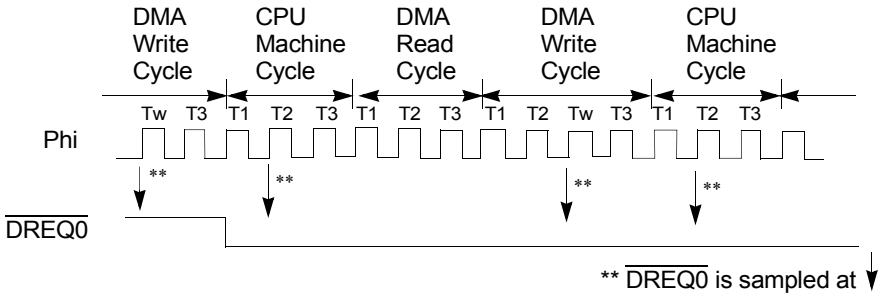


**Figure 48. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Edge-Sense**

During the transfers for channel 0, the $\overline{\text{TEND0}}$ output goes Low synchronous with the write cycle of the last (BCR0 = 00H) DMA transfer (Reference Figure 49).

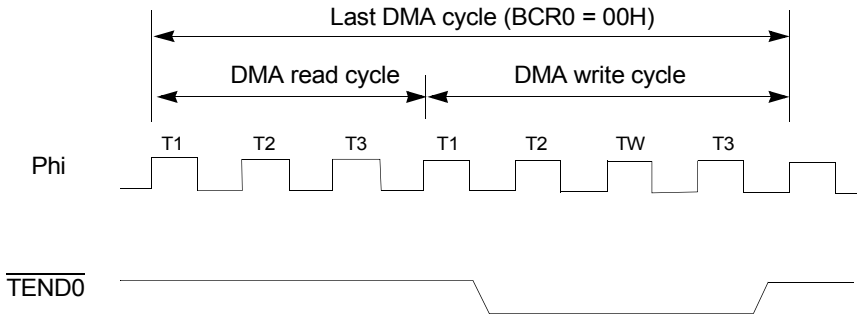


**Figure 49. $\overline{\text{TEND0}}$ Output Timing Diagram**

The $\overline{\text{DREQ0}}$ and $\overline{\text{TEND0}}$ pins are programmably multiplexed with the CKA0 and CKA1 ASCI clock input/outputs. However, when DMA channel 0 is programmed for memory to/from I/O (and memory to/from

**Table 17. Data Formats**

| MOD2 | MOD1 | MOD0 | Data Format |
|---|---|---|---|
| 0 | 0 | 0 | Start + 7 bit data + 1 stop |
| 0 | 0 | 1 | Start + 7 bit date + 2 Stop |
| 0 | 1 | 0 | Start + 7 bit data + parity + 1 stop |
| 0 | 1 | 1 | Start + 7 bit data + parity + 2 stop |
| 1 | 0 | 0 | Start + 8 bit data + 1 stop |
| 1 | 0 | 1 | Start + 8 bit data + 2 stop |
| 1 | 1 | 0 | Start + 8 bit data + parity + 1 stop |
| 1 | 1 | 1 | Start + 8 bit date + parity + 2 stop |

### ASCI Control Register B0, 1 (CNTLB0, 1)

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

| Bit Position | Bit/Field | R/W | Value | Description |
|---|---|---|---|---|
| 0 | Send Break | R/W | 0<br>1 | Normal Xmit<br>Drive TXA Low |

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

ASCI1 Extension Control Register (I/O Address: 13H) (Z8S180/L180-Class Processors Only)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit/Field | RDRF Int Inhibit | Reserved | | X1 Bit Clk ASCI1 | BRG1 Mode | Break Feature Enable | Break Detect (RO) | Send Break |
| R/W | R/W | ? | | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | | 0 | 0 | 0 | 0 | 0 |

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

| Bit Position | Bit/Field | R/W | Value | Description |
|---|---|---|---|---|
| 7 | RDRF Interrupt Inhibit | R/W | 0<br>1 | RDRF Interrupt Inhibit On<br>RDRF Interrupt Inhibit Off |
| 6–5 | Reserved | ? | 0 | Reserved. Must be 0 |
| 4 | X1 Bit Clk ASCI1 | R/W | 0<br>1 | CKA1 /16 or /64<br>CKA1 is bit clock |
| 3 | BRG1 Mode | R/W | 0<br>1 | As S180<br>Enable 16-bit BRG counter |

### ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

### ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

### ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

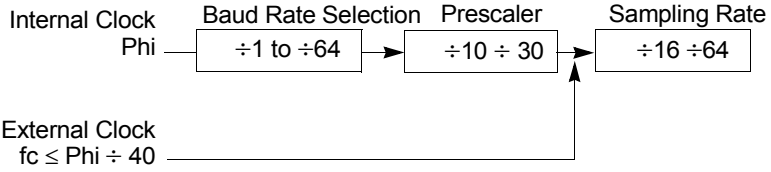


**Figure 56. ASCI Clock**

c. Poll the RE bit in CNTR until RE = 0.

d. Read the receive data from TRDR.

e. Repeat steps 2 to 4 for each receive data byte.

- Receive–Interrupts

a. Poll the RE bit in CNTR until RE is 0.

b. Set the RE and EIE bits in CNTR to 1.

c. When the receive interrupt occurs read the receive data from TRDR.

d. Set the RE bit in CNTR to 1.

e. Repeat steps 3 and 4 for each receive data byte.

### CSI/O Operation Timing Notes

- Transmitter clocking and receiver sampling timings are different from internal and external clocking modes. Figure 59 to Figure 62 illustrate CSI/O Transmit/Receive Timing.
- The transmitter and receiver is disabled TE and RE = 0) when initializing or changing the baud rate.

### CSI/O Operation Notes

- Disable the transmitter and receiver (TE and RE = 0) before initializing or changing the baud rate. When changing the baud rate after completion of transmission or reception, a delay of at least one bit time is required before baud rate modification.
- When RE or TE is cleared to 0 by software, a corresponding receive or transmit operation is immediately terminated. Normally, TE or RE is only cleared to 0 when EF is 1.
- Simultaneous transmission and reception is not possible. Thus, TE and RE are not both 1 at the same time.

**Table 23. Timer Output Control**

| TOC1 | TOC0 | OUTPUT | |
|---|---|---|---|
| 0 | 0 | Inhibited | (A18/TOUT pin is selected as an address output function.) |
| 0 | 1 | Toggled | |
| 1 | 0 | 0 | A18/TOUT pin is selected as a PRT1 output function! |
| 1 | 1 | 1 | |

Figure 64 illustrates timer initialization, count down, and reload timing. Figure 65 depicts timer output (A18/TOUT) timing.

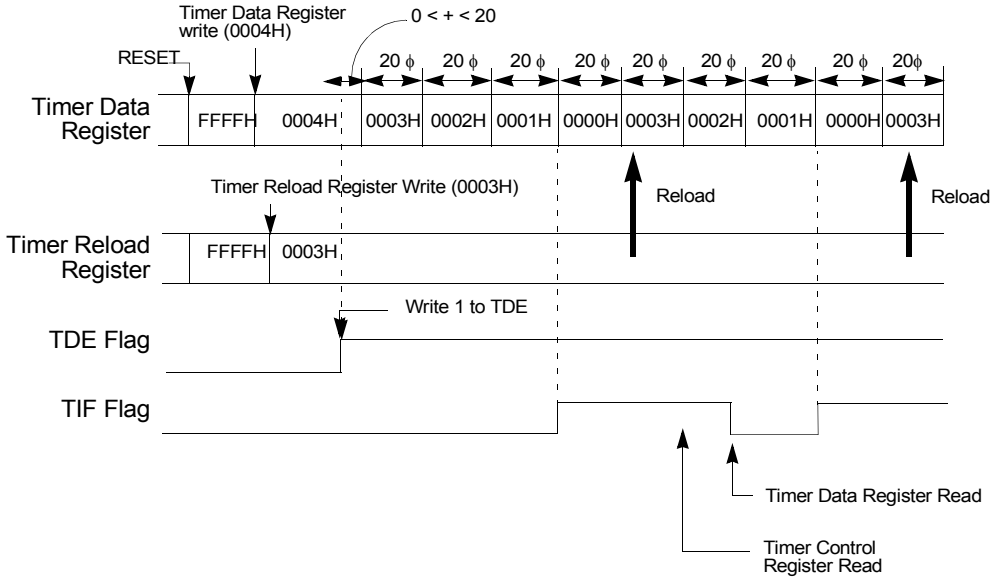


**Figure 64. Timer Initialization, Count Down, and Reload Timing Diagram**

These devices require connection with the Z8X180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z8X180 clock rate. Table 24, and Figure 67 through Figure 70 define E clock output timing.

Wait States are inserted in Op Code fetch, memory read/write, and I/O read/write cycles which extend the duration of E clock output High. During I/O read/write cycles with no Wait States (only occurs during on-chip I/O register accesses), E does not go High.

**Table 24. E Clock Timing in Each Condition**

| **Condition** | **Duration of E Clock Output High** | |
|---|---|---|
| Op Code Fetch Cycle<br>Memory Read/Write Cycle | T2 rise - T3 fall | (1.5 Phi + nw x Phi) |
| I/O read Cycle | 1st Tw rise - T3 fall | (0.5Phi + nw x Phi) |
| I/O Write Cycle | 1st Tw rise - T3 rise | $In_w$ x Phi) |
| $\overline{NMI}$ Acknowledge 1st MC | T2 rise - T3 fall | (1.5 Phi) |
| $\overline{INT0}$ Acknowledge 1st MC | 1st Tw rise - T3 fall | (0.50 + nw x Phi) |
| BUS RELEASE mode<br>SLEEP mode<br>SYSTEM STOP mode | Phi fall - Phi fall | (2 Phi or 1 Phi) |
| Note: nw = the number of Wait States; MC: Machine Cycle | | |

## IO (I/O)

IO addressing mode is used only by I/O instructions. This mode specifies I/O address ($\overline{\text{IORQ}}$ is 0) and outputs them as follows.

1. An operand is output to A0–A7. The contents of accumulator is output to A8–A15.
2. The contents of Register B is output to A0–A7. The contents of Register C is output to A8–A15.
3. An operand is output to A0–A7. 00H is output to A8–A15 (useful for internal I/O register access)
4. The contents of Register C is output to A0–A7. 00H is output to A8–A15 (useful for internal I/O register access).

# DATA MANIPULATION INSTRUCTIONS

**Table 38. Arithmetic and Logical Instructions (8-bit)**

| Operation Name | Mnemonics | Op Code | Addressing | | | | | | | Bytes | States | Operation | Flags | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Immed | Ext | Ind | Reg | Regl | Imp | Rel | | | | 7 | 6 | 4 | 2 | 1 | 0 |
| | | | | | | | | | | | | | S | Z | H | P/V | N | C |
| ADD | ADD A,g | 10 000 g | | | | S | | D | | 1 | 4 | Ar + gr→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADD A, (HL) | 10 000 110 | | | | | S | D | | 1 | 6 | Ar + $(HL)_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADD A, m | 11 000 110 | S | | | | | D | | 2 | 6 | Ar + m→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | <m> | | | | | | | | | | | | | | | | |
| | ADD A,(IX + d) | 11 011 101 | | | S | | | D | | 3 | 14 | Ar + $(IX + d)_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 000 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| | ADD A,(IY + d) | 11 111 101 | | | S | | | D | | 3 | 14 | Ar + $(IY + d))_M$→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 000 I10 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| ADC | ADC A,g | 10 001 g | | | | S | | D | | 1 | 4 | Ar + gr + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADC A,(HL) | 10 001 110 | | | | | S | D | | 1 | 6 | Ar + $(HL)_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | ADC A,m | 11 001 110 | S | | | | | D | | 2 | 6 | Ar + m + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | <m> | | | | | | | | | | | | | | | | |
| | ADC A,(IX + d) | 11 011 101 | | | S | | | D | | 3 | 14 | Ar + $(IX + d))_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 001 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |
| | ADC A,(IY + d) | 11 111 101 | | | S | | | D | | 3 | 14 | Ar + $(IY + d))_M$ + c→Ar | ↑ | ↑ | ↑ | V | R | ↑ |
| | | 10 001 110 | | | | | | | | | | | | | | | | |
| | | <d> | | | | | | | | | | | | | | | | |

**Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)**

| Instruction | Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LD (mn),A | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 1st operand Address | n | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC3 | T1T2T3 | 2nd operand Address | m | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC4 | Ti | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | MC5 | T1T2T3 | mn | A | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| LD A,I<br>LD A,R *4<br>LD I,A<br>LD R,A | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| LD ww, mn | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 1st operand Address | n | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC3 | T1T2T3 | 2nd operand Address | m | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| LD IX,mn<br>LD IY,mn | MC1 | T1T2T3 | 1st Op Code Address | 1st Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | MC2 | T1T2T3 | 2nd Op Code Address | 2nd Op Code | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | MC3 | T1T2T3 | 1st operand Address | n | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC4 | T1T2T3 | 2nd operand Address | m | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

*4 In the case of R1 and Z MASK, interrupt request is not sampled.

**Table 52. Interrupts (Continued)**

| Instruction | Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{INT0}$ Mode 2 | MC1 | T1T2TW TWT3 | Next Op Code Address (PC) | Vector | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| | MC2 | Ti | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | MC3 | T1T2T3 | SP-1 | PCH | 1 | 0 | 0 | 1 | 1 | | 1 |
| | MC4 | T1T2T3 | SP-2 | PCL | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | MC5 | T1T2T3 | I, Vector | DATA | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC6 | T1T2T3 T1T2,TW | I, Vector+1 | DATA | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| $\overline{INT1}$ $\overline{INT2}$ Internal Interrupts | MC1 | T1T2,TW TWT3 | Next Op Code Address (PC) | | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | MC2 | Ti | * | Z | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | MC3 | T1T2T3 | SP-1 | PCH | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | MC4 | T1T2T3 | SP-2 | PCL | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| | MC5 | T1T2T3 | I, Vector | DATA | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | MC6 | T1T2T3 | I, Vector+1 | DATA | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Table 55. Pin Outputs in Each Operating Mode (Continued)**

| Mode | | $\overline{M1}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{RFSH}$ | $\overline{HALT}$ | $\overline{BUSACK}$ | ST | Address BUS | Data BUS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Internal DMA | Memory Read | 1 | 0 | 1 | 0 | 1 | 1 | * | 1 | 0 | A | IN |
| | Memory Write | 1 | 0 | 1 | 1 | 0 | 1 | * | 1 | 0 | A | OUT |
| | I/O Read | 1 | 1 | 0 | 0 | 1 | 1 | * | 1 | 0 | A | IN |
| | I/O Write | 1 | 1 | 0 | 1 | 0 | 1 | * | 1 | 0 | A | OUT |
| RESET | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Z | IN |

- 1 : High
- 0 : Low
- A : Programmable
- Z : High Impedance
- IN : Input
- OUT : Output
- * : Invalid

## PIN STATUS

Tables 56 describes the status of each ping during RESET and LOW POWER OPERATION modes.

**Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)**

| Symbol | Pin Function | Pin Status in Each Operation Mode | | | |
|---|---|---|---|---|---|
| | | RESET | SLEEP | IOSTOP | SYSTEM STOP |
| $\overline{\text{MREQ}}$ | — | 1 | 1 | OUT | 1 |
| E | — | 0 | E Clock Output | ← | ← |
| $\overline{\text{M1}}$ | — | 1 | 1 | OUT | 1 |
| $\overline{\text{WR}}$ | — | 1 | 1 | OUT | 1 |
| $\overline{\text{RD}}$ | — | 1 | 1 | OUT | 1 |
| Phi | — | Phi Clock Output | ← | ← | ← |

- 1: HIGH 0: LOW A: Programmable Z: High Impedance
- IN (A): Input (Active) IN (N): Input (Not active) OUT: Output
- H: Holds the previous state
- ←: same as the left