Zilog - Z8018010FSC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010fsc

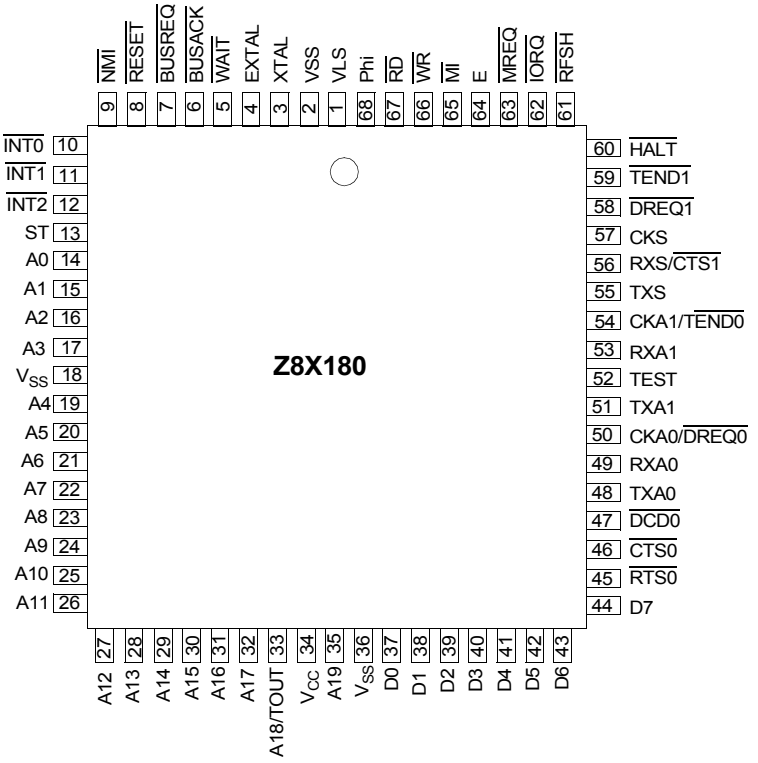

Figure 2. 68-Pin PLCC

$\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, during this cycle neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become Active.

$\overline{\text{IORQ}}$. *I/O Request (Output, Active Low, 3-state).* $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

$\overline{\text{M1}}$. *Machine Cycle 1 (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the Op Code fetch cycle of an instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

$\overline{\text{MREQ}}$. *Memory Request (Output, Active Low, 3-state).* $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the $\overline{\text{ME}}$ signal of the Z64180.

$\overline{\text{NMI}}$. *Non-maskable Interrupt (Input, negative edge triggered).* $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location `0066H`.

$\overline{\text{RD}}$. *Read (Output active Low, 3-state).* $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device must use this signal to gate data onto the CPU data bus.

$\overline{\text{RFSH}}$. *Refresh (Output, Active Low).* Together with $\overline{\text{MREQ}}$, $\overline{\text{RFSH}}$ indicates that the current CPU machine cycle and the contents of the address bus must be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7–A0) contain the refresh address.

This signal is analogous to the $\overline{\text{REF}}$ signal of the Z64180.

$\overline{\text{RTS0}}$. *Request to Send 0 (Output, Active Low).* This output is a programmable modem control signal for ASCI channel 0.

RXA0, RXA1. *Receive Data 0 and 1 (Inputs, Active High).* These signals are the receive data to the ASCI channels.

RXS. *Clocked Serial Receive Data (Input, Active High).* This line is the receiver data for the CSIO channel. RXS is multiplexed with the $\overline{\text{CTS1}}$ signal for ASCI channel 1.

ST. *Status (Output, Active High).* This signal is used with the $\overline{\text{M1}}$ and $\overline{\text{HALT}}$ output to decode the status of the CPU machine cycle. Table 1 provides status summary.

Table 1. Status Summary

ST	$\overline{\text{HALT}}$	$\overline{\text{M1}}$	Operation
0	1	0	CPU operation (1st Op Code fetch)
1	1	0	CPU operation (2nd Op Code and 3rd Op Code fetch)
1	1	1	CPU operation (MC[2] except for Op Code fetch)
0	X[1]	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (including SYSTEM STOP mode)

1. X = Don't care
2. MC = Machine cycle

$\overline{\text{TEND0}}$, $\overline{\text{TEND1}}$. *Transfer End 0 and 1 (Outputs, Active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND0}}$ in multiplexed with CKA1.

TEST. *Test (Output, not on DIP version).* This pin is for test and must be left open.

OPERATION MODES

The Z8X180 can be configured to operate like the Hitachi HD64180. This functionality is accomplished by allowing user control over the $\overline{M1}$, $\overline{IORQ}$, $\overline{WR}$, and $\overline{RD}$ signals. The Operation Mode Control Register (OMCR), illustrated in Figure 5, determines the $\overline{M1}$ options, the timing of the $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ signals, and the RETI operation.

Operation Mode Control Register

Bit	7	6	5	4	0
Bit/Field	M1E	$\overline{M1TE}$	IOC	Reserved	
R/W	R/W	W	R/W	–	
Reset	1	1	1	–	

Note: R = Read W = Write X = Indeterminate? = Not Applicable

Figure 5. Operation Mode Control Register

M1E (M1_Enable): This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E is 1, the $\overline{M1}$ output is asserted Low during the Op Code fetch cycle, the INT0 acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge. This action also causes the M1 signal to be Active during both fetches of the RETI instruction sequence, and may cause corruption of the external interrupt daisy chain. Therefore, this bit must be 0 for the Z8X180. When M1E is 0 the $\overline{M1}$ output is normally inactive and asserted Low only during the refetch of the RETI instruction sequence and the $\overline{INT0}$ acknowledge cycle (Figure 6).

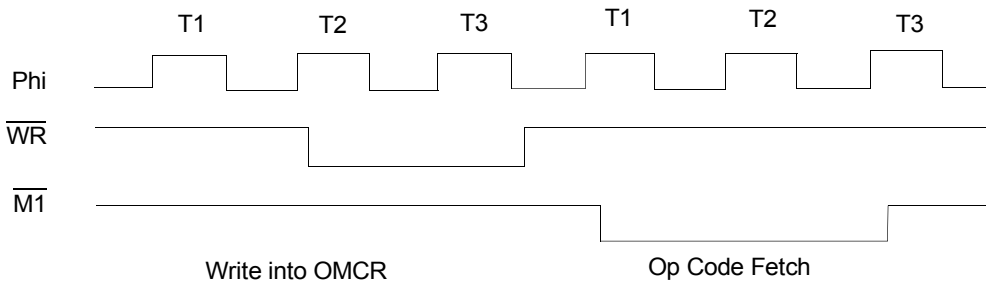

Figure 6. M1 Temporary Enable Timing

$\overline{\text{M1TE}}$ ($\overline{\text{M1}}$ Temporary Enable): This bit controls the temporary assertion of the $\overline{\text{M1}}$ signal. It is always read back as a 1 and is set to 1 during RESET. This function is used to *arm* the internal interrupt structure of the Z80PIO. When a control word is written to the Z80PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{\text{M1}}$ signal. When $\overline{\text{M1TE}}$ is 1, there is no change in the operation of the $\overline{\text{M1}}$ signal and M1E controls its function. When $\overline{\text{M1TE}}$ is 0, the $\overline{\text{M1}}$ output is asserted during the next Op Code fetch cycle regardless of the state programmed into the M1E bit. This situation is only momentary (one time) and the user need not reprogram a 1 to disable the function (See Figure 7).

$\overline{\text{IOC}}$: This bit controls the timing of the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals. $\overline{\text{IOC}}$ is set to 1 by RESET.

When $\overline{\text{IOC}}$ is 1, the $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals function the same as the HD64180.

Also, the $\overline{\text{WAIT}}$ input is ignored during RESET. For example, if RESET is detected while the Z8X180 is in a Wait State (TW), the Wait Stated cycle in progress is aborted, and the RESET sequence initiated. Thus, $\overline{\text{RESET}}$ has higher priority than $\overline{\text{WAIT}}$.

HALT and Low Power Operation Modes (Z80180-Class Processors Only)

The Z80180 can operate in two different modes:

- HALT mode
- IOSTOP mode

and two low-power operation modes:

- SLEEP
- SYSTEM STOP

In all operating modes, the basic CPU clock (XTAL, EXTAL) must remain active.

HALT Mode

HALT mode is entered by execution of the HALT instruction (Op Code 76H) and has the following characteristics:

- The internal CPU clock remains active
- All internal and external interrupts can be received
- Bus exchange ($\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$) can occur
- Dynamic RAM refresh cycle ($\overline{\text{RFSH}}$) insertion continues at the programmed interval
- I/O operations (ASCI, CSI/O and PRT) continue
- The DMAC can operate

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
DMA	DMA Source Address Register Ch 0L	SAR0L	XX100000	20H	93
	DMA Source Address Register Ch 0H	SAR0H	XX100001	21H	93
	DMA Source Address Register Ch 0B	SAR0B	XX100010	22H	93
	DMA Destination Address Register Ch 0L	DAR0L	XX100011	23H	94
	DMA Destination Address Register Ch 0H	DAR0H	XX100100	24H	94
	DMA Destination Address Register Ch 0B	DAR0B	XX100101	25H	94
	DMA Byte Count Register Ch 0L	BCR0L	XX100110	26H	94
	DMA Byte Count Register Ch 0H	BCR0H	XX100111	27H	94
	DMA Memory Address Register Ch 1L	MAR1L	XX101000	28H	94
	DMA Memory Address Register Ch 1H	MAR1H	XX101001	29H	94
	DMA Memory Address Register Ch 1B	MAR1B	XX101010	2AH	94
	DMA I/O Address Register Ch 1L	IAR1L	XX101011	2BH	102
	DMA I/O Address Register Ch 1H	IAR1H	XX101100	2CH	102
	DMA I/O Address Register Ch 1	IAR1B	XX101101	2DH	94
	DMA Byte Count Register Ch 1L	BCR1L	XX101110	2EH	94
	DMA Byte Count Register Ch 1H	BCR1H	XX101111	2FH	94
	DMA Status Register	DSTAT	XX110000	30H	95
	DMA Mode Register	DMODE	XX110001	31H	97
	DMA/WAIT Control Register	DCNTL	XX110010	32H	101

Bit Position	Bit/Field	R/W	Value	Description
0	DME	R		**DMA Main Enable** — A DMA operation is only enabled when its DE bit DE0 for channel 0, DE1 for channel 1) and the DME bit are set to 1. When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE0 and/or DE1 must be written with 1 (even if the contents are already 1). This action automatically sets DME to 1, allowing DMA operations to continue. DME cannot be directly written. It is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1.DME is cleared to 0 during RESET.

DMA Mode Register (DMODE)

DMODE is used to set the addressing and transfer mode for channel 0.

DMA Mode Register (DMODE: 31H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	?		DM1	DM0	SM1	SM0	MMOD	?
R/W	?		R/W	R/W	R/W	R/W	R/W	?
Reset	?		0	0	0	0	0	?

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
5–4	DM1:0	R/W		**Destination Mode Channel 0** — Specifies whether the destination for channel 0 transfers is memory, I/O or memory mapped I/O and the corresponding address modifier. Reference Table 12.

ASCI Receive Shift Register 0,1(RSR0, 1)

This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. The RSR is not program-accessible.

ASCI Receive Data Register 0,1 (RDR0, 1: I/O Address = 08H, 09H)

When a complete incoming data byte is assembled in RSR, it is automatically transferred to the RDR if RDR is empty. The next incoming data byte can be shifted into RSR while RDR contains the previous received data byte. Thus, the ASCI receiver on Z80180 is double-buffered.

ASCI Receive Data Register Ch. 0 (RDR0: 08H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	ASCI Receive Channel 0							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

ASCI Receive Data Register Ch. 1 (RDR1: 09H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	ASCI Receive Channel 1							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

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On the Z8S180 and Z8L180-class processors are quadruple buffered. The ASCI Receive Data Register is a read-only register. However, if RDRF =

Bit Position	Bit/Field	R/W	Value	Description
2–0	MOD2–0	R/W		**ASCI Data Format Mode 2, 1, 0** — These bits program the ASCI data format as follows. **MOD2** 0: 7 bit data 1: 8 bit data **MOD1** 0: No parity 1: Parity enabled **MOD0** 0: 1 stop bit 1: 2 stop bits The data formats available based on all combinations of MOD2, MOD1 and MOD0 are described in Table 17.

ASCI1 Time Constant Low Register (I/O Address: 1CH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

ASCI1 Time Constant High Register (I/O Address: 1DH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Modem Control Signals

ASCI channel 0 has $\overline{\text{CTS0}}$, $\overline{\text{DCD0}}$ and $\overline{\text{RTS0}}$ external modem control signals. ASCI channel 1 has a $\overline{\text{CTS1}}$ modem control signal which is multiplexed with Clocked Serial Receive Data (RXS).

$\overline{\text{CTS0}}$: Clear to Send 0 (Input)

The $\overline{\text{CTS0}}$ input allows external control (start/stop) of ASCI channel 0 transmit operations. When $\overline{\text{CTS0}}$ is High, the channel 0 TDRE bit is held at 0 whether or not the TDR0 (Transmit Data Register) is full or empty. When $\overline{\text{CTS0}}$ is Low, TDRE reflects the state of TDR0. The actual transmit operation is not disabled by CT High, only TDRE is inhibited:

$\overline{\text{DCD0}}$: Data Carrier Detect 0 (Input)

The $\overline{\text{DCD0}}$ input allows external control (start/stop) of ASCI channel 0 receive operations. When DCD0 is High, the channel 0 RDRF bit is held at 0 whether or not the RDR0, (Receive Data Register) is full or empty.

2^ss depends on the three least significant bits of the CNTLB register, as described in Table 21.

Table 21. 2^ss Values

ss2	ss1	ss0	2^ss
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	External Clock from CKA0

The ASCIs require a 50% duty cycle when CKA is used as an input. Minimum High and Low times on CKA0 are typical of most CMOS devices.

RDRF is set, and if enabled, an Rx Interrupt or DMA REquest is generated when the receiver transfers a character from the Rx Shift Register to the RX FIFO. The FIFO provides a margin against overruns. When the is more than one character in the FIFO, and software or a DMA channel reads a character, RDRF either remains set or is cleared and then immediately set again. For example, if a receive interrupt service routine does not real all the characters in the RxFIFO, RDRF and the interrupt request remain asserted.

The Rx DMA request is disabled when any of the error flags PE or FE or OVRN are set, so that software can identify with which character the problem is associated.

If Bit 7, RDRF Interrupt Inhibit, is set to 1, the ASCI does not request a Receive interrupt when its RDRF flag is 1. Set this bit when programming a DMA channel to handle the receive data from an ASCI. The other

Figure 74 depicts CPU register configurations.

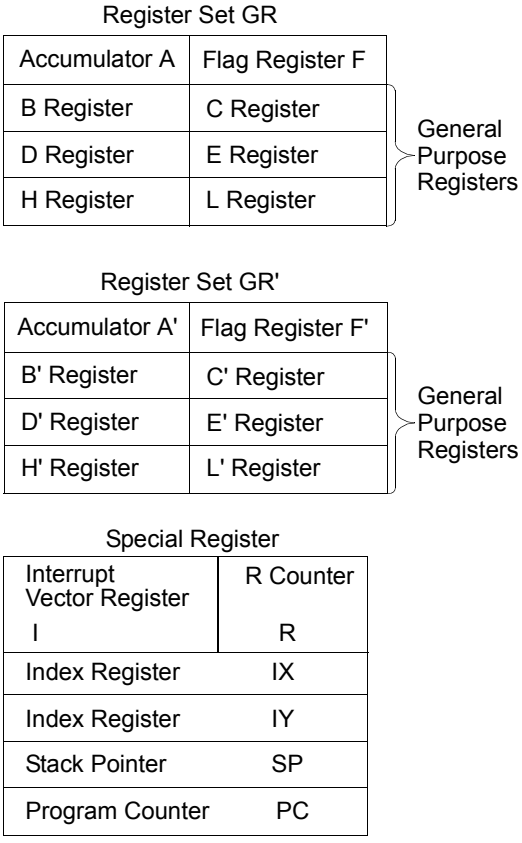

Figure 74. CPU Register Configurations

Accumulator (A, A')

The Accumulator (A) is the primary register used for many arithmetic, logical, and I/O instructions.

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8-bit signed displacement specified in the instruction. Refer to Figure 77

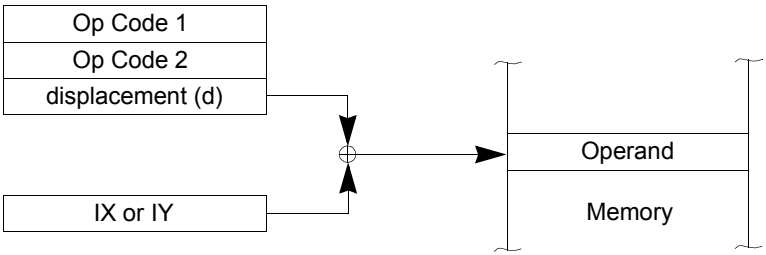

Figure 77. Indexed Addressing

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction, as depicted in Figure 78.

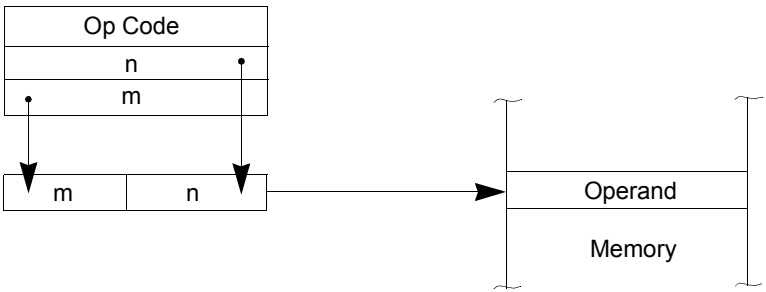

Figure 78. Extended Addressing

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5 t_{CY} C +75	—	75 t_{CYC} +60	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to PHI Fall	40	—	25	—	ns
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{\text{RESET}}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{\text{RESET}}$ Fall Time	—	50	—	50	ms

MNEMONICS	Bytes	Machine Cycles	States
LD (DE),A	1	3	7
LD ww,mn	3	3	9
LD ww,(mn)	4	6	18
LDDR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$
LD (HL),m	2	3	9
LD HL,(mn)	3	5	15
LD (HL),g	1	3	7
LDI	2	4	12
LDI,A	2	2	6
LDIR	2	6	14 (If $BC_R \neq 0$)
	2	4	12 (If $BC_R = 0$)
LD IX,mn	4	4	12
LID IX,(mn)	4	6	18
LD (IX+d),m	4	5	15
LD (IX+ d),g	3	7	15
LD IY,mn	4	4	12
LD IY,(mn)	4	6	18
LD (IY+d),m	4	5	15
LD (IY+d),g	3	7	15
LD (mn),A	3	5	13
LD (mn),ww	4	7	19
LD (mn),HL	3	6	16
LD (mn),IX	4	7	19
LD (mn),IY	4	7	19
LD R,A	2	2	6
LD g,(HL)	1	2	6
LD g,(IX+d)	3	6	14
LD g,(IY+d)	3	6	14
LD g,m	2	2	6

MNEMONICS	Bytes	Machine Cycles	States
LD g,g'	1	2	4
LD SP,HL	1	2	4
LD SP,IX	2	3	7
LD SP,IY	2	3	7
MLT ww"	2	13	17
NEG	2	2	6
NOP	1	1	3
OR (HL)	1	2	6
OR (IX+d)	3	6	14
OR (IY+d)	3	6	14
OR m	2	2	6
OR g	1	2	4
OTDM**	2	6	14
OTDMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTDR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0
OTIM**	2	6	14
OTIMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTIR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0)
OUTD	2	4	12
OUTI	2	4	12
OUT (m),A	2	4	10
OUT (C),g	2	4	10
OUT0 (m),g **	3	5	13
POP IX	2	4	12
POP IY	2	4	12
POP zz	1	3	9

Table 50. 2nd Op Code Map Instruction Format: ED XX

						ww (L0 = ALL)												
						BC	DE	HL	SP									
		G (L0 = 0~7)																
		B	D	H		B	D	H										
HI / LO		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	IN0 g, (m)				IN g, (C)						LDI	LDIR					0
0001	1	OUT0 (m),g				OUT (C),g						CPI	CPIR					1
0010	2					SBC HL, ww						INI	INIR					2
0011	3					LD (mn), ww				OTIM	OTIM R	OUTI	OTIR					3
0100	4	TST g			TST (HL)	NEG		TST m	TSTIO m									4
0101	5					RETN												5
0110	6					IM 0	IM 1		SLP									6
0111	7					LD I,A	LD A,I	RRD										7
1000	8	IN0 g, (m)				IN g, (C)						LDD	LDDR					8
1001	9	OUT0 (m), g				OUT (C) , g						CPD	CPDR					9
1010	A					ADC HL,ww						IND	INDR					A
1011	B					LD ww, (mn)				OTD M	OTD MR	OUTD	OTDR					B
1100	C	TST g				MLT ww												C
1101	D					RETI												D
1110	E						IM 2											E
1111	F					LDR, A	LD A,R	RLD										F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
		C	E	L	A	C	E	L	A									
		g (L0 = 8~F)																

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (mn),HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	mn	L	1	0	0	1	1	1	1
	MC6	T1T2T3	mn+1	H	1	0	0	1	1	1	1
LD (mn),ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	mn	wwL	1	0	0	1	1	1	1
	MC7	T1T2T3	mn+1	wwH	1	0	0	1	1	1	1