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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010fsg

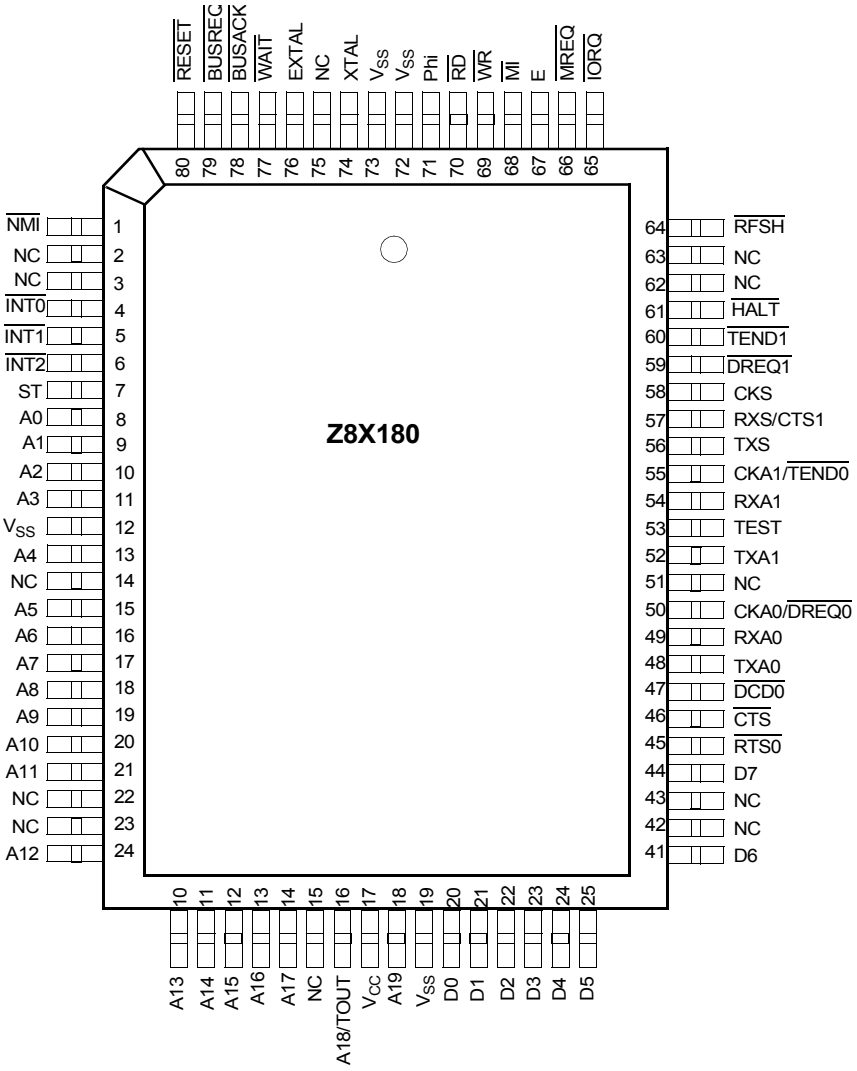


Figure 3. 80-Pin QFP

- Data Bus, 3-state

SLEEP mode is exited in one of two ways as described below.

- RESET Exit from SLEEP mode. If the $\overline{\text{RESET}}$ input is held Low for at least six clock cycles, it exits SLEEP mode and begins the normal RESET sequence with execution starting at address (logical and physical) 00000H.

- Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external ($\overline{\text{NMI}}$, $\overline{\text{INT0}}$, $\overline{\text{INT2}}$) or internal (ASCI, CSI/O, PRT) interrupt.

In case of $\overline{\text{NMI}}$, SLEEP mode is exited and the CPU begins the normal $\overline{\text{NMI}}$ interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag IEF1 and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP mode.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF1). If interrupts are globally enabled (IEF1 is 1) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled (IEF1 is 0) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. This feature provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 21 depicts SLEEP timing.

To avoid address conflicts with external I/O, the Z8X180 internal I/O addresses can be relocated on 64-byte boundaries within the bottom 256 bytes of the 64KB I/O address space.

I/O Control Register (ICR)

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode.

I/O Control Register (ICR: 3FH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	IOA7	IOA6	IOSTP	—	—	—	—	—
R/W	R/W	R/W	R/W					
Reset	0	0	0					

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–6	IOA7:6	R/W		IOA7 and IOA6 relocate internal I/O as depicted in Figure . The high-order 8 bits of 16-bit internal I/O addresses are always 0. IOA7 and IOA6 are cleared to 0 during RESET.
5	IOSTP	R/W		IOSTOP mode is enabled when IOSTP is set to 1. Normal. I/O operation resumes when IOSTP is reset to 0.

Table 6. I/O Address Map for Z80180-Class Processors Only (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
Timer	Data Register Ch 0 L	TMDR0L	XX001100	0CH	159
	Data Register Ch 0 H	TMDR0H	XX001101	0DH	159
	Reload Register Ch 0 L	RLDR0L	XX001110	0EH	159
	Reload Register Ch 0 H	RLDR0H	XX001111	0FH	159
	Timer Control Register	TCR	XX010000	10H	161
	Reserved		XX010001	11H	
			↕	↕	
			XX010011	13H	
	Data Register Ch 1 L	TMDR1L	XX010100	14H	160
	Data Register Ch 1 H	TMDR1H	XX010101	15H	160
	Reload Register Ch 1 L	RLDR1L	XX010110	16H	159
	Reload Register Ch 1 H	RLDR1H	XX010111	17H	159
Others	Free Running Counter	FRC	XX011000	18H	172
	Reserved		XX011001	19H	
			↕	↕	
			XX011111	1FH	

Whether address translation (Figure 26) takes place depends on the type of CPU cycle as follows.

- Memory Cycles

  Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch, and software interrupt restarts.

- I/O Cycles

  The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The four high-order bits (A16–A19) of the physical address are always `0` during I/O cycles.

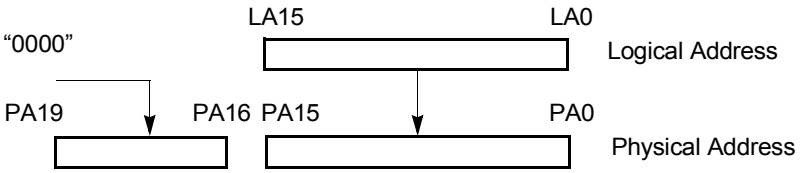


Figure 26. I/O Address Translation

- DMA Cycles

  When the Z8X180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The 20-bit source and destination registers in the DMAC are directly output on the physical address bus (A0–A19).

MMU Registers

Three MMU registers are used to program a specific configuration of logical and physical memory.

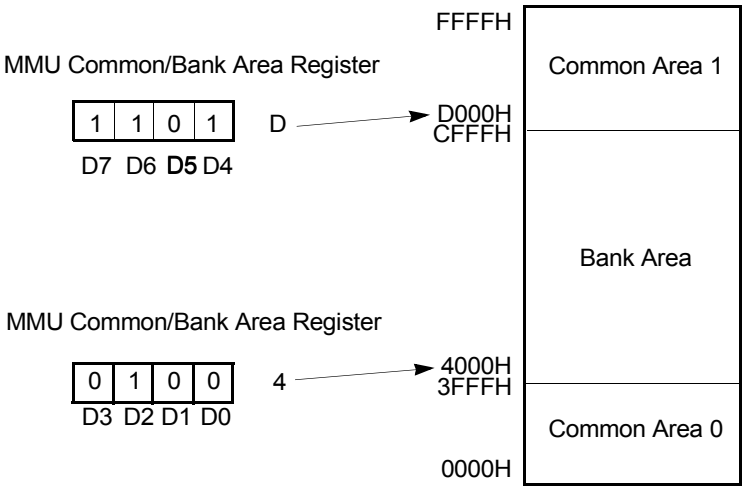


Figure 28. Logical Space Configuration (Example)

Z8X180. Figure 43 illustrates the INT1, INT2 and internal interrupts timing.

Table 10. RETI Control Signal States

Machine Cycle	States	Address	Data	$\overline{MI}$							
				$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1E=1}$	$\overline{M1E=0}$	$\overline{HALT}$	ST
1	T1-T3	1st Op Code	EDH	0	1	0	1	0	1	1	0
2	TI-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
3	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
4	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
5	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
6	T1-T3	1st Op Code	EDH	0	1	0	1	0	0	1	1
7	T1	Don't Care	3-state	1	1	1	1	1	1	1	1
8	T1-T3	2nd Op Code	4DH	0	1	0	1	0	1	1	1
9	T1-T3	SP	data	0	1	0	1	1	1	1	1
10	T1-T3	SP+1	data	0	1	0	1	1	1	1	1

IOC affects the IORQ/RD signals. M1E affects the assertion of M1. One state also reflects a 1 while the other reflects a 0

- $\overline{\text{DREQ}}$ Input

  Level- and edge-sense DREQ input detection are selectable.

  $\overline{\text{TEND}}$ Output Used to indicate DMA completion to external devices.

- Transfer Rate

  Each byte transfer occurs every 6 clock cycles. Wait States can be inserted in DMA cycles for slow memory or I/O devices. At the system clock (ϕ) = 6 MHz, the DMA transfer rate is as high as 1.0 megabytes/second (no Wait States).

There is an additional feature disc for DMA interrupt request by DMA END. Each channel has the following additional specific capabilities:

Channel 0

- Memory to memory
- Memory to I/O
- Memory to memory mapped I/O transfers.
- Memory address increment, decrement, no-change
- Burst or cycle steal memory to/from memory transfers
- DMA to/from both ASCI channels
- Higher priority than DMAC channel 1

Channel 1

- Memory to/from I/O transfer
- Memory address increment, decrement

DMAC Registers

Each channel of the DMAC (channel 0, 1) contains three registers specifically associated with that channel.

ASCI Control Register B 0 (CNTLB0: 02H)
ASCI Control Register B 1 (CNTLB1: 03H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MPBT	MP	$\overline{\text{CTS}}$/PS	PE0	DR	SS2	SS1	SS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	X	0	0	0	0	1	1	1

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	MPBT	R/W		**Multiprocessor Bit Transmit** — When multiprocessor communication format is selected (MP bit is 1), MPBT is used to specify the MPB data bit for transmission. If MPBT is 1, then MPB = 1 is transmitted. If MPBT is 0, then MPBT = 0 is transmitted. MPBT state is undefined during and after RESET.
6	MP	R/W		**Multiprocessor Mode** — When MP is set to 1, the data format is configured for multiprocessor mode based on the MOD2 (number of data bits) and MOD0 (number of stop bits) bits in CNTLA. The format is as follows. Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits Multiprocessor (MP = 1) format has no provision for parity. If MP is 0, the data format is based on MOD0 MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

Miscellaneous

Free Running Counter (I/O Address = 18H)

If data is written into the free running counter, the interval of DRAM refresh cycle and baud rates for the ASCI and CSI/O are not guaranteed.

In IOSTOP mode, the free running counter continues counting down. It is initialized to FFH during RESET.

Free Running counter (FRC: 18H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Counting Data							
R/W	R							
Reset	?							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Table 28. Z80180 DC Characteristics (Continued)

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
	Power Dissipation* (SYSTEM STOP mode)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	3.8 5 6.3	12.5 15.0 17.5	mA mA mA
CP	Pin Capacitance	VIN = 0V, f = 1MHz TA = 25°C	–	–	12	pF
Notes: * VIN min = V_{CC} –1.0V. VIL max = 0.8V (All output terminals are a no load.) V_{CC} = 5.0V						

Z8S180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.

Table 29. Z8S180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIH3	Input High Voltage CKS, CKA0, CKA1		2.4		V_{DD} + 0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8	V

AC Characteristics

This section describes the AC characteristics of the Z8X180 family and absolute maximum rating for these products.

AC CHARACTERISTICS—Z8S180

Table 31. Z8S180 AC Characteristics V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock “H” Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock “L” Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to $\overline{MREQ}$ Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High	5	—	5	—	ns

Timing Diagrams

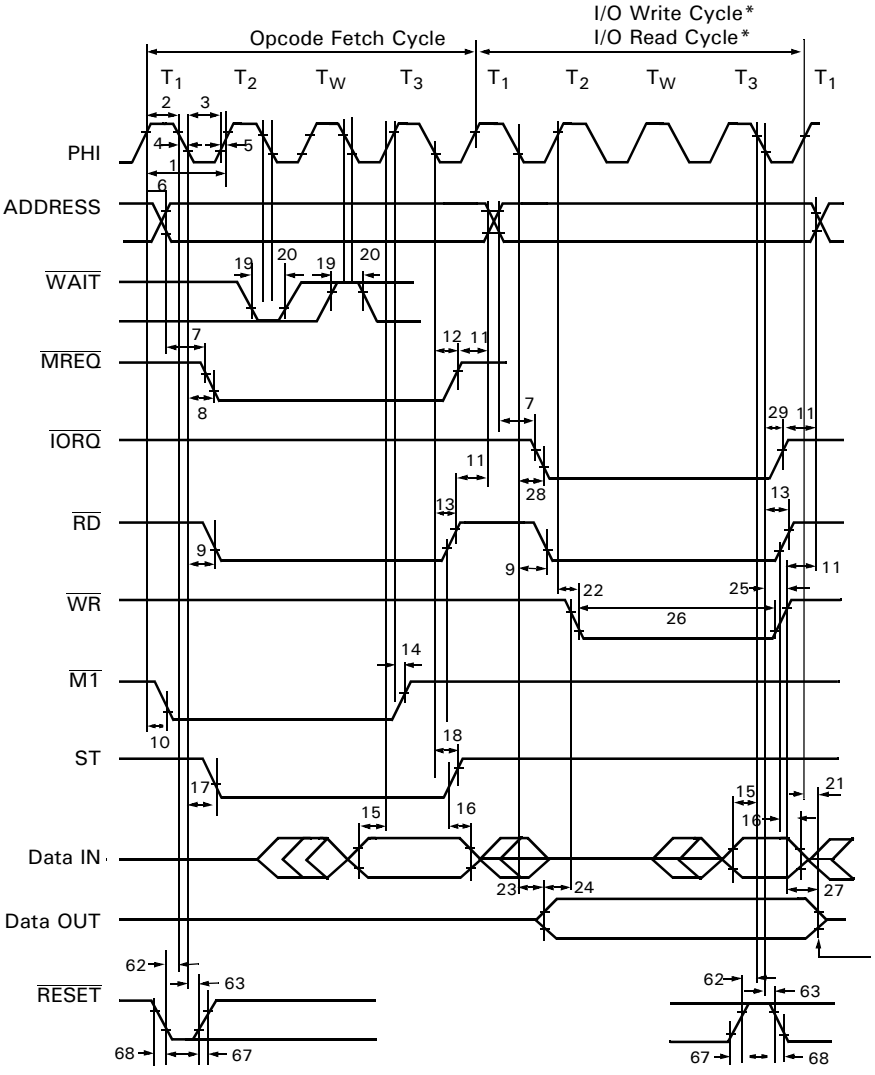


Figure 81. AC Timing Diagram 1

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
		11 001 011																
		<d>																
		00 001 110																
	RRD	11 101 101						S/D		2	16		↑	↑	R	P	R	•
		01 100 111										Ar b7 b0						
	SLA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 100 g																
	SLA (HL)	11 001 011					S/D			2	13	(HL)M b7 b0	↑	↑	R	P	R	↑
		00 100 110																
	SLA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011										C b7 b0 0						
		<d>																
		00 100 110																
	SLA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 100 110																
	SRA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 101 g																
	SRA (HL)	11 001 011					S/D			2	13	b7 b0 C	↑	↑	R	P	R	↑
		00 101 110																
	SRA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRL g	11 001 011				S/D				2	7	0 b7 b0 C	↑	↑	R	P	R	↑
		00 111 g																

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD (IX+d),m LD (IY+d),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	IX+ d IY+d	DATA	1	0	0	1	1	1	1
LD A, (BC) LD A, (DE)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	BC DE	DATA	0	1	0	1	1	1	1
LD A,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
LD (BC),A LD (DE),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	BC DE	A	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD HL, (mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC3	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC4	T1T2T3	mn	DATA	0	1	0	1	1	1	1
	MC5	T1T2T3	mn+1	DATA	0	1	0	1	1	1	1
LD ww,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	mn	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	mn+ 1	DATA	0	1	0	1	1	1	1
LD IX,(mn) LD IY,(mn)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	n	0	1	0	1	1	1	1
	MC4	T1T2T3	2nd operand Address	m	0	1	0	1	1	1	1
	MC5	T1T2T3	mn	DATA	0	1	0	1	1	1	1
	MC6	T1T2T3	mn+1	DATA	0	1	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
RLC (HL) RL (HL) RRC (HL) RR (HL) SLA (HL) SRA (HL) SRL (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	HL	DATA	1	0	0	1	1	1	1
RLC (IX + d) RLC (IY + d) RL (IX + d) RL (IY + d) RRC (IX + d) RRC (IY + d) RR (IX + d) RR (IY + d) SLA (IX + d) SLA (IY + d) SRA (IX + d) SRA (IY + d) SRL (IX + d) SRL (IY + d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2ndOp Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4	T1T2T3	3rd Op Code Address	3rd Op Code	0	1	0	1	0	1	1
	MC5	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
	MC6	Ti	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	DATA	1	0	0	1	1	1	1
RLD RRD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC7	TiTiTiTi *		Z	1	1	1	1	1	1	1
	MC8	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

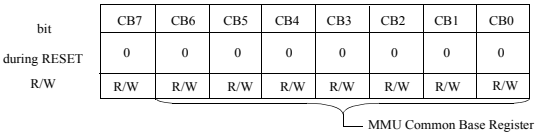
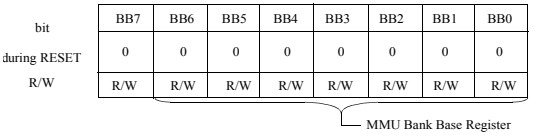
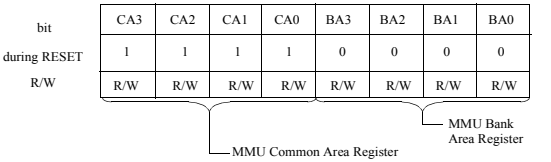
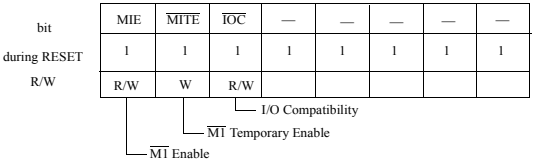
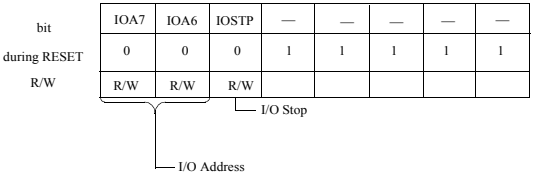
Register	Mnemonics	Address		Remarks
MMU Common Base Register:	CBR	3	8	
MMU Bank Base Register	BBR	3	9	
MMU Common/Bank Register	CBAR	3	A	
Operation Mode Control Register	OMCR	3	E	
I/O Control Register:	ICR	3	F	

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Interrupt Vector Low Register	IL	3	3	
INT/TRAP Control Register	ITC	3	4	
Refresh Control Register:	RCR	3	6	

bit	IL7	IL6	IL5	—	—	—	—	—
during RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

bit	TRAP	UF0	—	—	—	ITE2	ITE1	ITE0
during RESET	0	0	1	1	1	0	0	0
R/W	R/W	R				R/W	R/W	R/W

$\overline{\text{INT}}$ Enable 2,1,0

Unidentified Fetch Object

TRAP

bit	REFE	REFW	—	—	—	—	CYC1	CYC0
during RESET	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle select

Refresh Wait State

Refresh Enable

	Interval of Refresh Cycle
0 0	10 states
0 1	20
1 0	40
1 1	80