Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010pec

Z8018x
Family MPU User Manual

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

UM005003-0703

Table 23. Timer Output Control 163
Table 24. E Clock Timing in Each Condition 166
Table 25. Z8X180 Operating Frequencies 169

Software Architecture 173

Table 26. Instruction Set Summary 173

DC Characteristics 185

Table 27. Absolute Maximum Rating 185
Table 28. Z80180 DC Characteristics 186
Table 29. Z8S180 DC Characteristics 187
Table 30. Z8L180 DC Characteristics 189

AC Characteristics 193

Table 31. Z8S180 AC Characteristics 193

Instruction Set 207

Table 32. Register Values 207
Table 33. Bit Values 208
Table 34. Instruction Values 208
Table 35. Address Values 209
Table 36. Flag Conditions 209
Table 37. Operations Mnemonics 210
Table 38. Arithmetic and Logical Instructions (8-bit) 211
Table 39. Rotate and Shift Instructions 216
Table 40. Arithmetic Instructions (16-bit) 221
Table 41. 8-Bit Load 222
Table 42. 16-Bit Load 223

Table 43. Block Transfer 225
Table 44. Stock and Exchange 227
Table 45. Program Control Instructions 229
Table 46. I/O Instructions 231
Table 47. Special Control Instructions 235

Op Code Map 247

Table 48. 1st Op Code Map Instruction Format: XX 247
Table 49. 2nd Op Code Map Instruction Format: CB XX 249
Table 50. 2nd Op Code Map Instruction Format: ED XX 250

Bus Control Signal Conditions 251

Table 51. Bus and Control Signal Condition in Each Machine Cycle 251
Table 52. Interrupts 279

Operating Modes Summary 281

Table 53. Request Acceptances in Each Operating Mode 281
Table 54. The Z80180 Types of Requests 282

Status Signals 287

Table 55. Pin Outputs in Each Operating Mode 287
Table 56. Pin Status During RESET and LOW POWER OPERATION Modes 289

I/O Registers 293

Table 57. Internal I/O Registers 293

3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally *latched* (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and has no timing relationship with the exit from SLEEP mode.
4. Regarding (2) and (3), the refresh address is incremented by one for each successful refresh cycle, not for each refresh request. Thus, independent of the number of *missed* refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

DMA Controller (DMAC)

The Z8X180 contains a two-channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) feature the following capabilities:

- Memory Address Space

  Memory source and destination addresses can be directly specified anywhere within the 1024KB physical address space using 20-bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64KB physical address boundaries without CPU intervention.

- I/O Address Space

  I/O source and destination addresses can be directly specified anywhere within the 64KB I/O address space (16-bit source and destination I/O addresses).

- Transfer Length

  Up to 64KB are transferred based on a 16- bit byte count register.

$\overline{\text{DREQ0}}$ for ASCI transmission and reception respectively. To initiate memory to/from ASCI DMA transfer, perform the following operations:

1. Load the source and destination addresses into SAR0 and DAR0 Specify the I/O (ASCI) address as follows:
   a. Bits A0–A7 must contain the address of the ASCI channel transmitter or receiver (I/O addresses 6H-9H).
   b. Bits A8–A15 must equal 0.
   c. Bits SAR17–SAR16 must be set according to Table 16 to enable use of the appropriate ASCI status bit as an internal DMA request.

Table 16. DMA Transfer Request

SAR18	SAR17	SAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	RDRF (ASCI channel 0)
X	1	0	RDRF (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

DAR18	DAR17	DAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	TDRE (ASCI channel O)
X	1	0	TDRE (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

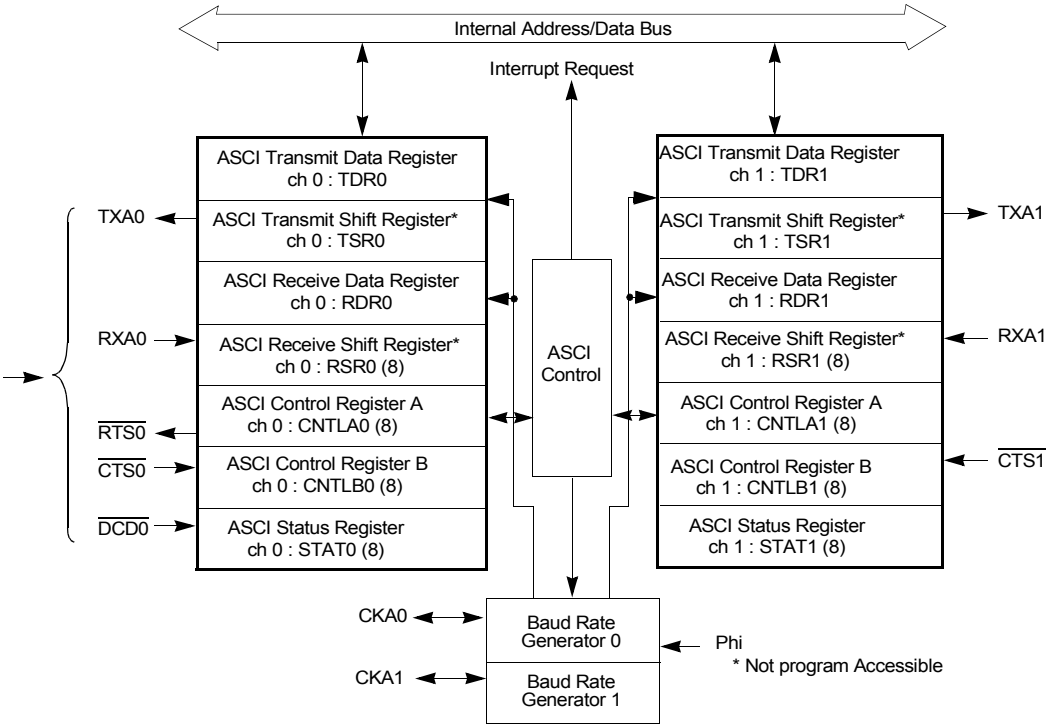


Figure 52. ASCI Block Diagram

ASCI Register Description

The following subparagraphs explain the various functions of the ASCI registers.

ASCI Transmit Shift Register 0, 1 (TSR0, 1)

When the ASCI Transmit Shift Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin.

ASCI Control Register A0, 1 (CNTLA0, 1)

Each ASCI channel Control Register A configures the major operating modes such as receiver/transmitter enable and disable, data format, and multiprocessor communication mode.

ASCI Status Register 1 (STAT1: 05H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
R/W	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF	R		**Receive Data Register Full** — RDRF is set to 1 when an incoming data byte is loaded into RDR. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into RDR. RDRF is cleared to 0 by reading RDR, when the DCD0 input is High, in IOSTOP mode, and during RESET.
6	OVRN	R		**Overrun Error** — OVRN is set to 1 when RDR is full and RSR becomes full. OVRN is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
5	PE	R		**Parity Error** — PE is set to 1 when a parity error is detected on an incoming data byte and ASCI parity detection is enabled (the MOD1 bit of CNTLA is set to 1). PE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.

Bit Position	Bit/Field	R/W	Value	Description
5	$\overline{\text{CTS}}$/PS	R/W		**Clear to Send/Prescale** — When read, $\overline{\text{CTS}}$/PS reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}$/PS is read as 1. When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0). For channel 1, the $\overline{\text{CTS1}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}$/PS is only valid when read if the channel 1 CTS1E bit is 1 and the CST1 input pin function is selected. The read data of $\overline{\text{CTS}}$/PS is not affected by RESET. When written, CT /PS specifies the baud rate generator prescale factor. If $\overline{\text{CTS}}$/PS is set to 1, the system clock is prescaled by 30 while if $\overline{\text{CTS}}$/PS is cleared to 0, the system clock is prescaled by 10.CTS/PS is cleared to 0 during RESET.
4	PEO	R/W		**Parity Even Odd** — PE0 selects even or odd parity. PE0 does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PE0 is cleared to 0, even parity is selected. If PE0 is set to 1, odd parity is selected.PE0 is cleared to 0 during RESET.
3	DR	R/W		**Divide Ratio** — DR specifies the divider used to obtain baud rate from the data sampling clock If DR is reset to 0, divide by 16 is used, while if DR is set to 1, divide by 64 is used. DR is cleared to 0 during RESET.
2–0	SS2–0	R/W		**Source/Speed Select** — Specifies the data clock source (internal or external) and baud rate prescale factor. SS2, SS1, and SS0 are all set to 1 during RESET. Table 18 describes the divide ratio corresponding to SS2, SS1 and SS0

The external ASCI channel 0 data clock pins are multiplexed with DMA control lines (CKA0/$\overline{\text{DREQ}}$ and CKA1/$\overline{\text{TEND0}}$). During RESET, these

Table 19. ASCI Baud Rate Selection (Continued)

Prescaler		Sampling Rate		Baud Rate				General Divide Ratio	Baud Rate (Example) (BPS)			CKA	
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio		ϕ = 6.144 MHz	ϕ = 4.608 MHz	ϕ = 3.072 MHz	I/O	Clock Frequency
1	ϕ ÷ 30	0	16	0	0	0	÷1	ϕ ÷ 480		9600			ϕ ÷ 30
				0	0	1	2	960		4800			60
				0	1	0	4	1920		2400			120
				0	1	1	8	3840		1200		0	240
				1	0	0	16	7680		600			480
				1	0	1	32	15360		300			960
				1	1	0	64	30720		150			1920
				1	1	1	—	fc ÷ 16	—	—	—	I	fc
		1	64	0	0	0	÷1	ϕ ÷ 1920		2400			ϕ ÷ 30
				0	0	1	2	3840		1200			60
				0	1	0	4	7680		600			120
				0	1	1	8	15360		300		0	240
				1	0	0	16	30720		150			480
				1	0	1	32	61440		75			960
				1	1	0	64	122880		37.5			1920
				1	1	1	—	fc ÷ 64	—	—	—	I	fc

Baud Rate Generator (Z8S180/Z8L180-Class Processors Only)

The Z8S180/Z8L180 Baud Rate Generator (BRG) features two modes. The first is the same as in the Z80180. The second is a 16-bit down counter that divides the processor clock by the value in a 16-bit time constant register, and is identical to the DMSCC BRG. This feature allows

Timer Reload Register Channel 0L (RLDR0L: 0EH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Reload Register Channel 0H (RLDR0L: 0FH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Data Register 1L (TMDR1L: 14H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Data Register 1H (TMDR1H: 15H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Table 28. Z80180 DC Characteristics (Continued)

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
	Power Dissipation* (SYSTEM STOP mode)	f = 6 MHz f = 8 MHz f = 33 MHz	– – –	3.8 5 6.3	12.5 15.0 17.5	mA mA mA
CP	Pin Capacitance	VIN = 0V, f = 1MHz TA = 25°C	–	–	12	pF
Notes: * VIN min = V_{CC} –1.0V. VIL max = 0.8V (All output terminals are a no load.) V_{CC} = 5.0V						

Z8S180 DC CHARACTERISTICS

V_{CC} = 5V ± 10%, V_{SS} = OV, Ta = 0° to +70°C, unless otherwise noted.

Table 29. Z8S180 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VIH1	Input High Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		V_{CC} –0.6	–	V_{CC} +0.3	V
VIH2	Input High Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		2.0		V_{CC} +0.3	V
VIH3	Input High Voltage CKS, CKA0, CKA1		2.4		V_{DD} + 0.3	V
VIL1	Input Low Voltage $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.6	V
VIL2	Input Low Voltage except $\overline{RESET}$, EXTAL $\overline{NMI}$		–0.3		0.8	V

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
OR	OR g	10 110 g				S		D		1	4	Ar + gr→Ar	↑	↑	R	P	R	R
	OR (HL)	10 110 110					S	D		1	6	Ar + $(HL)_M$→Ar	↑	↑	R	P	R	R
	OR m	11 110 110	S					D		2	6	Ar + m→Ar	↑	↑	R	P	R	R
		<m>																
	OR (IX + d)	11 011 101			S			D		3	14	Ar + $(IX + d)_M$→Ar	↑	↑	R	P	R	R
		10 110 110																
		<d>																
	OR (IY + d)	11 111 101			S			D		3	14	Ar + $(IY + d)_M$→Ar	↑	↑	R	P	R	R
		10 110 110																
		<d>																
SUB	SUB g	10 010 g				S		D		1	4	Ar-gr→Ar	↑	↑	↑	V	S	↑
	SUB (HL)	10 010 110					S	D		1	6	Ar-$(HL)_M$→Ar	↑	↑	↑	V	S	↑
	SUB m	11 010 110	S					D		2	6	Ar-m→Ar	↑	↑	↑	V	S	↑
		<m>																
	SUB (IX + d)	11 011 101			S			D		3	14	Ar-$(IX + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 011 110																
		<d>																
	SUB (IY + d)	11 111 101			S			D		3	14	Ar-$(IY + d)_M$-c→Ar	↑	↑	↑	V	S	↑
		10 010 110																
		<d>																

Table 39. Rotate and Shift Instructions (Continued)

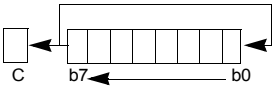
Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	RLC (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 000 110																
	RLC (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 000 110																
	RLD	11 101 101						S/D		2	16		↑	↑	R	P	R	•
		01 101 111																
	RRA	00 011 111						S/D		1	3		•	•	R	•	R	↑
	RRg	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 011 g																
	RR (HL)	11 001 011					S/D			2	13		↑	↑	R	P	R	↑
		00 011 110																
	RR (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 011 110																
	RR (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 011 110																
	RRCA	00 001 111						S/D		1	3		•	•	R	•	R	↑
	RRC g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 001 g																
	RRC (HL)	11 001 011					S/D			2	13		↑	↑	R	P	R	↑
		00 001 110																
	RRC (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 001 110																
	RRC (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
		11 001 011																
		<d>																
		00 001 110																
	RRD	11 101 101						S/D		2	16		↑	↑	R	P	R	•
		01 100 111										Ar b7 b0						
	SLA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 100 g																
	SLA (HL)	11 001 011					S/D			2	13	(HL)M b7 b0	↑	↑	R	P	R	↑
		00 100 110																
	SLA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011										C b7 b0 0						
		<d>																
		00 100 110																
	SLA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 100 110																
	SRA g	11 001 011				S/D				2	7		↑	↑	R	P	R	↑
		00 101 g																
	SRA (HL)	11 001 011					S/D			2	13	b7 b0 C	↑	↑	R	P	R	↑
		00 101 110																
	SRA (IX + d)	11 011 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRA (IY + d)	11 111 101			S/D					4	19		↑	↑	R	P	R	↑
		11 001 011																
		<d>																
		00 101 110																
	SRL g	11 001 011				S/D				2	7	0 b7 b0 C	↑	↑	R	P	R	↑
		00 111 g																

MNEMONICS	Bytes	Machine Cycles	States
PUSH IX	2	6	14
PUSH IY	2	6	14
PUSH zz	1	5	11
RES b,(HL)	2	5	13
RES b,(IX+d)	4	7	19
RES b,(IY+d)	4	7	19
RES b,g	2	3	7
RET	1	3	9
RET f	1	3	5
			(If condition is false)
	1	4	10
			(If condition is true)
RETI	2	4 (R0, R1)	12 (R0, R1)
	10 (Z)		22 (Z)
RETN	2	4	12
RLA	1	1	3
RLCA	1	1	3
RLC (HL)	2	5	13
RLC (IX-1-dl	4	7	19
RLC (IY+d)	4	7	19
RLC g	2	3	7
RLD	2	8	16
RL (HL)	2	5	13
RL (IX+d)	4	7	19
RL (IY+d)	4	7	19
RL g	2	3	7
RRA	1	1	3
RRCA	1	1	3
RRC (HL)	2	5	13
RRC (IX+d)	4	7	19

Bus Control Signal Conditions

BUS AND CONTROL SIGNAL CONDITION IN EACH MACHINE CYCLE

* (ADDRESS) invalid

Z (DATA) high impedance.

** added new instructions to Z80

Table 51. Bus and Control Signal Condition in Each Machine Cycle

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
ADD HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC5	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADD IX,xx ADD IY,yy	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADC HL,ww SBC HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
ADD A,g ADC A,g SUB g SBC A,g AND g OR g XOR g CP g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
ADD A,m ADC A,m SUB m SBC A,m AND m OR m XOR m CP m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
ADD A, (HL) ADC A, (HL) SUB (HL) SBC A, (HL) AND HU OR (HL) XOR (HL) CP (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	HL	DATA	0	1	0	1	1	1	1
ADD A, (IX+ d) ADD A, (IY+d) ADC A, (IX+d) ADC A, (IY+d) SUB (lX+d) SUB (IY+d) SBC A, (IX+ d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
SBC A, (IY+ d) AND (IX+d)	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
OUT (m),A	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	m to A0~A7 A to A8~A15	A	1	0	1	0	1	1	1
OUT (C),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	BC	g	1	0	1	0	1	1	1
OUT0 (m),g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	m to A0~A7 00H to A8~A15	g	1	0	1	0	1	1	1

Operating Modes Summary

REQUEST ACCEPTANCES IN EACH OPERATING MODE

Table 53. Request Acceptances in Each Operating Mode

Current Status / Request		Normal Operation (CPU mode and IOSTOP Mode)	WAIT State	Refresh Cycle	Interrupt Acknowledge Cycle	DMA Cycle	BUS RELEASE Mode	SLEEP Mode	SYSTEM STOP Mode
$\overline{WAIT}$		Acceptable	Acceptable	Not acceptable	Acceptable	Acceptable	Not acceptable	Not acceptable	Not acceptable
Refresh Request Request of Refresh by the on-chip Refresh Controller		Refresh cycle begins at the end of Machine Cycle (MC)	Not acceptable	Not acceptable	Refresh cycle begins at the end MC	Refresh cycle begins at the end of MC	Not acceptable	Not acceptable	Not acceptable
$\overline{DREQ0}$ $\overline{DREQ1}$		DMA cycle begins at the end of MC	DMA cycle begins at the end of MC	Acceptable Refresh cycle precedes. DMA cycle begins at the end of one MC	Acceptable DMA cycle begins at the end of MC.	Acceptable Refer to "DMA Controller" for details.	Acceptable *After BUS RELEASE cycle, DMA cycle begins at the end of one MC	Not acceptable	Not acceptable
$\overline{BUSREQ}$		Bus is released at the end of MC	Not acceptable	Not acceptable	Bus is released at the end of MC	Bus is released at the end of MC	Continue BUS RELEASE mode	Acceptable	Acceptable
Interrupt	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$	Accepted after executing the current instruction.	Accepted after executing the current instruction	Not acceptable	Not acceptable	Not acceptable	Not acceptable	Acceptable Return from SLEEP mode to normal operation.	Acceptable Return from SYSTEM STOP mode to normal operation

DMA TEND0 output 108
E clock (memory and I/O R/W cycles) 201
E clock (R/W and INTACK cycles) 167
E clock (SLEEP and SYSTEM STOP modes) 168
E clock BUS RELEASE, SLEEP and SYSTEM STOP modes) 201
E clock minimum timing example of PWEL and PWEH) 202
External clock rise and fall 204
HALT 33
I/O Read and Write cycles with IOC = 0 17
I/O read and write cycles with IOC=1 17
I/O read/write timing 23
Input rise and fall time 204
Instruction 24
INT0 interrupt mode 2 80
INT0 mode 0 76
INT0 mode 1 78
INT1, INT2 and Internal interrupts 86
M1 temporary enable 16
Memory read/write timing (with Wait state) 22
Memory read/write timing (without Wait state) 21
NMI and DMA operation 115
Op Code Fetch timing (with Wait state) 20
Op Code Fetch timing (without Wait state) 19
PRT bus release mode 167
Refresh cycle 87
RESET 25
RTS0 140
SLEEP 35
TRAP timing - 2nd Op Code Undefined 71
TRAP timing - 3rd Op Code Undefined 72
WAIT 28
TRAP 68
Interrupt 70
Timing 71

U

Undefined Fetch Object (UFO) 68

V

Vector acquisition
INT0 mode 2 79
INT1, INT2 81
Vector table 82

W

Wait state generation
I/O Wait insertion 29
Memory and 29
Programmable Wait state insertion 28
Wait input and reset 30
Wait state insertion 30