Zilog - Z8018010PEG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010peg

D0–D7. *Data Bus (Bidirectional, Active High, 3-state).* D0-D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during RESET and external bus acknowledge cycles.

$\overline{\text{DCD0}}$. *Data Carrier Detect 0 (Input, Active Low).* This input is a programmable modem control signal for ASCI channel 0.

$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$. *DMA Request 0 and 1 (Input, Active Low).* DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level- or edge-sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0.

E. *Enable Clock (Output, Active High).* Synchronous machine cycle clock output during bus transactions.

EXTAL. *External Clock/Crystal (Input, Active High).* Crystal oscillator connection. An external clock can be input to the Z8X180 on this pin when a crystal is not used. This input is Schmitt-triggered.

$\overline{\text{HALT}}$. *Halt/Sleep Status (Output, Active Low).* This output is asserted after the CPU has executed either the $\overline{\text{HALT}}$ or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. $\overline{\text{HALT}}$ is also used with the $\overline{\text{M1}}$ and ST signals to decode status of the CPU machine cycle.

$\overline{\text{INT0}}$. *Maskable Interrupt Request 0 (Input, Active Low).* This signal is generated by external I/O devices. The CPU honors this request at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become Active.

$\overline{\text{INT1}}$, $\overline{\text{INT2}}$. *Maskable Interrupt Requests 1 and 2 (Inputs, Active Low).* This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$, To avoid address conflicts with external I/O, the Z8X180 internal I/O addresses can be relocated on 64-byte boundaries within the bottom 256 bytes of the 64KB I/O address space.

I/O Control Register (ICR)

ICR allows relocating of the internal I/O addresses. ICR also controls enabling/disabling of the IOSTOP mode.

I/O Control Register (ICR: 3FH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	IOA7	IOA6	IOSTP	—	—	—	—	—
R/W	R/W	R/W	R/W					
Reset	0	0	0					

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–6	IOA7:6	R/W		IOA7 and IOA6 relocate internal I/O as depicted in Figure . The high-order 8 bits of 16-bit internal I/O addresses are always 0. IOA7 and IOA6 are cleared to 0 during RESET.
5	IOSTP	R/W		IOSTOP mode is enabled when IOSTP is set to 1. Normal. I/O operation resumes when IOSTP is reset to 0.

Table 8. State of IEF1 and IEF2 (Continued)

CPU Operation	IEF1	IEF2	REMARKS
DI	0	0	
LD A, I	not affected	not affected	Transfers the contents of IEF1 to P/V
LID A, R	not affected	not affected	Transfers the contents of IEF1 to P/V

TRAP Interrupt

The Z8X180 generates a non-maskable (not affected by the state of IEF1) TRAP interrupt when an undefined Op Code fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during Op Code fetch cycles and also if an undefined Op Code is fetched during the interrupt acknowledge cycle for $\overline{\text{INT0}}$ when Mode 0 is used.

When a TRAP interrupt occurs the Z8X180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to `1`.
2. The current PC (Program Counter) value, reflecting location of the undefined Op Code, is saved on the stack.
3. The Z8X180 vectors to logical address 0. Note that if logical address `0000H` is mapped to physical address `00000H`. the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address `00000H` was caused by RESET or TRAP.

The state of the UFO (Undefined Fetch Object) bit in ITC allows TRAP manipulation software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the Op Code generated the TRAP. If UFO is `0`, the starting address of the invalid instruction is equal to the

Table 13. Channel 0 Source

SM1	SM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 14 describes all DMA TRANSFER mode combinations of DM0 DM1, SM0 SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
0	0	0	0	Memory to Memory	SAR0+1, DAR0+1
0	0	0	1	Memory to Memory	SAR0-1, DAR0+1
0	0	1	0	Memory* to Memory	SAR0 fixed, DAR0+ 1
0	0	1	1	I/O to Memory	SAR0 fixed DAR0+1
0	1	0	0	Memory to Memory	SAR0+1, DAR0-1
0	1	0	1	Memory to Memory	SAR0-1,DAR0-1
0	1	1	0	Memory to Memory	SAR0 fixed, DAR0-1
0	1	1	1	I/O to Memory	SAR0 fixed. DAR0-1
1	0	0	0	Memory to Memory*	SAR0+ 1, DAR0 fixed
1	0	0	1	Memory to Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	

Table 15. Channel 1 Transfer Mode

DIM1	DIM0	Transfer Mode	Address Increment/Decrement
0	0	Memory to I/O	MARI +1, IAR1 fixed
0	1	Memory to I/O	MARI -1, IAR1 fixed
1	0	I/O to Memory	IAR1 fixed, MAR1+1
1	1	I/O to Memory	IAR1 fixed, MAR1-1

DMA I/O Address Register Ch. 1 (IAR1B: 2DH) (Z8S180/L180-Class Processor Only)

Bit	7	6	5	4	3	2	1	0
Bit/Field			Reserved					
R/W	R/W	R/W	R/W		R/W	R/W		
Reset	0	0	0		0	0		

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7		R/W		Alternating Channels
			0	DMA Channels are independent
			1	Toggle between DMA channels for same device
6		R/W		Currently selected DMA channel when Bit 7 = 1
5–4	Reserved	R/W	0	Reserved. Must be 0.
3		R/W	0	TOUT/$\overline{\text{DREQ}}$ is DREQ In
			1	TOUT/$\overline{\text{DREQ}}$ is TOUT Out

4. Specify whether DREQ1 is level- or edge- sense in the DMS1 bit in DCNTL.

5. Enable or disable DMA termination interrupt with the DIE1 bit in DSTAT.

6. Program DE1 = `1` (with DWE1 = 0 in the same access) in DSTAT and the DMA operation with the external I/O device begins using the external DREQ1 input and TEND1 output.

DMA Bus Timing

When memory (and memory mapped I/O) is specified as a source or destination, MREQ goes Low during the memory access. When I/O is specified as a source or destination, IORQ goes Low during the I/O access.

When I/O (and memory mapped I/O) is specified as a source or destination, the DMA timing is controlled by the external DREQ input and the TEND output indicates DMA termination

Note: External I/O devices may not overlap addresses with internal I/O and control registers, even using DMA.

For I/O accesses, one Wait State is automatically inserted. Additional Wait States can be inserted by programming the on-chip wait state generator or using the external WAIT input.

Note: For memory mapped I/O accesses, this automatic I/O Wait State is not inserted.

For memory to memory transfers (channel 0 only), the external DREQ0 input is ignored. Automatic DMA timing is programmed as either BURST or CYCLE STEAL.

When a DMA memory address carry/borrow between bits A15 and A16 of the address bus occurs (crossing 64KB boundaries), the minimum bus

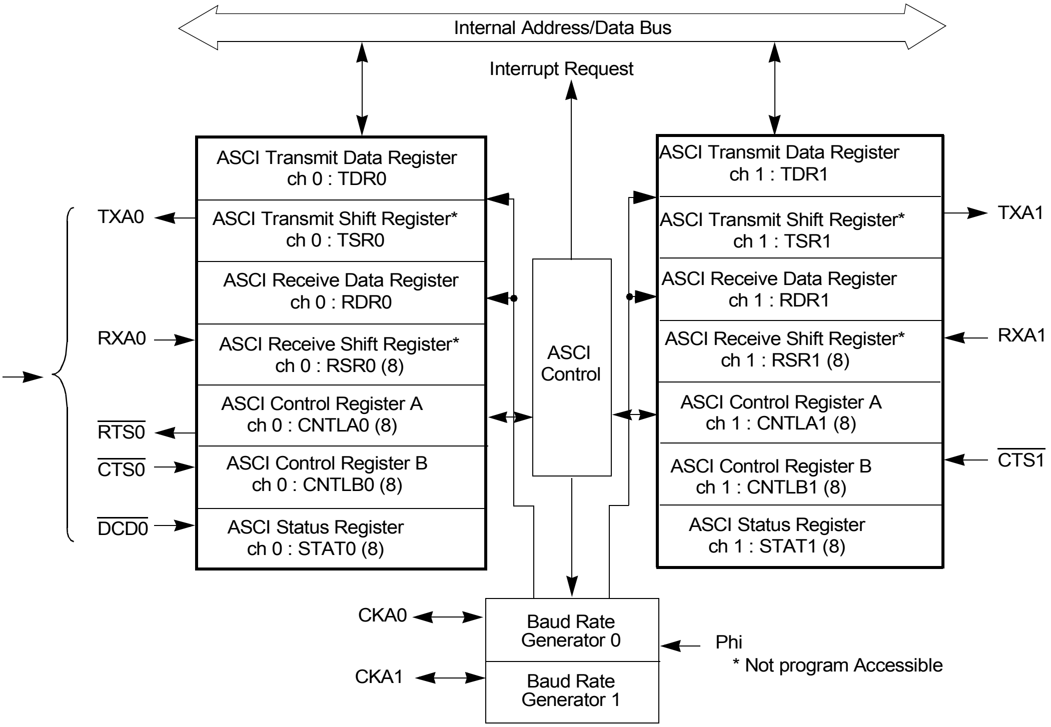

Figure 52. ASCI Block Diagram

ASCI Register Description

The following subparagraphs explain the various functions of the ASCI registers.

ASCI Transmit Shift Register 0, 1 (TSR0, 1)

When the ASCI Transmit Shift Register receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin.

ASCI Receive Shift Register 0,1(RSR0, 1)

This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. The RSR is not program-accessible.

ASCI Receive Data Register 0,1 (RDR0, 1: I/O Address = 08H, 09H)

When a complete incoming data byte is assembled in RSR, it is automatically transferred to the RDR if RDR is empty. The next incoming data byte can be shifted into RSR while RDR contains the previous received data byte. Thus, the ASCI receiver on Z80180 is double-buffered.

ASCI Receive Data Register Ch. 0 (RDR0: 08H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	ASCI Receive Channel 0							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

ASCI Receive Data Register Ch. 1 (RDR1: 09H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	ASCI Receive Channel 1							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

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On the Z8S180 and Z8L180-class processors are quadruple buffered. The ASCI Receive Data Register is a read-only register. However, if RDRF =

Bit Position	Bit/Field	R/W	Value	Description
6	RE	R/W		**Receiver Enable** — When RE is set to 1, the ASCI receiver is enabled. When RE is reset to 0, the receiver is disabled and any receive operation in progress is interrupted. However, the RDRF and error flags are not reset and the previous contents of RDRF and error flags are held. RE is cleared to 0 in IOSTOP mode, and during RESET.
5	TE	R/W		**Transmitter Enable** — When TE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode, and during RESET.
4	$\overline{\text{RTS0}}$	R/W		**Request to Send Channel 0** — When $\overline{\text{RTS0}}$ is reset to 0, the $\overline{\text{RTS0}}$ output pin goes Low. When $\overline{\text{RTS0}}$ is set to 1, the $\overline{\text{RTS0}}$ output immediately goes High.
3	MPBR/ EFR	R/W		**Multiprocessor Bit Receive/Error Flag Reset** — When multiprocessor mode is enabled (MP in CNTLB is 1), MPBR, when read, contains the value of the MPB bit for the last receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE and PE) to 0. MPBR/EFR is undefined during RESET.

Table 17. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit date + 2 Stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit date + parity + 2 stop

ASCI Control Register B0, 1 (CNTLB0, 1)

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

These devices require connection with the Z8X180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z8X180 clock rate. Table 24, and Figure 67 through Figure 70 define E clock output timing.

Wait States are inserted in Op Code fetch, memory read/write, and I/O read/write cycles which extend the duration of E clock output High. During I/O read/write cycles with no Wait States (only occurs during on-chip I/O register accesses), E does not go High.

Table 24. E Clock Timing in Each Condition

Condition	Duration of E Clock Output High	
Op Code Fetch Cycle Memory Read/Write Cycle	T2 rise - T3 fall	(1.5 Phi + nw x Phi)
I/O read Cycle	1st Tw rise - T3 fall	(0.5Phi + nw x Phi)
I/O Write Cycle	1st Tw rise - T3 rise	In$_{W}$ x Phi)
$\overline{\text{NMI}}$ Acknowledge 1st MC	T2 rise - T3 fall	(1.5 Phi)
$\overline{\text{INT0}}$ Acknowledge 1st MC	1st Tw rise - T3 fall	(0.50 + nw x Phi)
BUS RELEASE mode SLEEP mode SYSTEM STOP mode	Phi fall - Phi fall	(2 Phi or 1 Phi)
Note: nw = the number of Wait States; MC: Machine Cycle		

IO (I/O)

IO addressing mode is used only by I/O instructions. This mode specifies I/O address ($\overline{\text{IORQ}}$ is `0`) and outputs them as follows.

1. An operand is output to A0–A7. The contents of accumulator is output to A8–A15.
2. The contents of Register B is output to A0–A7. The contents of Register C is output to A8–A15.
3. An operand is output to A0–A7. `00H` is output to A8–A15 (useful for internal I/O register access)
4. The contents of Register C is output to A0–A7. `00H` is output to A8–A15 (useful for internal I/O register access).

Instruction Summary

** : Added new instructions to Z80

MNEMONICS	Bytes	Machine Cycles	States
ADC A,m	2	2	6
ADC A,g	1	2	4
ADC A, (HL)	1	2	6
ADC A, (IX+d)	3	6	14
ADC A, (IY+d)	3	6	14
ADD A,m	2	2	6
ADD A,g	1	2	4
ADD A, (HL)	1	2	6
ADD A, (IX+d)	3	6	14
ADD A, (IY+d)	3	6	14
ADC HL,ww	2	6	10
ADD HL,ww	1	5	7
ADD IX,xx	2	6	10
ADD IY,yy	2	6	10
AND m	2	2	6
AND g	1	2	4
AND (HL)	1	2	6
AND (IX+d)	3	6	14
AND (IY+d)	3	6	14
BIT b, HU	2	3	9
BIT b, (IX+d)	4	5	15
BIT b, (IY+d)	4	5	15
BIT b,g	2	2	6
CALL f,mn	3	2	6 (If condition is false)

MNEMONICS	Bytes	Machine Cycles	States
	3	3	9 (If f is true)
JP (HL)	1	1	3
JP (IX)	2	2	6
JP (IY)	2	2	6
JP mn	3	3	9
JR j	2	4	8
JR C,j	2	2	6 (If condition is false)
	2	4	8 (If condition is true)
JR NC,j	2	2	6 (if condition is false)
	2	4	8 (If condition is true)
JR Z,j	2	2	6 (If condition is false)
	2	4	8 If condition is true)
JR NZ,j	2	2	6 (If condition is false)
	2	4	8 (If condition is true)
LD A, (BC)	1	2	6
LD A, (DE)	1	2	6
LD A,I	2	2	6
LD A, (mn)	3	4	12
LD A,R	2	2	6
LD (BC),A	1	3	7
LDD	2	4	12

Note 1: (HL) replaces g.

Note 2: (HL) replaces s.

Note 3: If DDH is supplemented as first Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IX and (HL) with (IX+d).

```
ex. 22H : LD (mn), HL
```

```
DDH 22H : LD (mn), IX
```

If FDH is supplemented as 1st Op Code for the instructions which have HL or (HL) as an operand in Table 48, the instructions are executed replacing HL with IY and (HL) with (IY+d).

```
ex. 34H : INC (HL)
```

```
FDH 34H : INC (IY+d)
```

However, JP (HL) and EX DE, HL are exceptions and note the following.

- If DDH is supplemented as 1st Op Code for JP (HL), (IX) replaces (HL) as operand and JP (IX) is executed
- If FDH is supplemented as 1st Op Code for JP (HL), (IY) replaces (HL) as operand and JP (IY) is executed
- Even if DDH or FDH is supplemented as 1st Op Code for EX DE, HL, HL is not replaced and the instruction is regarded as illegal instruction.

Bus Control Signal Conditions

BUS AND CONTROL SIGNAL CONDITION IN EACH MACHINE CYCLE

* (ADDRESS) invalid

Z (DATA) high impedance.

** added new instructions to Z80

Table 51. Bus and Control Signal Condition in Each Machine Cycle

Instruction	Machine Cycle	States	Address	Data	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{MREQ}}$	$\overline{\text{IORQ}}$	$\overline{\text{M1}}$	$\overline{\text{HALT}}$	ST
ADD HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2 ~MC5	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADD IX,xx ADD IY,yy	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1
ADC HL,ww SBC HL,ww	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3 ~MC6	TiTiTiTi	*	Z	1	1	1	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD g, (IX+d) LD g, (IY+d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC5	TiTi	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
LD (HL),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	HL	g	1	0	0	1	1	1	1
LD (IX + d),g LD (IY + d),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	g	1	0	0	1	1	1	1
LD (HL),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{MREQ}}$	$\overline{\text{IORQ}}$	$\overline{\text{M1}}$	$\overline{\text{HALT}}$	ST
TST g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
TST m**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
TST (HL)**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	2	0	2	0	2	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T23	HL	Data	0	1	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

<table>
<tr><th>Register</th><th>Mnemonics</th><th>Address</th><th>Remarks</th></tr>
<tr><td>MMU Common Base Register:</td><td>CBR</td><td>3 8</td><td>
<table>
<tr><td>bit</td><td>CB7</td><td>CB6</td><td>CB5</td><td>CB4</td><td>CB3</td><td>CB2</td><td>CB1</td><td>CB0</td></tr>
<tr><td>during RESET</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
</table>
MMU Common Base Register</td></tr>
<tr><td>MMU Bank Base Register</td><td>BBR</td><td>3 9</td><td>
<table>
<tr><td>bit</td><td>BB7</td><td>BB6</td><td>BB5</td><td>BB4</td><td>BB3</td><td>BB2</td><td>BB1</td><td>BB0</td></tr>
<tr><td>during RESET</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
</table>
MMU Bank Base Register</td></tr>
<tr><td>MMU Common/Bank Register</td><td>CBAR</td><td>3 A</td><td>
<table>
<tr><td>bit</td><td>CA3</td><td>CA2</td><td>CA1</td><td>CA0</td><td>BA3</td><td>BA2</td><td>BA1</td><td>BA0</td></tr>
<tr><td>during RESET</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
</table>
MMU Bank Area Register
MMU Common Area Register</td></tr>
<tr><td>Operation Mode Control Register</td><td>OMCR</td><td>3 E</td><td>
<table>
<tr><td>bit</td><td>MIE</td><td>$\overline{\text{MITE}}$</td><td>$\overline{\text{IOC}}$</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>during RESET</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>R/W</td><td>R/W</td><td>W</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>
I/O Compatibility
$\overline{\text{M1}}$ Temporary Enable
$\overline{\text{M1}}$ Enable</td></tr>
<tr><td>I/O Control Register:</td><td>ICR</td><td>3 F</td><td>
<table>
<tr><td>bit</td><td>IOA7</td><td>IOA6</td><td>IOSTP</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>during RESET</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr>
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I/O Stop
I/O Address</td></tr>
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