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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010psc

Bit Position	Bit/Field	R/W	Value	Description
2	LNIO	R/W	0 1	Standard Drive 33% Drive on certain external I/O
1	LNCPUCTL	R/W	0 1	Standard Drive 33% Drive on CPU control signals
0	LNAD/ DATA	R/W	0 1	Standard Drive 33% drive on A10–A0, D7–D0

Memory Management Unit (MMU)

The Z8X180 features an on-chip MMU which performs the translation of the CPU 64KB (16-bit addresses 0000H to FFFFH) logical memory address space into a 1024KB (20-bit addresses 00000H to FFFFFH) physical memory address space. Address translation occurs internally in parallel with other CPU operation.

Logical Address Spaces

The 64KB CPU logical address space is interpreted by the MMU as consisting of up to three separate logical address areas, Common Area 0, Bank Area, and Common Area 1.

As depicted in Figure 23, a variety of logical memory configurations are possible. The boundaries between the Common and Bank Areas can be programmed with 4KB resolution.

MMU Register Description

MMU Common/Bank Area Register (CBAR)

CBAR specifies boundaries within the Z8X180 64KB logical address space for up to three areas; Common Area 0, Bank Area and Common Area 1.

MMU Common/Bank Area Register (CBAR: 3AH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–4	CA7–4	R/W		CA specifies the start (low) address (on 4KB boundaries) for the Common Area 1. This also determines the last address of the Bank Area.
3–0	BA3–0	R/W		BA specifies the start (low) address (on 4KB boundaries) for the Bank Area. This also determines the last address of the Common Area 0.

Figure 35. $\overline{\text{NMI}}$ Timing

INT0 - Maskable Interrupt Level 0

The next highest priority external interrupt after $\overline{\text{NMI}}$ is $\overline{\text{INT0}}$. $\overline{\text{INT0}}$ is sampled at the falling edge of the clock state prior to T3 or T1 in the last machine cycle. If $\overline{\text{INT0}}$ is asserted LOW at the falling edge of the clock state prior to T3 or T1 in the last machine cycle, $\overline{\text{INT0}}$ is accepted. The interrupt is masked if either the IEF1 flag or the ITEO (Interrupt Enable 0) bit in ITC are reset to `0`. After $\overline{\text{RESET}}$ the state is as follows:

1. IEF1 is `0`, so $\overline{\text{INT0}}$ is masked
2. ITE0 is `1`, so $\overline{\text{INT0}}$ is enabled by execution of the El (Enable Interrupts) instruction

The $\overline{\text{INT0}}$ interrupt is unique in that 3 programmable interrupt response modes are available - Mode 0, Mode 1 and Mode 2. The specific mode is selected with the IM 0, IM 1 and IM 2 (Set Interrupt Mode) instructions. During $\overline{\text{RESET}}$, the Z8X180 is initialized to use Mode 0 for $\overline{\text{INT0}}$. The 3 interrupt response modes for $\overline{\text{INT0}}$ are:

- Mode 0–Instruction fetch from data bus
- Mode 1–Restart at logical address `0038H`
- Mode 2–Low-byte vector table address fetch from data bus

INT0 Mode 0

During the interrupt acknowledge cycle, an instruction is fetched from the data bus (DO–D7) at the rising edge of T3. Often, this instruction is one of the eight single byte RST (RESTART) instructions which stack the PC and restart execution at a fixed logical address. However, multibyte instructions can be processed if the interrupt acknowledging device can provide a multibyte response. Unlike all other interrupts, the PC is not automatically stacked:

3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally *latched* (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and has no timing relationship with the exit from SLEEP mode.
4. Regarding (2) and (3), the refresh address is incremented by one for each successful refresh cycle, not for each refresh request. Thus, independent of the number of *missed* refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

DMA Controller (DMAC)

The Z8X180 contains a two-channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) feature the following capabilities:

- Memory Address Space

  Memory source and destination addresses can be directly specified anywhere within the 1024KB physical address space using 20-bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64KB physical address boundaries without CPU intervention.

- I/O Address Space

  I/O source and destination addresses can be directly specified anywhere within the 64KB I/O address space (16-bit source and destination I/O addresses).

- Transfer Length

  Up to 64KB are transferred based on a 16- bit byte count register.

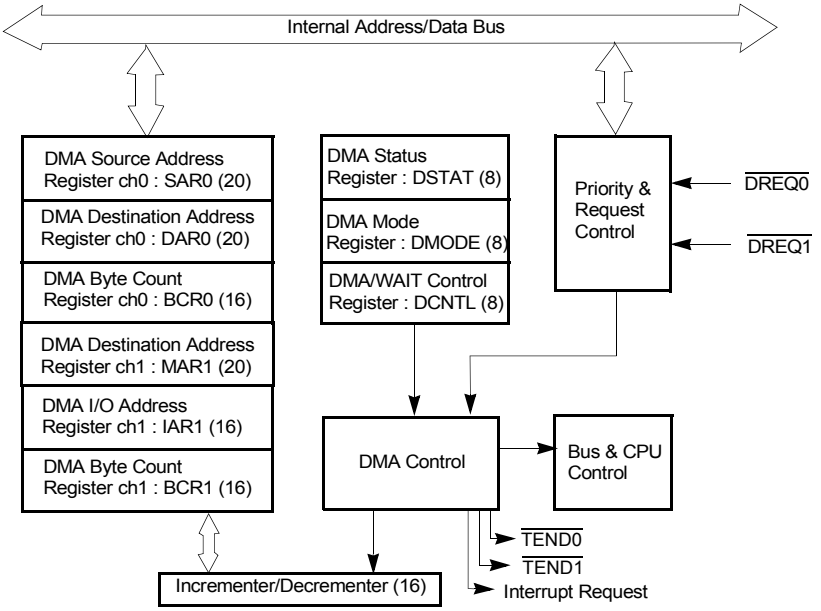


Figure 45. DMAC Block Diagram

DMAC Register Description

DMA Source Address Register Channel 0 (SAR0 I/O Address = 20H to 22H)

Specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O.

DMA Status Register (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also determines DMA transfer status, that is, completed or in progress.

DMA Status Register (DSTAT: 30H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	DE1	DE0	$\overline{\text{DWE1}}$	$\overline{\text{DWE0}}$	DIE1	DIE0	?	DME
R/W	R/W	R/W	W	W	R/W	R/W	?	R
Reset	0	0	1	1	0	0	?	

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	DE1	R/W		**Enable Channel 1** — When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU. To perform a software write to DE1, DWE1 is written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

Table 13. Channel 0 Source

SM1	SM0	Memory/I/O	Address Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	-1
1	0	Memory	fixed
1	1	I/O	fixed

Table 14 describes all DMA TRANSFER mode combinations of DM0 DM1, SM0 SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 14. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Increment/Decrement
0	0	0	0	Memory to Memory	SAR0+1, DAR0+1
0	0	0	1	Memory to Memory	SAR0-1, DAR0+1
0	0	1	0	Memory* to Memory	SAR0 fixed, DAR0+ 1
0	0	1	1	I/O to Memory	SAR0 fixed DAR0+1
0	1	0	0	Memory to Memory	SAR0+1, DAR0-1
0	1	0	1	Memory to Memory	SAR0-1,DAR0-1
0	1	1	0	Memory to Memory	SAR0 fixed, DAR0-1
0	1	1	1	I/O to Memory	SAR0 fixed. DAR0-1
1	0	0	0	Memory to Memory*	SAR0+ 1, DAR0 fixed
1	0	0	1	Memory to Memory*	SAR0-1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	

rising edge of the clock prior to T3 at which time the DMA operation (re)starts. Figure 48 depicts the edge-sense DMA timing.

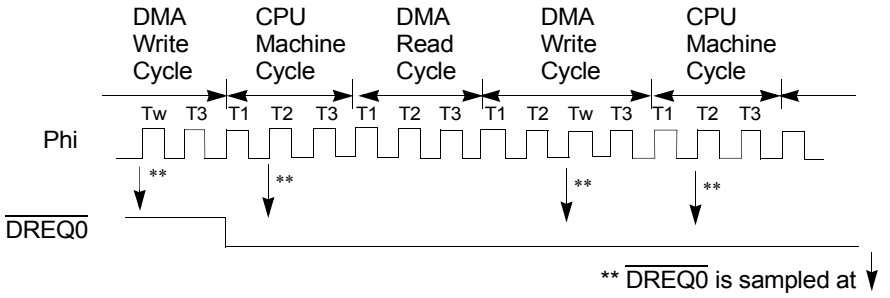


Figure 48. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Edge-Sense

During the transfers for channel 0, the $\overline{\text{TEND0}}$ output goes Low synchronous with the write cycle of the last (BCR0 = 00H) DMA transfer (Reference Figure 49).

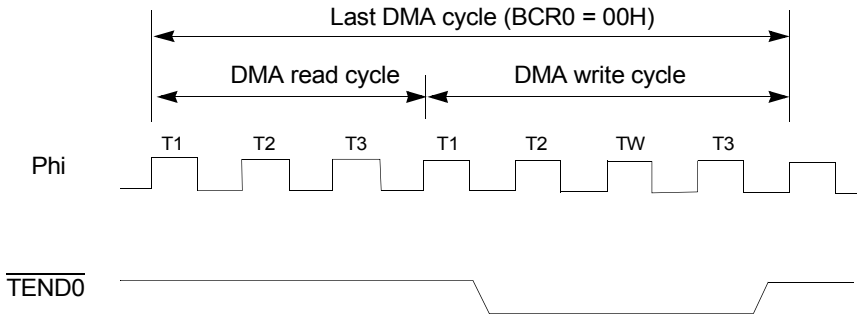


Figure 49. $\overline{\text{TEND0}}$ Output Timing Diagram

The $\overline{\text{DREQ0}}$ and $\overline{\text{TEND0}}$ pins are programmably multiplexed with the CKA0 and CKA1 ASCI clock input/outputs. However, when DMA channel 0 is programmed for memory to/from I/O (and memory to/from

The key functions for ASCI on Z80180, Z8S180 and Z8L180 class processors are listed below. Each channel is independently programmable.

- Full-duplex communication
- 7- or 8-bit data length
- Program controlled 9th data bit for multiprocessor communication
- 1 or 2 stop bits
- Odd, even, no parity
- Parity, overrun, framing error detection
- Programmable baud rate generator, /16 and /64 modes
- Modem control signals – Channel 0 contains $\overline{\text{DCD0}}$, $\overline{\text{CTS0}}$ and $\overline{\text{RTS0}}$; Channel 1 contains $\overline{\text{CTS1}}$
- Programmable interrupt condition enable and disable
- Operation with on-chip DMAC

ASCI Block Diagram for the Z8S180/Z8L180-Class Processors

Figure 52 illustrates the ASCI block diagram.

ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

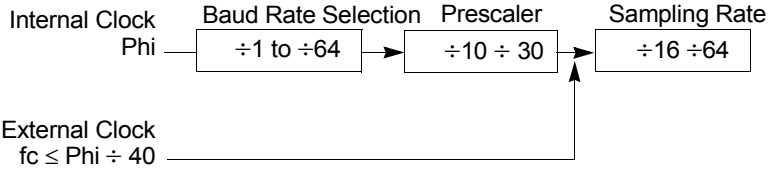


Figure 56. ASCI Clock

Table 23. Timer Output Control

TOC1	TOC0	OUTPUT	
0	0	Inhibited	(A18/TOUT pin is selected as an address output function.)
0	1	Toggled	
1	0	0	A18/TOUT pin is selected as a PRT1 output function!
1	1	1	

Figure 64 illustrates timer initialization, count down, and reload timing. Figure 65 depicts timer output (A18/TOUT) timing.

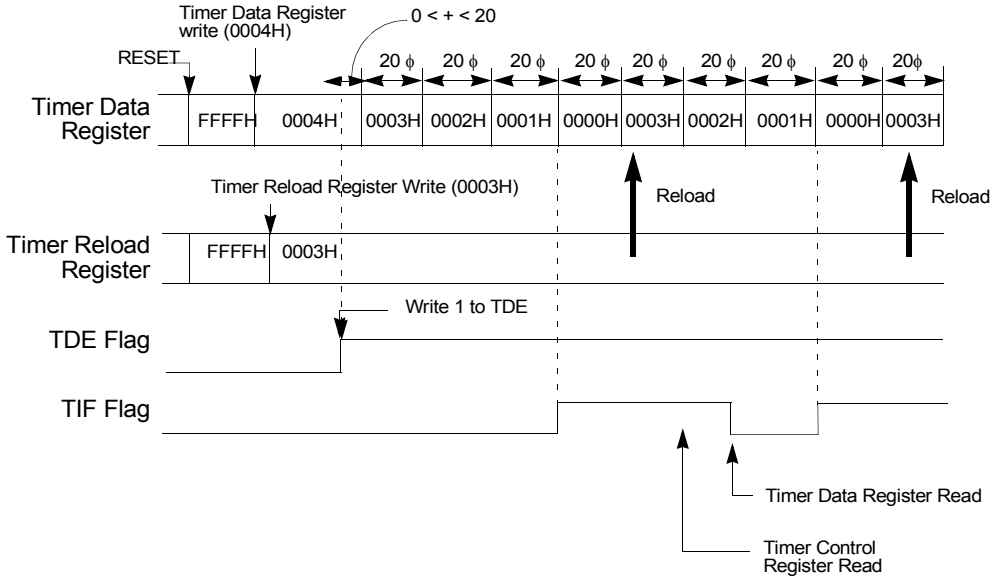


Figure 64. Timer Initialization, Count Down, and Reload Timing Diagram

Stack Pointer (SP)

The Stack Pointer (SP) contains the memory address based LIFO stack. SP is cleared to 0000H during reset.

Program Counter (PC)

The Program Counter (PC) contains the address of the instruction to be executed and is automatically updated after each instruction fetch. PC is cleared to 0000H during reset.

Flag Register (F)

The Flag Register stores the logical state reflecting the results of instruction execution. The contents of the Flag Register are used to control program flow and instruction operation.

Flag Register

Bit	7	6	5	4	3	2	1	0
Bit/Field	S	Z	Not Used	H	Not Used	P/V	N	C
R/W	R/W	R/W	?	R/W	?	R/W	R/W	R/W
Reset	0	0	?	0	?	0	0	0

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	S	R/W	0	**Sign.** S stores the state of the most significant bit (bit 7) of the result. This is useful for operations with signed numbers in which values with bit 7 = 1 are interpreted as negative.

AC Characteristics

This section describes the AC characteristics of the Z8X180 family and absolute maximum rating for these products.

AC CHARACTERISTICS—Z8S180

Table 31. Z8S180 AC Characteristics V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock “H” Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock “L” Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to $\overline{MREQ}$ Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High	5	—	5	—	ns

Table 41. 8-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 8-Bit Data	LD (IX + d),m	11 011 101 00 110 110 <d>	S		D					4	15	$m \rightarrow (IX + d)_M$	•	•	•	•	•	•
	LD (IY + d),m	11 111 101 01 110 g <d> <m>	S		D					4	15	$m \rightarrow (IY + d)_M$	•	•	•	•	•	•
	LD (HL),g	01 110 g				S	D			1	7	$gr \rightarrow (HL)_M$	•	•	•	•	•	•
	LD (IX + d),g	11 011 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IX+d)_M$	•	•	•	•	•	•
	LD (IY + d),g	11 111 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IY + d)_M$	•	•	•	•	•	•
(1) In the case of R1 and Z Mask, interrupts are not sampled at the end of LD A, I or LD A,R.																		

Table 42. 16-Bit Load

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 16-Bit Data	LD ww,mn	00 ww0 001 <n> <m>	S			D				3	9	$mn \rightarrow ww_R$	•	•	•	•	•	•
	LD IX,mn	11 011 101 00 100 001 <n> <m>	S					D		4	12	$mn \rightarrow IX_R$	•	•	•	•	•	•

Table 50. 2nd Op Code Map Instruction Format: ED XX

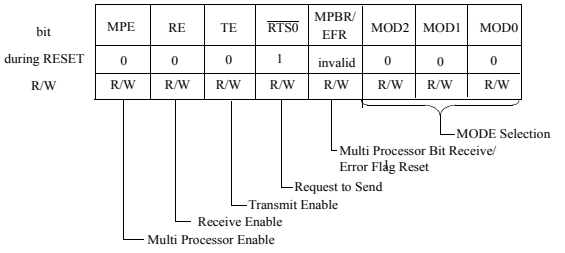
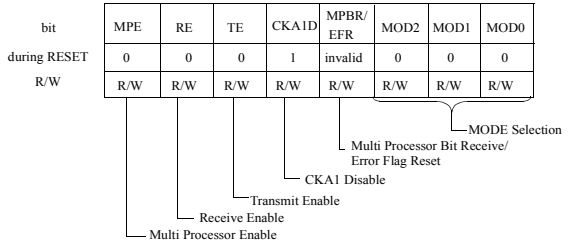
						ww (L0 = ALL)												
						BC	DE	HL	SP									
		G (L0 = 0~7)																
		B	D	H		B	D	H										
HI / LO		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0	IN0 g, (m)				IN g, (C)						LDI	LDIR					0
0001	1	OUT0 (m),g				OUT (C),g						CPI	CPIR					1
0010	2					SBC HL, ww						INI	INIR					2
0011	3					LD (mn), ww				OTIM	OTIM R	OUTI	OTIR					3
0100	4	TST g			TST (HL)	NEG		TST m	TSTIO m									4
0101	5					RETN												5
0110	6					IM 0	IM 1		SLP									6
0111	7					LD I,A	LD A,I	RRD										7
1000	8	IN0 g, (m)				IN g, (C)						LDD	LDDR					8
1001	9	OUT0 (m), g				OUT (C) , g						CPD	CPDR					9
1010	A					ADC HL,ww						IND	INDR					A
1011	B					LD ww, (mn)				OTD M	OTD MR	OUTD	OTDR					B
1100	C	TST g				MLT ww												C
1101	D					RETI												D
1110	E						IM 2											E
1111	F					LDR, A	LD A,R	RLD										F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
		C	E	L	A	C	E	L	A									
		g (L0 = 8~F)																

I/O Registers

INTERNAL I/O REGISTERS

By programming IOA7 and IOA6 as the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

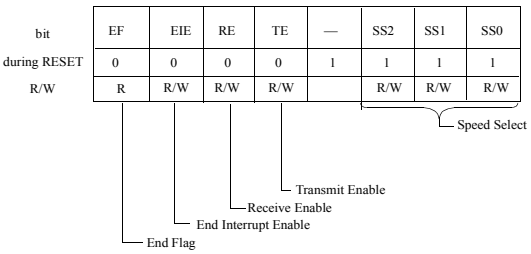
Table 57. Internal I/O Registers

Register	Mnemonics	Address		Remarks
ASCI Control Register A Channel 0:	CNTLA0	0	0	
ASCI Control Register A Channel 1:	CNTLA1	0	1	

MOD 2 1 0
0 0 0 Start + 7 bit Data + 1 Stop
0 0 1 Start + 7 bit Data + 2 Stop
0 1 0 Start + 7 bit Data + Parity + 1 Stop
0 1 1 Start + 7 bit Data + Parity + 2 Stop
1 0 0 Start + 8 bit Data + 1 Stop
1 0 1 Start + 8 bit Data + 2 Stop
1 1 0 Start + 8 bit Data + Parity + 1 Stop
1 1 1 Start + 8 bit Data + Parity + 2 Stop

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Transmit Data Register Channel 0:	TDR0	0	6	
ASCI Transmit Data Register Channel 1:	TDR1	0	7	
ASCI Receive Data Register Channel 0:	TSR0	0	8	
ASCI Receive Data Register Channel 1:	TSR1	0	9	
CSI/O Control Register:	CNTR	0	A	



SS2 1 0	Baud Rate	SS2 1 0	Baud Rate
0 0 0	Phi ÷ 20	1 0 0	Phi ÷ 320
0 0 1	÷ 40	1 0 1	÷ 640
0 1 0	÷ 80	1 1 0	÷ 1280
0 1 1	÷ 160	1 1 1	External frequency < ÷ 20)

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.