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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010psg

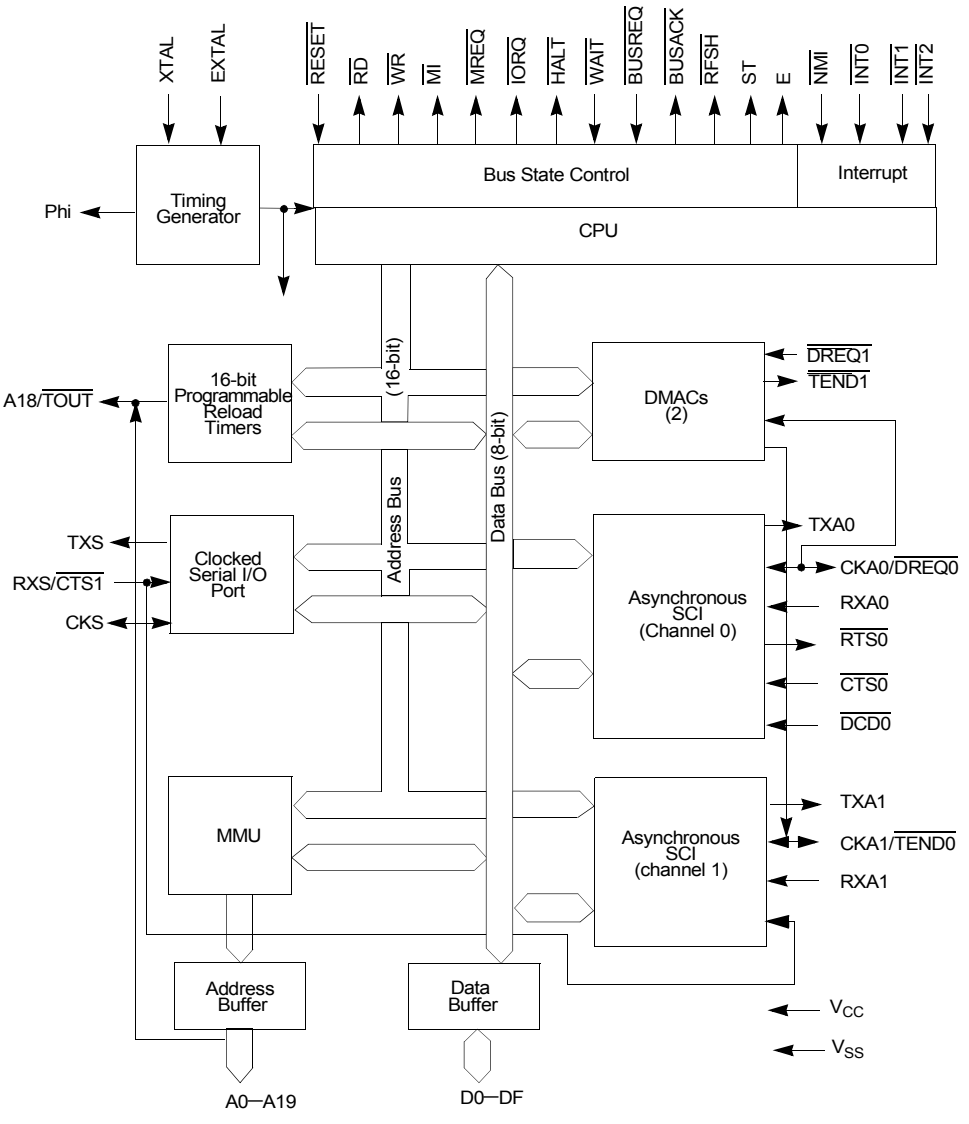


Figure 4. Z80180/Z8S180/Z8L180 Block Diagram

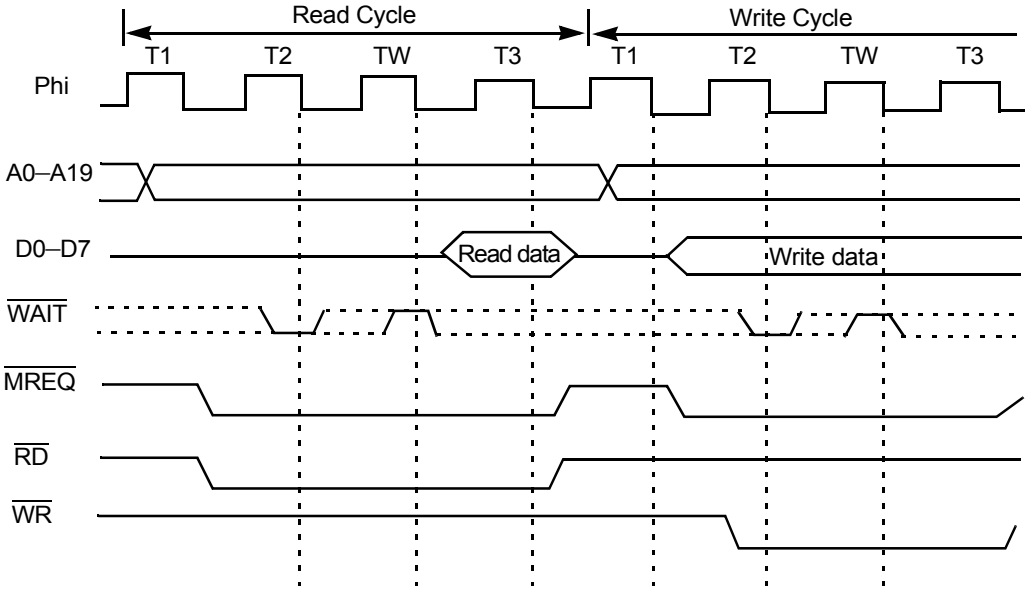


Figure 12. Memory Read/Write (with Wait State) Timing Diagram

I/O Read/Write Timing

I/O Read/Write operations differ from memory Read/Write operations in the following three ways:

- The $\overline{\text{IORQ}}$ (I/O Request) signal is asserted Low instead of the $\overline{\text{MREQ}}$ signal
- The 16-bit I/O address is not translated by the MMU
- A16–A19 are held Low

At least one Wait State (TW) is always inserted for I/O read and write cycles (except internal I/O cycles).

Figure 13 illustrates I/O read/write timing with the automatically inserted Wait State (TW).

The external bus is IDLE while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing

Figure 15 depicts the Z8X180 hardware RESET timing. If the $\overline{\text{RESET}}$ pin is Low for six or more clock cycles, processing is terminated and the Z8X180 restarts execution from (logical and physical) address `00000H`.

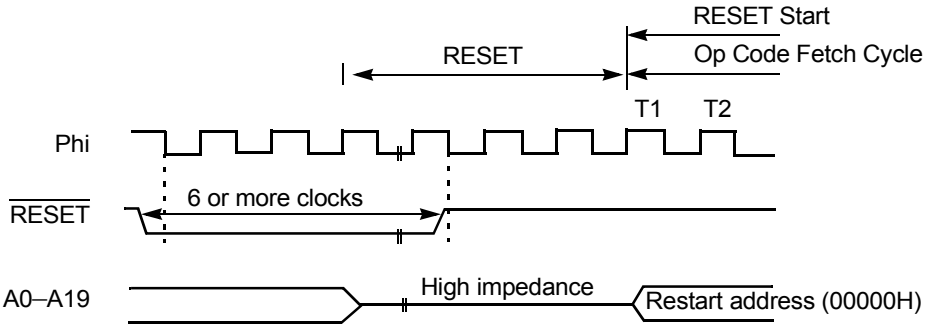


Figure 15. RESET Timing Diagram

$\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ Bus Exchange Timing

The Z8X180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{\text{BUSREQ}}$ (Bus Request) input Low. After the Z8X180 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{\text{BUSACK}}$ (Bus Acknowledge) output Low.

The bus may be released by the Z8X180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of three clock cycles (more if wait states are inserted) for Op Code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

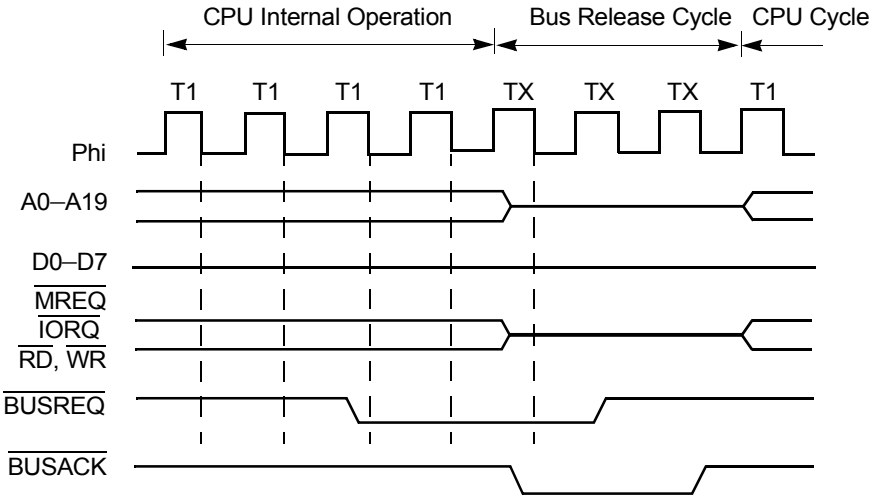


Figure 17. Bus Exchange Timing During CPU Internal Operation

Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z8X180 uses Wait States (TW) to extend bus cycle timing. A Wait State(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (TW) generator. Wait States (TW) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted Low, Wait State(s) (TW) are inserted between T2 and T3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T2 or TW. If the $\overline{\text{WAIT}}$ input is asserted Low at the falling edge of the system clock in TW, another TW is inserted into the bus cycle.

Note: $\overline{\text{WAIT}}$ input transitions must meet specified setup and hold times. This specification can easily be accomplished by

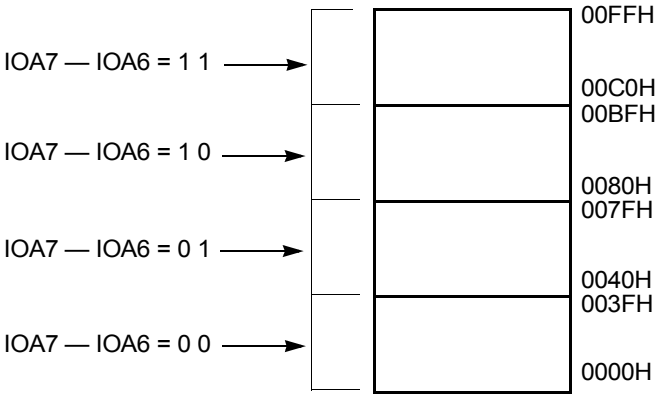


Figure 22. I/O Address Relocation

Internal I/O Registers Address Map

The internal I/O register addresses are described in Table 6 and Table 7. These addresses are relative to the 64-byte boundary base address specified in ICR.

I/O Addressing Notes

The internal I/O register addresses are located in the I/O address space from `0000H` to `00FFH` (16-bit I/O addresses). Thus, to access the internal I/O registers (using I/O instructions), the high-order 8 bits of the 16-bit I/O address must be `0`.

The conventional I/O instructions (OUT (m), A/IN A, (m) / OUTI/INI, for example) place the contents of a CPU register on the high-order 8 bits of the address bus, and thus may be difficult to use for accessing internal I/O registers.

For efficient internal I/O register access, a number of new instructions have been added, which force the high-order 8 bits of the 16-bit I/O

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
INT	IL Register (Interrupt Vector Low Register)	IL	XX110011	33H	67
	INT/TRAP Control Register	ITC	XX110100	34H	68
	Reserved		XX110101	35H	
Refresh	Refresh Control Register	RCR	XX110110	36H	88
	Reserved		XX110111	37H	
MMU	MMU Common Base Register	CBR	XX111000	38H	61
	MMU Bank Base Register	BBR	XX111001	39H	62
	MMU Common/Bank Area Register	CBAR	XX111010	3AH	60
I/O	Reserved		XX111011	3BH	
			↕	↕	
			XX111101	3DH	
	Operation Mode Control Register	OMCR	XX111110	3EH	15
	I/O Control Register	ICR	XX111111	3FH	42

If IEF1 is 0, all maskable interrupts are disabled. IEF1 can be reset to 0 by the DI (Disable Interrupts) instruction and set to 1 by the El (Enable Interrupts) instruction.

The purpose of IEF2 is to correctly manage the occurrence of $\overline{\text{NMI}}$. During $\overline{\text{NMI}}$, the prior interrupt reception state is saved and all maskable interrupts are automatically disabled (IEF1 copied to IEF2 and then IEF1 cleared to 0). At the end of the $\overline{\text{NMI}}$ interrupt service routine, execution of the RETN (Return from Non-maskable Interrupt) automatically restores the interrupt receiving state (by copying IEF2 to IEF1) prior to the occurrence of $\overline{\text{NMI}}$.

Table 8 describes how the IEF2 state can be reflected in the P/V bit of the CPU Status Register by executing LD A, I or LD A, R instructions.

Table 8. State of IEF1 and IEF2

CPU Operation	IEF1	IEF2	REMARKS
RESET	0	0	Inhibits the interrupt except $\overline{\text{NMI}}$ and TRAP.
NMI	0	IEF1	Copies the contents of IEF1 to IEF2
RETN	IEF2	not affected	Returns from the $\overline{\text{NMI}}$ service routine.
Interrupt except $\overline{\text{NMI}}$ end TRAP	0	0	Inhibits the interrupt except $\overline{\text{NMI}}$ end TRAP
RETI	not affected	not affected	
TRAP	not affected	not affected	
EI	1	1	

DMA Destination Address Register Channel 0 (DAR0 I/O Address = 23H to 25H)

Specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024KB memory addresses or up to 64KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O.

DMA Byte Count Register Channel 0 (BCR0 I/O Address = 26H to 27H)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one. If *n* bytes are transferred, *n* is stored before the DMA operation.

DMA Memory Address Register Channel 1 (MAR1: I/O Address = 28H to 2AH)

Specifies the physical memory address for channel 1 transfers. This address may be a destination or source memory address. The register contains 20 bits and may specify up to 1024KB memory address.

DMA I/O Address Register Channel 1 (IAR1: I/O Address = 2BH to 2CH)

Specifies the I/O address for channel 1 transfers. This address may be a destination or source I/O address. The register contains 16 bits and may specify up to 64KB I/O addresses.

DMA Byte Count Register Channel 1 (BCR1: I/O Address = 2EH to 2FH)

Specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64KB transfers. When one byte is transferred, the register is decremented by one.

DMA Status Register (DSTAT)

DSTAT is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also determines DMA transfer status, that is, completed or in progress.

DMA Status Register (DSTAT: 30H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	DE1	DE0	$\overline{\text{DWE1}}$	$\overline{\text{DWE0}}$	DIE1	DIE0	?	DME
R/W	R/W	R/W	W	W	R/W	R/W	?	R
Reset	0	0	1	1	0	0	?	

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	DE1	R/W		**Enable Channel 1** — When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU. To perform a software write to DE1, DWE1 is written with 0 during the same register write access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DME (DMA Main Enable) to 1. DE1 is cleared to 0 during RESET.

$\overline{\text{DREQ0}}$ for ASCI transmission and reception respectively. To initiate memory to/from ASCI DMA transfer, perform the following operations:

1. Load the source and destination addresses into SAR0 and DAR0 Specify the I/O (ASCI) address as follows:
   a. Bits A0–A7 must contain the address of the ASCI channel transmitter or receiver (I/O addresses 6H-9H).
   b. Bits A8–A15 must equal 0.
   c. Bits SAR17–SAR16 must be set according to Table 16 to enable use of the appropriate ASCI status bit as an internal DMA request.

Table 16. DMA Transfer Request

SAR18	SAR17	SAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	RDRF (ASCI channel 0)
X	1	0	RDRF (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

DAR18	DAR17	DAR16	DMA Transfer Request
X	0	0	$\overline{\text{DREQ0}}$
X	0	1	TDRE (ASCI channel O)
X	1	0	TDRE (ASCI channel 1)
X	1	1	Reserved
Note: X = Don't care			

Table 17. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit date + 2 Stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit date + parity + 2 stop

ASCI Control Register B0, 1 (CNTLB0, 1)

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

Timer Data Register 0L (TMDR0L: 0CH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Data Register 0H (TMDR0H: 0DH)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Data							
R/W	R/W							
Reset	0							
Note: R = Read W = Write X = Indeterminate ? = Not Applicable								

Timer Reload Register (RLDR: I/O Address = CH0: 0EH, 0FH, CHI, 16H, 17H)

PRT0 and PRT1 each contain 16-bit Timer Reload Registers (RLDR). RLDR0 and RLDR1 are each accessed as low and high byte registers (RLDR0H, RLDR0L and RLDR1H, RLDR1L). During RESET, RLDR0 and RLDR1 are set to FFFFH

When the TMDR counts down to 0, it is automatically reloaded with the contents of RLDR.

Bit Position	Bit/Field	R/W	Value	Description
7–6	TIF1–0	R		**TIF1: Timer Interrupt Flag** — When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0. When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.
5–4	TIE1–0	R/W		**Timer Interrupt Enable** — When TIE1 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE1 is reset to 0, the interrupt request is inhibited. During RESET, TIE1 is cleared to 0. When TIE0 is set to 1, TIF0 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.
3–2	TOC1–0	R/W		**Timer Output Control** — TOC1, and TOC0 control the output of PRT1 using the multiplexed A18/TOUT pin as shown in Table 23. During RESET, TOC1 and TOC0 are cleared to 0. This selects the address function for A18/TOUT. By programming TOC1 and TOC0 the A18/TOUT pin can be forced HIGH, LOW, or toggled when TMDR1 decrements to 0. Reference Table 23.
1–0	TDE1–0	R/W		**Timer Down Count Enable** — TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0 respectively. When TDEn (n = 0, 1) is set to 1, down counting is executed for TMDRn. When TDEn is reset to 0, down counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

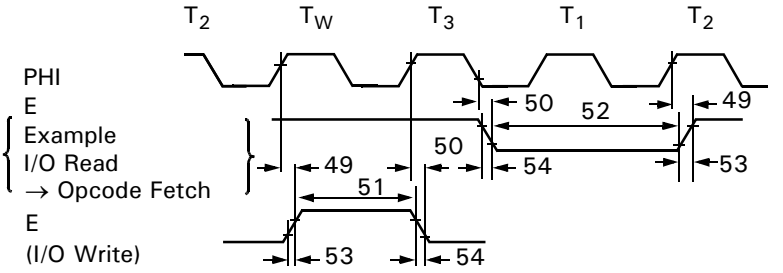


Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

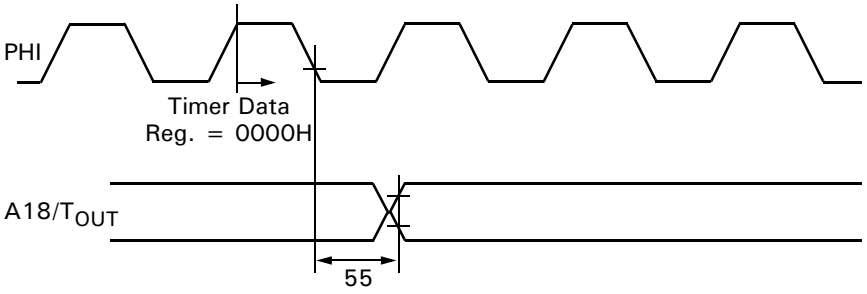


Figure 88. Timer Output Timing

Table 38. Arithmetic and Logical Instructions (8-bit) (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
AND	AND g	10 100 g				S		D		1	4	Ar*gr→Ar	↑	↑	S	P	R	R
	AND (HL)	10 100 110					S	D		1	6	Ar*$(HL)_M$→Ar	↑	↑	S	P	R	R
	AND m	11 100 110	S					D		2	6	Ar*m→Ar	↑	↑	S	P	R	R
		<m>																
	AND (IX + d)	11 011 101			S			D		3	14	Ar*$(1X + d))_M$→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
	AND (IY + d)	11 111 101			S			D		3	14	Ar*(1Y + d)v→Ar	↑	↑	S	P	R	R
		10 100 110																
		<d>																
Compare	CP g	10 111 g				S		D		1	4	Ar-gr	↑	↑	↑	V	S	↑
	CP (HL)	10 111 110					S	D		1	6	Ar-$(HL)_M$	↑	↑	↑	V	S	↑
	CP m	11 111 110	S					D		2	6	Ar-m	↑	↑	↑	V	S	↑
		<m>																
	CP (IX + d)	11 011 101		S				D		3	14	Ar-$(IX + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
	CP (IY + d)	11 111 101		S				D		3	14	Ar-$(IY + d))_M$	↑	↑	↑	V	S	↑
		10 111 110																
		<d>																
Complement	CPL	00 101 111						S/D		1	3	$\overline{Ar}$→Ar	•	•	S	•	S	•

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes

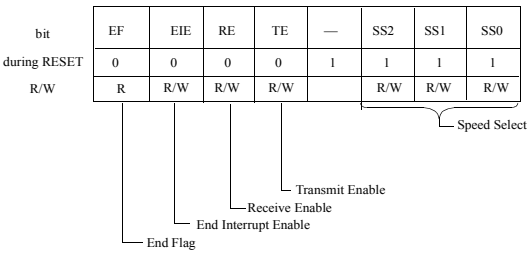
Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
$\overline{WAIT}$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{BUSACK}$	—	1	OUT	OUT	OUT
$\overline{BUSREQ}$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{RESET}$	—	0	IN (A)	IN (A)	IN (A)
$\overline{NMI}$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_0$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_1$	—	IN (N)	IN (A)	IN (A)	IN (A)
$\overline{INT}_2$	—	IN (N)	IN (A)	IN (A)	IN (A)
ST	—	1	1	OUT	1
A0–A17, A19	—	Z	1	A	1
A18/TOUT	A18	Z	1	A	1
	TOUT	Z	OUT	H	H
D0–D7	—	Z	Z	A	Z
$\overline{RTS}$0	—	1	H	OUT	H
$\overline{CTS}$0	—	IN (N)	IN (A)	IN (N)	N (N)
$\overline{DCD}$0	—	IN (N)	IN (A)	IN (N)	IN (N)
TXA0	—	1	OUT	H	H
RXA0	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA0/$\overline{DREQ}$0	CKA0 (Internal Clock Mode)	Z	OUT	Z	Z

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
	CKA0 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{DREQ0}}$	Z	IN (N)	IN (A)	IN (N)
TXA1	—	1	OUT	H	H
RXA1	—	IN (N)	IN (A)	IN (N)	IN (N)
CKA1/$\overline{\text{TEND0}}$	CKA1 (Internal Clock Mode)	Z	OUT	Z	Z
	CKA1 (External Clock Mode)	Z	IN (A)	IN (N)	IN (N)
	$\overline{\text{TEND0}}$	Z	1	OUT	1
TXS	—	1	OUT	H	H
RXS/$\overline{\text{CTS}}_1$	RXS	IN (N)	IN (A)	IN (N)	IN (N)
	$\overline{\text{CTS1}}$	IN (N)	IN (A)	IN (N)	IN (N)
CKS	CKS (Internal Clock Mode)	Z	OUT	1	1
	CKS (External Clock Mode)	Z	IN (A)	Z	Z
$\overline{\text{DREQ}}_1$	—	IN (N)	IN (N)	IN (A)	IN (N)
$\overline{\text{TEND}}_1$	—	1	1	OUT	1
$\overline{\text{HALT}}$	—	1	0	OUT	0
$\overline{\text{RFSH}}$	—	1	1	OUT	1
$\overline{\text{IORQ}}$	—	1	1	OUT	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Transmit Data Register Channel 0:	TDR0	0	6	
ASCI Transmit Data Register Channel 1:	TDR1	0	7	
ASCI Receive Data Register Channel 0:	TSR0	0	8	
ASCI Receive Data Register Channel 1:	TSR1	0	9	
CSI/O Control Register:	CNTR	0	A	



SS2 1 0	Baud Rate	SS2 1 0	Baud Rate
0 0 0	Phi ÷ 20	1 0 0	Phi ÷ 320
0 0 1	÷ 40	1 0 1	÷ 640
0 1 0	÷ 80	1 1 0	÷ 1280
0 1 1	÷ 160	1 1 1	External frequency < ÷ 20)

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
Timer Data Register Channel 1L:	TMDR1L	1	4	
Timer Data Register Channel 1H:	TMDR1H	1	5	
Timer Reload Register Channel 1L	RLDR1L	1	6	
Timer Reload Register Channel 1H:	RLDR1H	1	7	
Free Running Counter:	FRC	1	8	Read only
DMA Source Address Register Channel 0L:	SAR0L	2	0	
DMA Source Address Register Channel 0H:	SAR0H	2	1	
DMA Source Address Register Channel 0B:	SAR0B	2	2	Bits 0-2 (3) are used for SAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — RDR0 (ASCI0) X X 1 0 — RDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Destination Address Register Channel 0L:	DAR0L	2	3	
DMA Destination Address Register Channel 0H:	DAR0H	2	4	
DMA Destination Address Register Channel 0B:	DAR0B	2	5	Bits 0-2 (3) are used for DAR0B A_{19}*, A_{18}, A_{17}, A_{16} X X 0 0 — $\overline{DREQ}_0$ (external) X X 0 1 — TDR0 (ASCI0) X X 1 0 — TDR1 (ASCI1) X X 1 1 — Not used DMA Transfer Request
DMA Byte Count Register Channel 0L:	BCROL	2	6	
DMA Byte Count Register Channel 0H:	BCROH	2	7	
DMA Memory Address Register Channel 1L:	MAR1L	2	8	
DMA Memory Address Register Channel 1H:	MAR1H	2	9	

* In the R1 and Z mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68.

ORDERING INFORMATION

Codes

- Package
  P = Plastic Dip
  V = Plastic Chip Carrier
  F = Quad Flat Pack
- Temperature
  S = 0°C to +70°C
  E = -40°C to 100°C
- Speed
  06 = 6 MHz
  08 = 8 MHz
  10 = 10 MHz
- Environmental
  C = Plastic Standard
- Example
  Z8018008PSC is an 80180 8 MHz, Plastic DIP, 0°C to 70°C, Plastic Standard Flow.