Zilog - Z8018010VEC Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010vec

Z8018x
Family MPU User Manual

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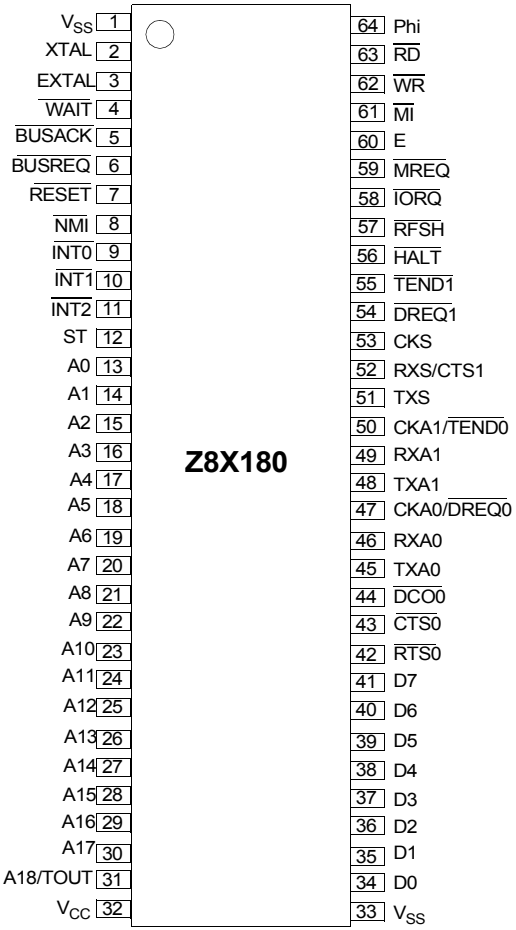

Figure 1. 64-Pin DIP

TOUT. *Timer Out (Output, Active High).* TOUT is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. *Transmit Data 0 and 1 (Outputs, Active High).* These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. *Clocked Serial Transmit Data (Output, Active High).* This line is the transmitted data from the CSIO channel.

$\overline{\text{WAIT}}$. *Wait (Input; Active Low).* $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The $\overline{\text{WAIT}}$ input is sampled on the falling edge of T2 (and subsequent Wait States). If the input is sampled Low, then additional Wait States are inserted until the $\overline{\text{WAIT}}$ input is sampled High, at which time execution continues.

$\overline{\text{WR}}$. *Write (Output, Active Low, 3-state).* $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. *Crystal (Input, Active High). Crystal oscillator connection.* This pin must be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

Multiplexed pins are described in Table 2.

The external bus is IDLE while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing

Figure 15 depicts the Z8X180 hardware RESET timing. If the $\overline{\text{RESET}}$ pin is Low for six or more clock cycles, processing is terminated and the Z8X180 restarts execution from (logical and physical) address `00000H`.

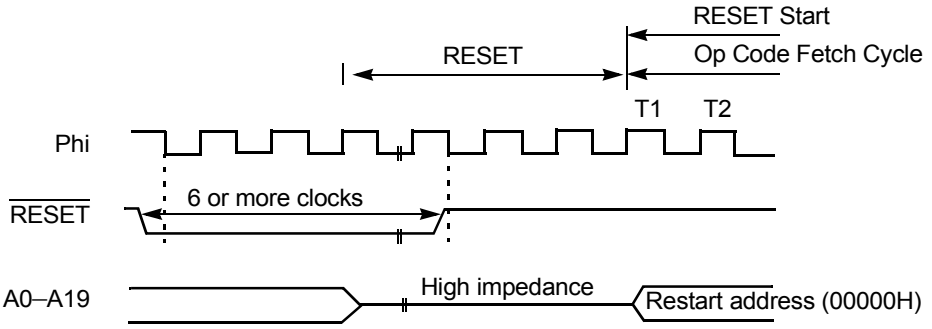

Figure 15. RESET Timing Diagram

$\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ Bus Exchange Timing

The Z8X180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{\text{BUSREQ}}$ (Bus Request) input Low. After the Z8X180 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{\text{BUSACK}}$ (Bus Acknowledge) output Low.

The bus may be released by the Z8X180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of three clock cycles (more if wait states are inserted) for Op Code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

If the Global Interrupt Enable Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180/Z8L180-class processors to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

- The interrupt input follows the normal interrupt daisy-chain protocol
- The interrupt source is active until the acknowledge cycle is complete

If the Global Interrupt Enable Flag IEF1 is disabled (reset to 0) and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input still causes the Z8S180/Z8L180-class processors to exit STANDBY mode. The CPU proceeds to fetch and execute instructions that follow the SLEEP instruction when clocking resumes.

If the Extend Maskable Interrupt input is not active until clocking resumes, the Z8S180/Z8L180-class processors do not exit STANDBY mode. If the Non-Maskable Interrupt ($\overline{\text{NMI}}$) is not active until clocking resumes, the Z8S180/Z8L180-class processors still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because $\overline{\text{NMI}}$ is edge-triggered. The condition is latched internally when $\overline{\text{NMI}}$ is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180/ Z8L180-class processors.

1. Set bits 6 and 3 to `0` and `1`, respectively.
2. Set the I/O STOP bit (bit 5 of ICR, I/O Address = `3FH` to 1.
3. Execute the SLEEP instruction

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, using RESET, BUS REQUEST or EXTERNAL INTERRUPTS,

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
INT	IL Register (Interrupt Vector Low Register)	IL	XX110011	33H	67
	INT/TRAP Control Register	ITC	XX110100	34H	68
	Reserved		XX110101	35H	
Refresh	Refresh Control Register	RCR	XX110110	36H	88
	Reserved		XX110111	37H	
MMU	MMU Common Base Register	CBR	XX111000	38H	61
	MMU Bank Base Register	BBR	XX111001	39H	62
	MMU Common/Bank Area Register	CBAR	XX111010	3AH	60
I/O	Reserved		XX111011	3BH	
			↕	↕	
			XX111101	3DH	
	Operation Mode Control Register	OMCR	XX111110	3EH	15
	I/O Control Register	ICR	XX111111	3FH	42

MMU Common Base Register (CBR)

CBR specifies the base address (on 4K boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register (CBR: 38H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7–0	CB7–0	R/W		CBR specifies the base address (on 4KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses.

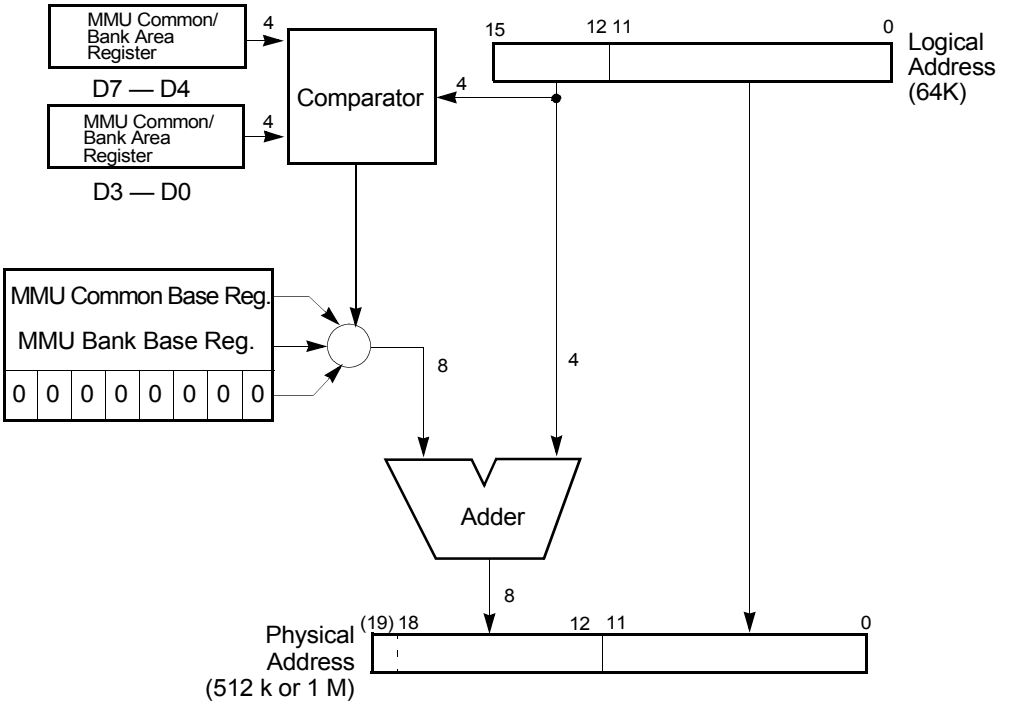

Figure 29. Physical Address Generation

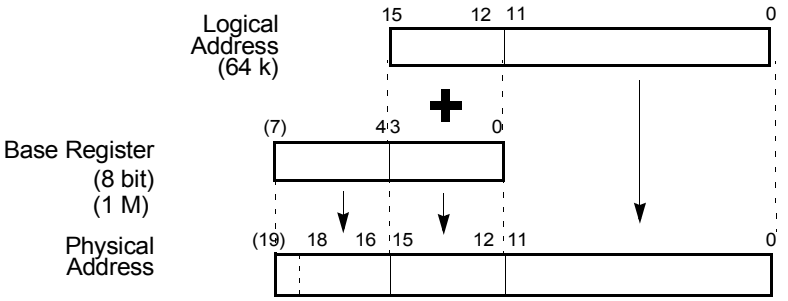

Figure 30. Physical Address Generation 2

Bit Position	Bit/Field	R/W	Value	Description
2-0		R/W	000	DMA1 ext TOUT/DREQ
			001	DMA1 ASCI0
			010	DMA1 ASCI1
			011	DMA1 ESCC
			111	DMA1 PIA27-20 (P1284)

DMA Register Description

Bit 7

This bit must be set to 1 only when both DMA channels are set to take their requests from the same device. If this bit is 1 (it resets to 0), the TEND output of DMA channel o sets a flip-flop, so that thereafter the device's request is visible to channel 1, but not visible to channel 0. The internal TEND signal of channel 1 clears the FF, so that thereafter, the device's request is visible to channel 0, but no visible to channel 1.

If DMA request are from differing sources, DMA channel 0 request is forced onto DMA channel 1 after TEND output of DMA channel 0 sets the flop-flop to alternate.

Bit 6

When both DMA channels are programmed to take their requests from the same device, this bit (FF mentioned in the previous paragraph) controls which channel the device's request is presented to: 0 = DMA0, 1 = DMA l. When Bit 7 is 1, this bit is automatically toggled by the channel end output of the channels.

rising edge of the clock prior to T3 at which time the DMA operation (re)starts. Figure 48 depicts the edge-sense DMA timing.

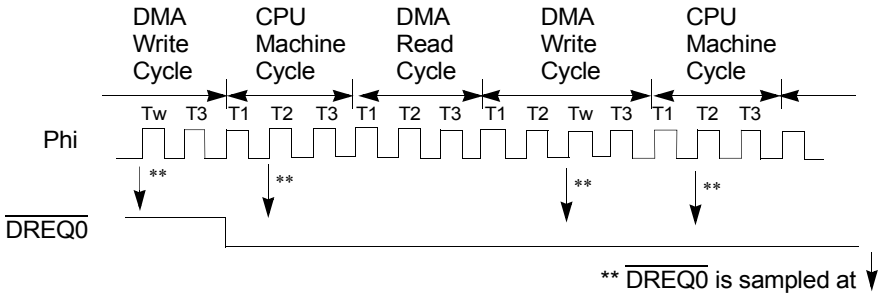

Figure 48. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Edge-Sense

During the transfers for channel 0, the $\overline{\text{TEND0}}$ output goes Low synchronous with the write cycle of the last (BCR0 = 00H) DMA transfer (Reference Figure 49).

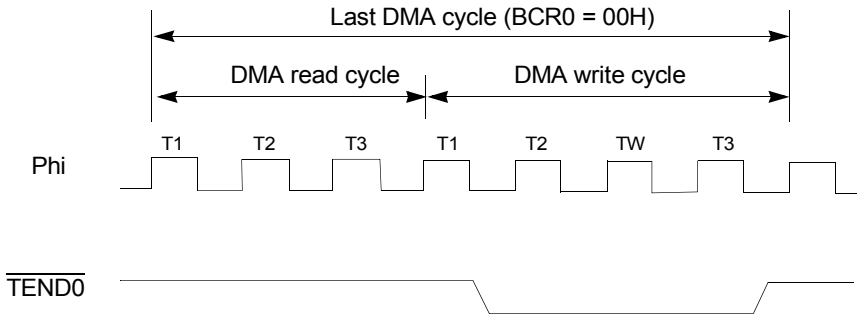

Figure 49. $\overline{\text{TEND0}}$ Output Timing Diagram

The $\overline{\text{DREQ0}}$ and $\overline{\text{TEND0}}$ pins are programmably multiplexed with the CKA0 and CKA1 ASCI clock input/outputs. However, when DMA channel 0 is programmed for memory to/from I/O (and memory to/from

return accurate data without requiring the timer to be stopped. The write procedure requires the PRT to be stopped.

For reading (without stopping the timer), TMDR is read in the order of lower byte - higher byte (TMDRnL, TMDRnH). The lower byte read (TMDRnL) stores the higher byte value in an internal register. The following higher byte read (TMDRnH) accesses this internal register. This procedure insures timer data validity by eliminating the problem of potential 16-bit timer updating between each 8-bit read. Specifically, reading TMDR in higher byte–lower byte order may result in invalid data. Note the implications of TMDR higher byte internal storage for applications which may read only the lower and/or higher bytes. In normal operation all TMDR read routines must access both the lower and higher bytes, in that order. For writing, the TMDR down counting must be inhibited using the TDE (Timer Down Count Enable) bits in the TCR (Timer Control Register). Then, any or both higher and lower bytes of TMDR can be freely written (and read) in any order.

CSI/O Transmit/Receive Data Register (TRDR: I/O Address = 0BH).

TRDR is used for both CSI/O transmission and reception. Thus, the system design must insure that the constraints of half-duplex operation are met (Transmit and receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, the CSI/O does not work.

TRDR is not buffered. Attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in progress. Similarly, reading TRDR during a transmit or receive must be avoided.

DC Characteristics

This section describes the DC characteristics of the Z8X180 family and absolute maximum rating for these products.

ABSOLUTE MAXIMUM RATING

Table 27. Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply Voltage	Vcc	- 0.3 ~ + 7.0	V
Input Voltage	Vin	-0.3 ~ Vcc+0.3	V
Operating Temperature	Topr	0 ~ 70	°C
Extended Temperature	Text	-40 ~ 85	°C
Storage Temperature	Tstg	- 55 ~ +150	°C

Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of IC.

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns
32	t_{INTH}	$\overline{INT}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{BUSACK}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{BUSACK}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{RFSH}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{RFSH}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{HALT}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{HALT}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{TENDi}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{TENDi}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns

Timing Diagrams

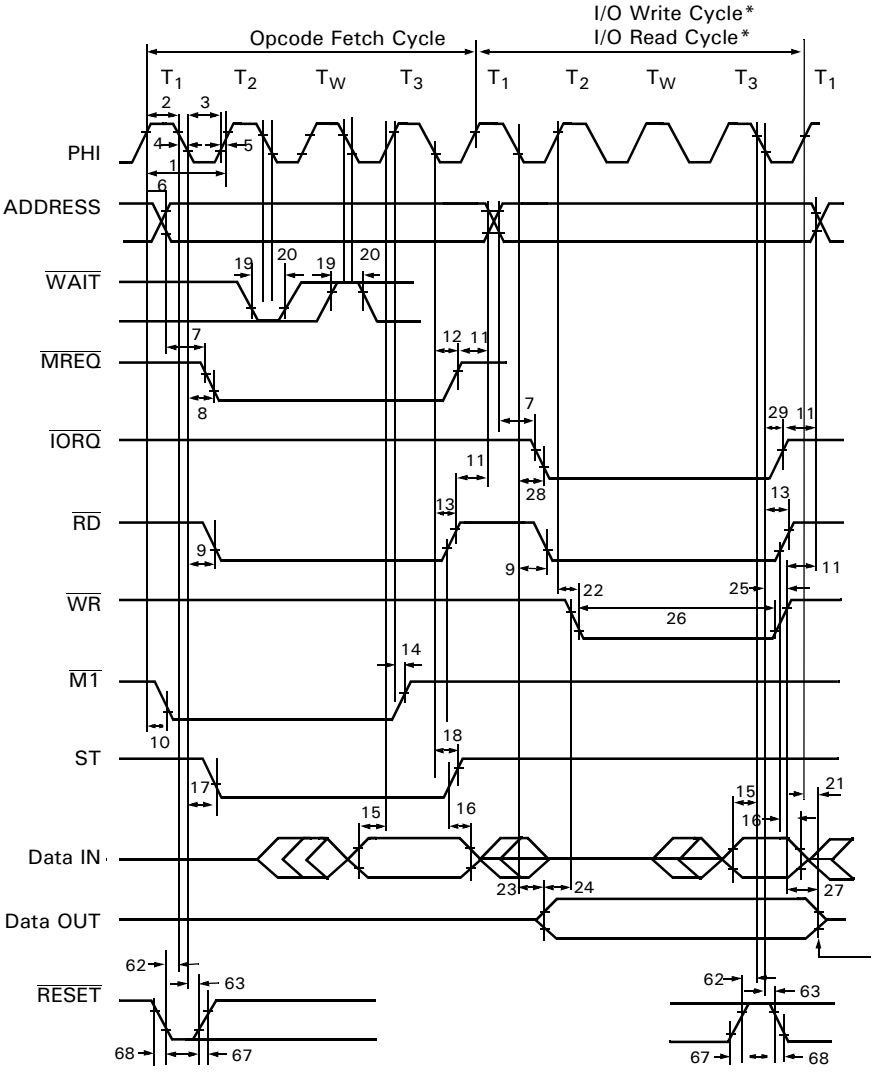

Figure 81. AC Timing Diagram 1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
CPI CPD	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4 ~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R \neq 0$ and $Ar = (HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC8	TiTiTi TiTi	*	Z	1	1	1	1	1	1	1
CPIR CPDR (If $BC_R=0$ or $Ar=(HL)_M$)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
CPL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
DAA	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
DI*1	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
* 1 Interrupt request is not sampled.											

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
EX (SP),IX EX (SP),IY	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC4	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
	MC5	Ti	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	SP+1	IXH IYH	1	0	0	1	1	1	1
	MC7	T1T2T3	SP	IXL IYL	1	0	0	1	1	1	1
HALT	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	—	—	Next Op Code Address	Next Op Code	0	1	0	1	0	0	0
IM0 IM1 IM2	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
INC g DEC g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
INC (HL) DEC (HL)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	HL	DATA	0	1	0	1	1	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
TST g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
TST m**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
TST (HL)**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	2	0	2	0	2	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T23	HL	Data	0	1	0	1	1	1	1

Status Signals

PIN OUTPUTS IN EACH OPERATING MODE

Table 55 describes pin outputs in each operating mode.

Table 55. Pin Outputs in Each Operating Mode

Mode		$\overline{M1}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{RD}$	$\overline{WR}$	$\overline{RFSH}$	$\overline{HALT}$	$\overline{BUSACK}$	ST	Address BUS	Data BUS
CPU Operation	Op Code Fetch (1st Op Code)	0	0	1	0	1	1	1	1	0	A	IN
	Op Code Fetch (except 1 st Op Code)	0	0	1	0	1	1	1	1	1	A	IN
	MemRead	1	0	1	0	1	1	1	1	1	A	IN
	Memory Write	1	0	1	1	0	1	1	1	1	A	OUT
	I/O Read	1	1	0	0	1	1	1	1	1	A	IN
	I/O Write	1	1	0	1	0	1	1	1	1	A	OUT
	Internal Operation	1	1	1	1	1	1	1	1	1	A	IN
Refresh		1	0	1	1	1	0	1	1	*	A	IN
Interrupt Acknowledge Cycle (1st Machine Cycle)	$\overline{NMI}$	0	0	1	0	1	1	1	1	0	A	IN
	$\overline{INT0}$	0	1	0	1	1	1	1	1	0	A	IN
	$\overline{INT1}$, $\overline{INT2}$ & Internal Interrupts	1	1	1	1	1	1	1	1	0	A	IN
BUS RELEASE		1	Z	Z	Z	Z	1	1	0	*	Z	IN
HALT		0	0	1	0	1	1	0	1	0	A	IN
SLEEP		1	1	1	1	1	1	0	1	1	1	IN

Table 56. Pin Status During RESET and LOW POWER OPERATION Modes (Continued)

Symbol	Pin Function	Pin Status in Each Operation Mode			
		RESET	SLEEP	IOSTOP	SYSTEM STOP
$\overline{\text{MREQ}}$	—	1	1	OUT	1
E	—	0	E Clock Output	←	←
$\overline{\text{M1}}$	—	1	1	OUT	1
$\overline{\text{WR}}$	—	1	1	OUT	1
$\overline{\text{RD}}$	—	1	1	OUT	1
Phi	—	Phi Clock Output	←	←	←

- 1: HIGH 0: LOW A: Programmable Z: High Impedance
- IN (A): Input (Active) IN (N): Input (Not active) OUT: Output
- H: Holds the previous state
- ←: same as the left