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Zilog - Z8018010VEC00TR Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010vec00tr

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2

on-chip memory management unit (MMU) with the capability of addressing up to 1 MB of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several *glue* functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z8X180 consume a low amount of power during normal operation, but processors with Z8S180 and Z8L180 class processors also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a *stopped* state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a *stopped* state, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z8X180 provides an excellent solution to system applications requiring high performance, and low power operation.

Figures 1 through 3 illustrate the three pin packages in the Z8X180 MPU family:

- 64-Pin Dual In-line Package (DIP), Figure 1
- 68-Pin Plastic Leaded Chip Carrier (PLCC), Figure 2
- 80-Pin Quad Flat Pack (QFP), Figure 3

Pin out package descriptions for other Z8X180-based products are covered in their respective product specifications.

Figure 4 depicts the block diagram that is shared throughout all configurations of the Z8X180.

Bit Position	Bit/Field	R/W	Value	Description
2-0		R/W	000 001 010 011 111	DMA1 ext TOUT/DREQ DMA1 ASCI0 DMA1 ASCI1 DMA1 ESCC DMA1 PIA27-20 (P1284)

DMA Register Description

Bit 7

This bit must be set to 1 only when both DMA channels are set to take their requests from the same device. If this bit is 1 (it resets to 0), the TEND output of DMA channel o sets a flip-flop, so that thereafter the device's request is visible to channel 1, but not visible to channel 0. The internal TEND signal of channel 1 clears the FF, so that thereafter, the device's request is visible to channel 0, but no visible to channel 1.

If DMA request are from differing sources, DMA channel 0 request is forced onto DMA channel 1 after TEND output of DMA channel 0 sets the flop-flop to alternate.

Bit 6

When both DMA channels are programmed to take their requests from the same device, this bit (FF mentioned in the previous paragraph) controls which channel the device's request is presented to: 0 = DMA0, 1 = DMA l. When Bit 7 is 1, this bit is automatically toggled by the channel end output of the channels.



208

Table 33.Bit Values

b	Bit
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

CONDITION

f specifies the condition in program control instructions. Table 34 describes the correspondence between **f** and conditions.

Table 34.Instruction Values

f	Co	ondition
000	NZ	Nonzero
001	Z	Zero
010	NC	Non Carry
011	С	Carry
100	PO	Parity Odd
101	PE	Parity Even
110	Р	Sign Plus
111	М	Sign Minus



220

															F	lags		
					Add	Iress	ing						7	6	4	2	1	0
Operation Name	Mnemonics	Op Code	Immed	Ext	Ind	Reg	Regi	Imp	Rel	Bytes	State s	Operation	s	z	н	P/V	N	с
Bit Reset	RES b,(IY + d)	11 011 101			S/D					4	19	0→b•(IY + d) _M	•	•	•	•	•	•
		11 001 011																
		<d></d>																
		10 b 110																
Bit Test	BIT b, g	11 001 011				S				2	6	b∙gr→z	Х	↑	s	Х	R	•
		01bg																
	BIT b,(HL)	11 001 011					s			2	9	b•(HL) _M →z	х	↑	s	х	R	•
		01 b 110																
	BIT b,(IX + d)	11 011 101			s					4	15	b•(IX + d) _M →z	х	↑	s	х	R	•
		11 001 011																
		<d></d>																
		01 b 110																
	BIT b,(IY + d)	11 111 101			s					4	15	b•(IY + d) _M →z	х	↑	s	х	R	•
		11 001 011																
		<d></d>																
		01 b 110																ĺ

Table 39. Rotate and Shift Instructions (Continued)



															F	lag	s		
					Add	dressi	ng						7	6	4	2	1	1	0
Operation Name	Mnemonics	Op Code	Immed	Ext	Ind	Reg	Regl	Imp	Rel	Bytes	States	Operation	s	z	н	P/	v١	N	С
Load	LD (mn),HL	00 100 010		D				s		3	16	Hr→(mn + 1) _M	•	•	•	•	•	•	•
Data		<n></n>										Lr→(mn) _M							
		<m></m>																	
	LD (mn),IX	11 011 101		D				S		4	19	IXHr-(mn + 1) _M	•	•	•	•	•	•	•
		00 100 010										IXLr→(mn) _M							
		<n></n>																	
		<m></m>																	
	LD (mn),IY	11 111 101		D				s		4	19	IYHr→(mn + 1) _M	•	•	•	•	•	•	•
		00 100 010										IYLr→(mn) _M							
		<n></n>																	
		<m></m>																	

 Table 42.
 16-Bit Load (Continued)

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Table 43.Block Transfer

															Fla	ags		
					Ad	dress	ing						7	6	4	2	1	0
Operation Name	Mnemonics	Op Code	Immed	Ext	Ind	Reg	Regl	Imp	Rel	Bytes	States	Operation	s	z	н	P/V	N	с
Block														(3)		(2)		
I ranster Search	CPD	11 101 101					s	s		2	12	Ar = (HL) _M	↑	↑	↑	↑	s	•
Data		10 101 001										BC _R -1→BC _R						
												HL _R -1→HL _R		(3)		(2)		
	CPDR	11 101 101					s	s		2	14	BC _R ≠0 Ar≠(HL) _M	↑	↑	↑	↑	s	•
		10 111 001									12	$BC_R = 0 \text{ or } Ar = (HL)_M$						
												Ar-(HL) _R Q BC _R -1-BC _R HL _R -1→HL _R						
												Repeat Q until Ar = (HL) _M or BC _R = 0		(3)		(2)		



		Machine	
MNEMONICS	Bytes	Cycles	States
	3	6	16
			(If condition is true)
CALL mn	3	6	16
CCF	1	1	3
CPD	2	6	12
CPDR	2	8	14
			$(\text{If BC}_R \neq 0 \text{ and } \text{Ar} \neq (\text{HL})_M$
	2	6	12
			$(\text{If BC}_{R} = 0 \text{ or } \text{Ar} = (\text{HL})_{M}$
CP (HL)	1	2	6
CPI	2	6	12
CPIR	2	8	14
			$(\text{If BC}_R \neq 0 \text{ and } \text{Ar} \neq (\text{HL})_M$
	2	6	12
			$(\text{If BCR} = 0 \text{ or } \text{Ar} = (\text{HL})_{\text{M}}$
CP (IX+d)	3	6	14
CP (IY+d)	3	6	14
CPL	1	1	3
CP m	2	2	6
CP g	1	2	4
DAA	1	2	4
DEC (HL)	1	4	10
DEC IX	2	3	7
DEC IY	2	3	7
DEC (IX+d)	3	8	18
DEC (IY+d)	3	8	18
DEC g	1	2	4
DEC ww	1	2	4
DI	1	1	3
DJNZ j	2	5	9 (if Br \neq 0)



262

Instruction	Machine Cycle	States	Address	Data	RD	WR	MREQ	IORQ	<u>M1</u>	HALT	ST
	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
LD g, (IX+d)	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
LD g, (IY+d)	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~M C5	TiTi	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
LD (HL),g	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	HL	g	1	0	0	1	1	1	1
	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
LD (IX + d),g	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
LD (IY + d),g	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~ MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	g	1	0	0	1	1	1	1
	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
LD (HL),m	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	T1T2T3	HL	DATA	1	0	0	1	1	1	1

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)



INTERRUPTS

Instruction	Machine Cycle	States	Address	Data	RD	WR	MREQ	IORQ	<u>M1</u>	HALT	ST
	MC1	T1T2T3	Next Op Code Address (PC)		0	1	0	1	0	1	0
NMI	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	РСН	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
INTO Mode 0	MC1	T1T2TW TWT3	Next Op Code Address	1st(PC) Op Code	1	1	1	0	0	1	0
(RST Inserted)	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	РСН	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
	MC1	T1T2Tw TWT3	Next Op Code Address (PC)	1st Op Code	1	1	1	0	0	1	0
INT0 Mode 0	MC2	T1T2T3	PC	n	0	1	0	1	1	1	1
(Call	MC3	T1T2T3	PC+1	m	0	1	0	1	1	1	1
Inserted)	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PC+2(H)	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PC+2(L)	1	0	0	1	1	1	1
INT0 Mode 1	MC1	T1T2TW TWT3	Next Op Code Address (PC)		1	1	1	0	0	1	0
	MC2	T1T2T3	SP-1	РСН	1	0	0	1	1	1	1
	MC3	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1

Table 52.Interrupts

UM005003-0703



Register	Mnemonics Address		Remarks										
DMA Memory Address Register Channel 1B:	MAR1B	2	А	Bits 0 - 2	are use	d for N	MAR1	В					
DMA I/O Address Register Channel 1L:	IAR1L	2	В										
DMA I/O Address Register Channel 1H	IAR1H	2	С										
DMA Byte Count Register Channel 1L:	BCR1L	2	Е										
DMA Byte Count Register Channel 1H:	BCR1H	2	F										
DMA Status Register:	DSTAT	3	0	bit	DE1	DE0	DWEI	DWE0	DIE1	DIE0	_	DME	
				during RESE	Т 0	0	1	1	R/W	0	1	0	-
				R/W	R/W	R/W	W	W		R/W	ļ		A Master
						I				L DMA	Interrupt	Enable 1 ()
								DMA	Enable I	Bit Write I	Enable 1,0)	
DMA Mode Register	DMODE	3	1			DM.	A enable c	h 1,0					
Dun't widde Register.	DMODE	5	1	bit	_	_	DM1	DM0	SM1	SM0	MMOD	_	
				during RESE	Г 1	1	0	0	0	0	0	1	
				R/W			R/W	R/W	R/W	R/W	R/W	famory M	ODE calag
										_ Ch 0 S	ource Mo	de 1,0	
									Destinatio	n Mode 1,	0		
				DM1,0	Destination	A	ddress	SN	41,0	Source	e	Address	
				0 0 0 1	M M		AR0+1 AR0-1		0 0 1	M		SAR0+1 SAR0-1	
				10	M I/O		AR0 fixed		10	M I/C))	SAR0 fix	ed ed
				MMOD	Mada	Di	inter		-			5.400 HA	
				0	Cycle Ste	eal Mode							
				1	Burst Mo	de							

 Table 57.
 Internal I/O Registers (Continued)



308

Memory and I/O Wait state insertion 29 Memory management unit (MMU) 13 Memory to ASCI 109 Memory to memory 105 MMU Register description 60 Mode HALT 31 IOSTOP 35 SLEEP 33 SYSTEM STOP 35 Modem control signals 138

Ν

NMI and DMA operation timing diagram 115 Use 74 Non-maskable interrupt 72

0

On-chip clock generator Circuit board design rules 170 External clock interface 169 Operating frequencies 168 Operation modes Control register 84 CPU timing 18 IOC 16 M1 Enable 15 M1 temporary enable 16

Ρ

Pin description A0 through CTS1 7 BUSREQ through RFSH 9 D0 through INT2 8 RTS0 through TEND1 10 TEST through XTAL 10 Pin package 64-pin DIP 3 68-pin PLCC 4 80-pin QFP 5 Programmable reload timer (PRT) 14 Programming Level-sense 109 PRT Block diagram 157 Bus release mode timing diagram 167 Interrupt request generation 164 Timer control register 161

R

Refresh 87 Control register 88 Register ASCI Control A0 125 ASCI Control A1 128 ASCI Control B 131 ASCI Status 0 120 ASCI Status 1 123



CSI/O control/status 147, 150, 159, 160, 161, 172 Direct bit field definitions 181 DMA mode (DMODE) 97 DMA status 95 DMA/WAIT control 100 Flag 178 I/O Control 42 I/O control (ICR) 42 Indirect addressing 181 INT/TRAP control (ITC) 67 Interrupt Vector (I) 66 MMU bank base (BBR) 62 MMU common bank area (CBAR) 60 MMU common base (CBR) 61 Operation mode control 15, 84 PRT timer control register 161 Refresh control 88 Relative addressing Addressing Relative 183 RETI control signal states 85 Instruction sequence 84 RTS0 timing diagram 140

S

Secondary bus interface 165 SLEEP mode 33 SLP execution cycle timing diagram Timing diagram SLP execution cycle 203 Status summary table 10 SYSTEM STOP mode 35

Т

Test conditions, standard 205 Timer initialization, count down and reload 163 Timer output timing diagram Timing diagram Timer output 202 Timing diagram 163 AC 197 Bus Exchange Timing During CPU Internal Operation 27 Bus Exchange Timing During Memory Read 26 CPU (I/O Read/Write cycles) 199 CSI/O external clock receive 156 CSI/O external clock transmit 154 CSI/O internal clock receive 155 CSI/O internal clock transmit 153 CSI/O receive/transmit 204 CSI/O timer output 164 DCD0 139 DMA control signals 200 DMA CYCLE STEAL mode 106 DMA edge-sense 108 DMA level-sense 107