Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010vec00tr

on-chip memory management unit (MMU) with the capability of addressing up to 1 MB of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several *glue* functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z8X180 consume a low amount of power during normal operation, but processors with Z8S180 and Z8L180 class processors also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a *stopped* state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a *stopped* state, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z8X180 provides an excellent solution to system applications requiring high performance, and low power operation.

Figures 1 through 3 illustrate the three pin packages in the Z8X180 MPU family:

- 64-Pin Dual In-line Package (DIP), Figure 1
- 68-Pin Plastic Leaded Chip Carrier (PLCC), Figure 2
- 80-Pin Quad Flat Pack (QFP), Figure 3

Pin out package descriptions for other Z8X180-based products are covered in their respective product specifications.

Figure 4 depicts the block diagram that is shared throughout all configurations of the Z8X180.

Bit Position	Bit/Field	R/W	Value	Description
2-0		R/W	000	DMA1 ext TOUT/DREQ
			001	DMA1 ASCI0
			010	DMA1 ASCI1
			011	DMA1 ESCC
			111	DMA1 PIA27-20 (P1284)

DMA Register Description

Bit 7

This bit must be set to 1 only when both DMA channels are set to take their requests from the same device. If this bit is 1 (it resets to 0), the TEND output of DMA channel o sets a flip-flop, so that thereafter the device's request is visible to channel 1, but not visible to channel 0. The internal TEND signal of channel 1 clears the FF, so that thereafter, the device's request is visible to channel 0, but no visible to channel 1.

If DMA request are from differing sources, DMA channel 0 request is forced onto DMA channel 1 after TEND output of DMA channel 0 sets the flop-flop to alternate.

Bit 6

When both DMA channels are programmed to take their requests from the same device, this bit (FF mentioned in the previous paragraph) controls which channel the device's request is presented to: 0 = DMA0, 1 = DMA l. When Bit 7 is 1, this bit is automatically toggled by the channel end output of the channels.

Table 33. Bit Values

b	Bit
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

CONDITION

f specifies the condition in program control instructions. Table 34 describes the correspondence between **f** and conditions.

Table 34. Instruction Values

f	Condition	
000	NZ	Nonzero
001	Z	Zero
010	NC	Non Carry
011	C	Carry
100	PO	Parity Odd
101	PE	Parity Even
110	P	Sign Plus
111	M	Sign Minus

Table 39. Rotate and Shift Instructions (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regi	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Bit Reset	RES b,(IY + d)	11 011 101 11 001 01l <d> 10 b 110			S/D					4	19	$0 \rightarrow b \bullet (IY + d)_M$	•	•	•	•	•	•
Bit Test	BIT b, g	11 001 011 01bg				S				2	6	$\overline{b} \bullet \overline{g} r \rightarrow z$	X	↑	S	X	R	•
	BIT b,(HL)	11 001 011 01 b 110					S			2	9	$\overline{b} \bullet \overline{(HL)}_M \rightarrow z$	X	↑	S	X	R	•
	BIT b,(IX + d)	11 011 101 11 001 011 <d> 01 b 110			S					4	15	$\overline{b} \bullet \overline{(IX + d)}_M \rightarrow z$	X	↑	S	X	R	•
	BIT b,(IY + d)	11 111 101 11 001 011 <d> 01 b 110			S					4	15	$\overline{b} \bullet \overline{(IY + d)}_M \rightarrow z$	X	↑	S	X	R	•

Table 42. 16-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Load 16-bit Data	LD (mn),HL	00 100 010 <n> <m>		D				S		3	16	Hr→(mn + 1)$_M$ Lr→(mn)$_M$	•	•	•	•	•	•
	LD (mn),IX	11 011 101 00 100 010 <n> <m>		D				S		4	19	IXHr-(mn + 1)$_M$ IXLr→(mn)$_M$	•	•	•	•	•	•
	LD (mn),IY	11 111 101 00 100 010 <n> <m>		D				S		4	19	IYHr→(mn + 1)$_M$ IYLr→(mn)$_M$	•	•	•	•	•	•

Table 43. Block Transfer

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
Block Transfer Search Data	CPD	11 101 101 10 101 001					S	S		2	12	Ar = (HL)$_M$ BC$_R$-1→BC$_R$ HL$_R$-1→HL$_R$	↑	(3) ↑	↑	(2) ↑ (3)	S	•
	CPDR	11 101 101 10 111 001					S	S		2	14 12	BC$_R$ ≠ 0 Ar ≠ (HL)$_M$ BC$_R$ = 0 or Ar = (HL)$_M$ Q Ar-(HL)$_R$ BC$_R$-1-BC$_R$ HL$_R$-1→HL$_R$ Repeat Q until Ar = (HL)$_M$ or BC$_R$ = 0	↑	↑ (3)	↑	(2) ↑ (2)	S	•

MNEMONICS	Bytes	Machine Cycles	States
	3	6	16 (If condition is true)
CALL mn	3	6	16
CCF	1	1	3
CPD	2	6	12
CPDR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If $BC_R = 0$ or $Ar = (HL)_M$
CP (HL)	1	2	6
CPI	2	6	12
CPIR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If BCR = 0 or $Ar = (HL)_M$
CP (IX+d)	3	6	14
CP (IY+d)	3	6	14
CPL	1	1	3
CP m	2	2	6
CP g	1	2	4
DAA	1	2	4
DEC (HL)	1	4	10
DEC IX	2	3	7
DEC IY	2	3	7
DEC (IX+d)	3	8	18
DEC (IY+d)	3	8	18
DEC g	1	2	4
DEC ww	1	2	4
DI	1	1	3
DJNZ j	2	5	9 (if Br ≠ 0)

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

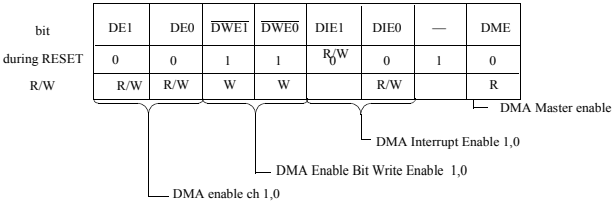
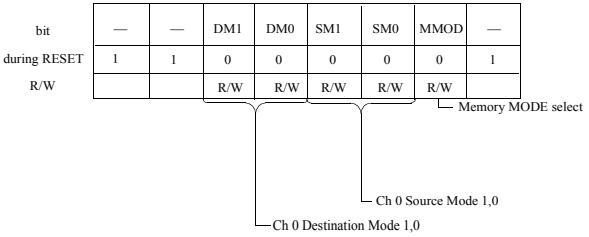
Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
LD g, (IX+d) LD g, (IY+d)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC5	TiTi	*	Z	1	1	1	1	1	1	1
	MC6	T1T2T3	IX+d IY+d	DATA	0	1	0	1	1	1	1
LD (HL),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	HL	g	1	0	0	1	1	1	1
LD (IX + d),g LD (IY + d),g	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	d	0	1	0	1	1	1	1
	MC4~MC6	TiTiTi	*	Z	1	1	1	1	1	1	1
	MC7	T1T2T3	IX+d IY+d	g	1	0	0	1	1	1	1
LD (HL),m	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
	MC3	T1T2T3	HL	DATA	1	0	0	1	1	1	1

INTERRUPTS

Table 52. Interrupts

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
$\overline{NMI}$	MC1	T1T2T3	Next Op Code Address (PC)		0	1	0	1	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (RST Inserted)	MC1	T1T2TW TWT3	Next Op Code Address	1st(PC) Op Code	1	1	1	0	0	1	0
	MC2 ~MC3	T1T1	*	Z	1	1	1	1	1	1	1
	MC4	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC5	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 0 (Call Inserted)	MC1	T1T2Tw TWT3	Next Op Code Address (PC)	1st Op Code	1	1	1	0	0	1	0
	MC2	T1T2T3	PC	n	0	1	0	1	1	1	1
	MC3	T1T2T3	PC+1	m	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP-1	PC+2(H)	1	0	0	1	1	1	1
	MC6	T1T2T3	SP-2	PC+2(L)	1	0	0	1	1	1	1
$\overline{INT0}$ Mode 1	MC1	T1T2TW TWT3	Next Op Code Address (PC)		1	1	1	0	0	1	0
	MC2	T1T2T3	SP-1	PCH	1	0	0	1	1	1	1
	MC3	T1T2T3	SP-2	PCL	1	0	0	1	1	1	1

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
DMA Memory Address Register Channel 1B:	MAR1B	2	A	Bits 0 - 2 are used for MAR1B
DMA I/O Address Register Channel 1L:	IAR1L	2	B	
DMA I/O Address Register Channel 1H	IAR1H	2	C	
DMA Byte Count Register Channel 1L:	BCR1L	2	E	
DMA Byte Count Register Channel 1H:	BCR1H	2	F	
DMA Status Register:	DSTAT	3	0	
DMA Mode Register:	DMODE	3	1	

DM1,0	Destination	Address
0 0	M	DAR0+1
0 1	M	DAR0-1
1 0	M	DAR0 fixed
1 1	I/O	DAR0 fixed

SM1,0	Source	Address
0 0	M	SAR0+1
0 1	M	SAR0-1
1 0	M	SAR0 fixed
1 1	I/O	SAR0 fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

N

O

P

R

S

T