Zilog - Z8018010VEG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010veg

- Programmable Reload Timers (PRT, 2 channels)
- Clock Serial I/O (CSIO) channel.

Other Z8X180 family members (such as Z80183, Z80S183, Z80185/195) feature, in addition to these blocks, additional peripherals and are covered in their associated Product Specification

Clock Generator

This logic generates the system clock from either an external crystal or clock input. The external clock is divided by two and provided to both internal and external devices.

Bus State Controller

This logic performs all of the status and bus control activity associated with both the CPU and some on-chip peripherals. This includes Wait State timing, RESET cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller

This block monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To remain compatible with the Z80 CPU, three different interrupt modes are supported.

Memory Management Unit

The MMU allows the user to map the memory used by the CPU (logically only 64K) into the 1MB addressing range supported by the Z8X180. The organization of the MMU object code features compatibility with the Z80 CPU while offering access to an extended memory space. This capability is accomplished by using an effective *common area - banked area* scheme.

- The HALT output pin is asserted Low
- The external bus activity consists of repeated dummy fetches of the Op Code following the HALT instruction.

Essentially, the Z80180 operates normally in HALT mode, except that instruction execution is stopped.

HALT mode can be exited in the following two ways:

- $\overline{\text{RESET}}$ Exit from HALT Mode

  If the $\overline{\text{RESET}}$ input is asserted Low for at least six clock cycles, HALT mode is exited and the normal $\overline{\text{RESET}}$ sequence (restart at address `00000H`) is initiated.

- Interrupt Exit from HALT mode

  When an internal or external interrupt is generated, HALT mode is exited and the normal interrupt response sequence is initiated.

If the interrupt source is masked (individually by enable bit, or globally by IEF1 state), the Z80180 remains in HALT mode. However, $\overline{\text{NMI}}$ interrupt initiates the normal $\overline{\text{NMI}}$ interrupt response sequence independent of the state of IEF1.

HALT timing is illustrated in Figure 20.

Low Power Modes (Z8S180/Z8L180 only)

The following section is a detailed description of the enhancements to the Z8S180/L180 from the standard Z80180 in the areas of STANDBY, IDLE and STANDBY QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce current consumption. The Z8S180 features two additional power-down modes, STANDBY and IDLE, to reduce current consumption even further. The differences in these power-down modes are summarized in Table 5.

1. Set bits 6 and 3 to `1` and `0`, respectively.
2. Set the I/O STOP bits (bit 5 of ICR, I/O Address = `3FH`) to `1`.
3. Execute the SLEEP instruction.

When the device is in STANDBY mode, it performs similar to the SYSTEM STOP mode as it exists on the Z80180-class processors, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to 50 µA (typical).

Because the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180Z8L180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{17} counts before acknowledgment is sent to the interrupt source.

The recovery source must remain asserted for the duration of the 2^{17} count, otherwise STANDBY restarts.

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the $\overline{\text{BUSREQ}}$ input is asserted. The crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- 3-State the address outputs A19–A0
- 3-State the bus control outputs $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$
- Asserting $\overline{\text{BUSACK}}$

The Z8S180 regains the system bus when $\overline{\text{BUSREQ}}$ is deactivated. The address outputs and the bus control outputs are then driven High. The STANDBY mode is exited.

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
INT	IL Register (Interrupt Vector Low Register)	IL	XX110011	33H	67
	INT/TRAP Control Register	ITC	XX110100	34H	68
	Reserved		XX110101	35H	
Refresh	Refresh Control Register	RCR	XX110110	36H	88
	Reserved		XX110111	37H	
MMU	MMU Common Base Register	CBR	XX111000	38H	61
	MMU Bank Base Register	BBR	XX111001	39H	62
	MMU Common/Bank Area Register	CBAR	XX111010	3AH	60
I/O	Reserved		XX111011	3BH	
			↕	↕	
			XX111101	3DH	
	Operation Mode Control Register	OMCR	XX111110	3EH	15
	I/O Control Register	ICR	XX111111	3FH	42

Clock Multiplier Register (CMR: 1EH) (Z8S180/L180-Class Processors Only)

Bit	7	6						0
Bit/Field	X2	Reserved						
R/W	R/W	?						
Reset	0	1						

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	X2 Clock Multiplier Mode	R/W		X2 Clock Multiplier Mode
			0	Disable
			1	Enable
6–0	Reserved	?	?	Reserved

Whether address translation (Figure 26) takes place depends on the type of CPU cycle as follows.

- Memory Cycles

  Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch, and software interrupt restarts.

- I/O Cycles

  The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The four high-order bits (A16–A19) of the physical address are always `0` during I/O cycles.

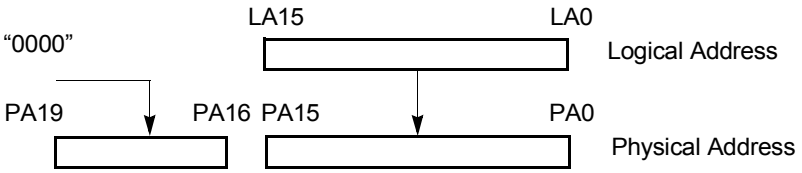


Figure 26. I/O Address Translation

- DMA Cycles

  When the Z8X180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The 20-bit source and destination registers in the DMAC are directly output on the physical address bus (A0–A19).

MMU Registers

Three MMU registers are used to program a specific configuration of logical and physical memory.

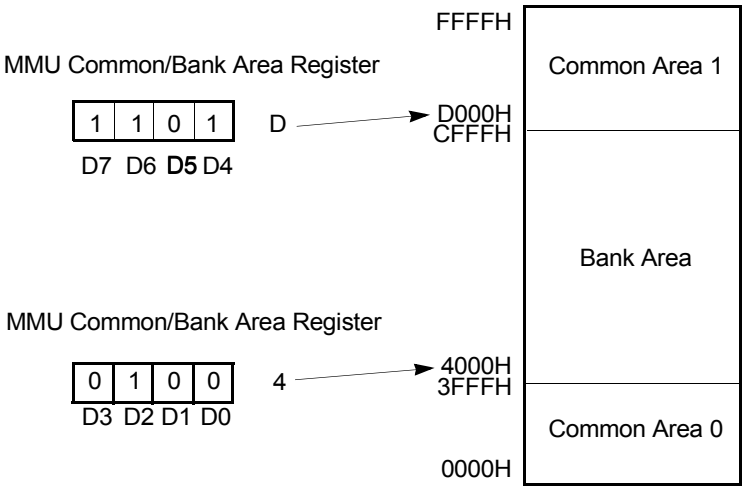


Figure 28. Logical Space Configuration (Example)

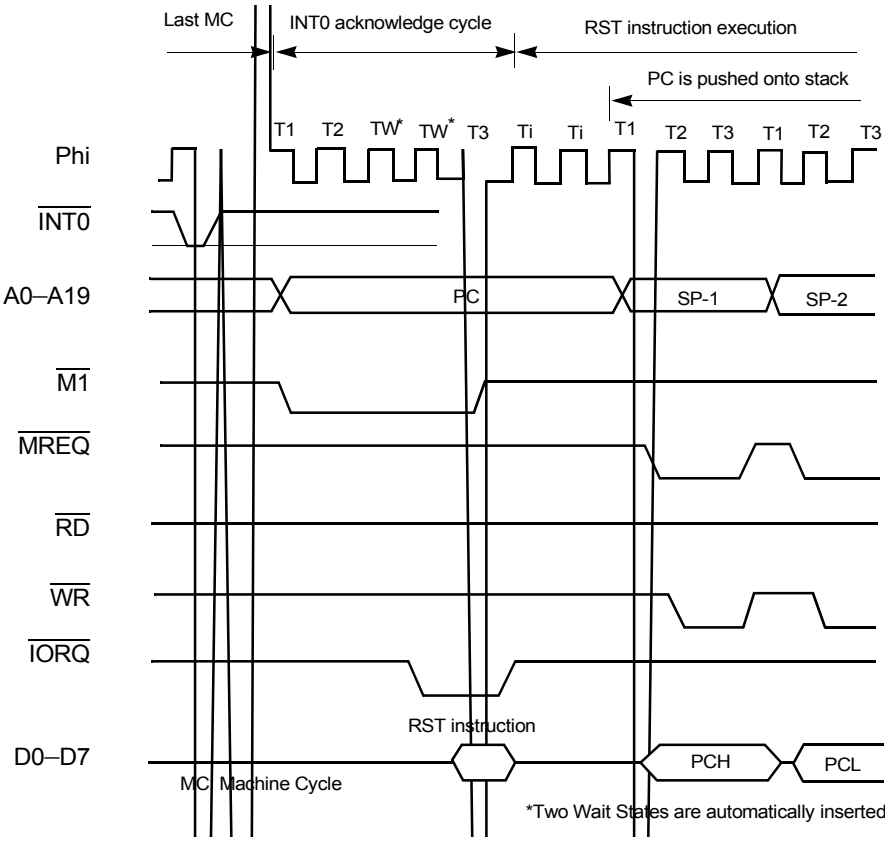
MMU and RESET

During RESET, all bits of the CA field of CBAR are set to 1 while all bits of the BA field of CBAR, CBR and BBR are reset to 0. The logical 64KB address space corresponds directly with the first 64KB 0000H to FFFFH) of the 1024KB 00000H. to FFFFFH) physical address space. Thus, after RESET, the Z8X180 begins execution at logical and physical address 0.

MMU Register Access Timing

When data is written into CBAR, CBR or BBR, the value is effective from the cycle immediately following the I/O write cycle which updates these registers.

During MMU programming insure that CPU program execution is not disrupted. The next cycle following MMU register programming is normally an Op Code fetch from the newly translated address. One technique is to localize all MMU programming routines in a Common Area that is always enabled.



Note: The TRAP interrupt occurs if an invalid instruction is fetched during Mode 0 interrupt acknowledge. (Reference Figure 36.)

Figure 36. $\overline{\text{INT0}}$ Mode 0 Timing Diagram

INT0 Mode 1

When $\overline{\text{INT0}}$ is received, the PC is stacked and instruction execution restarts at logical address `0038H`. Both IEF1 and IEF2 flags are reset to `0`,

In addition, the operation of channel 0 DMA with the on-chip ASCI (Asynchronous Serial Communication Interface) as well as Channel 1 DMA are described.

Memory to Memory—Channel 0

For memory to/from memory transfers, the external $\overline{\text{DREQ0}}$ input is not used for DMA transfer timing. Rather, the DMA operation is timed in one of two programmable modes – BURST or CYCLE STEAL. In both modes, the DMA operation automatically proceeds until termination (shown by byte count-BCR0) = 0.

In BURST mode, the DMA operation proceeds until termination. In this case, the CPU cannot perform any program execution until the DMA operation is completed. In CYCLE STEAL mode, the DMA and CPU operation are alternated after each DMA byte transfer until the DMA is completed. The sequence:

- 1 CPU Machine Cycle
- DMA Byte Transfer

is repeated until DMA is completed. Figure 46 describes CYCLE STEAL mode DMA timing.

Bit Position	Bit/Field	R/W	Value	Description
0	TIE	R/W		**Transmit Interrupt Enable** — TIE must be set to 1 to enable ASCI transmit interrupt requests. If TIE is 1, an interrupt is requested when TDRE is 1. TIE is cleared to 0 during RESET.

Timer Reload Register Channel 1L (RLDR1L: 16H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Timer Reload Register Channel 1H (RLDR1H: 17H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	Timer Reload Data							
R/W	R/W							
Reset	0							

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Timer Control Register (TCR)

TCR monitors both channels (PRT0, PRT1) TMDR status. It also controls enabling and disabling of down counting and interrupts along with controlling output pin A18/TOUT for PRT1.

Timer Control Register (TCR: 10H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Software Architecture

INSTRUCTION SET

The Z80180 is object code-compatible with the Z80 CPU. Refer to the *Z80 CPU Technical Manual* or the *Z80 Assembly Language Programming Manual* for further details.

Table 26. Instruction Set Summary

New Instructions	Operation
SLP	Enter SLEEP mode
MLT	8-bit multiply with 16-bit result
INO g, (m)	Input contents of immediate I/O address
OUT0 (m), g	Output register contents to immediate I/O address
OTIM	Block output - increment
OTIMR	Block output - increment and repeat
OTDM	Block output - decrement
OTDMR	Block output - decrement and repeat
TSTIO m	Non-destructive AND, I/O port, and accumulator
TST g	Non-destructive AND, register, and accumulator
TST m	Non-destructive AND, immediate data, and accumulator
TST (HL)	Non-destructive AND, memory data, and accumulator

SLP - Sleep

The SLP instruction causes the Z80180 to enter the SLEEP low power consumption mode. See page 32 for a complete description of the SLEEP state.

MNEMONICS	Bytes	Machine Cycles	States
SRL (IY+d)	4	7	19
SRL g	2	3	7
SUB (HL)	1	2	6
SUB (IX+d)	3	6	14
SUB (IY+d)	3	6	14
SUB m	2	2	6
SUB g	1	2	4
**TSTIO m	3	4	12
**TST g	2	3	7
TST m**	3	3	9
TST (HL)**	2	4	10
XOR (HL)	1	2	6
XOR (IX+d)	3	6	14
XOR (IY+d)	3	6	14
XOR m	2	2	6
XOR g	1	2	4

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
TST g**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
TST m**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	T1T2T3	1st operand Address	m	0	1	0	1	1	1	1
TST (HL)**	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	2	0	2	0	2	0
	MC2	T1T2T3	2nd Op Code Address	2nd Op Code	0	1	0	1	0	1	1
	MC3	Ti	*	Z	1	1	1	1	1	1	1
	MC4	T1T23	HL	Data	0	1	0	1	1	1	1

Operating Modes Summary

REQUEST ACCEPTANCES IN EACH OPERATING MODE

Table 53. Request Acceptances in Each Operating Mode

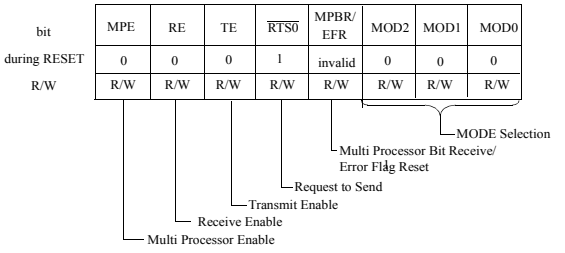
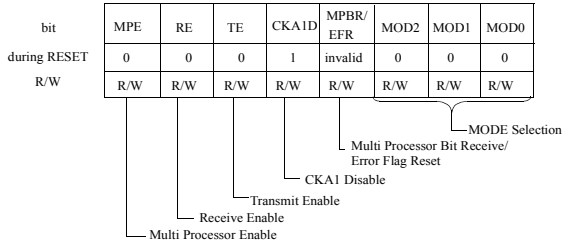
Current Status / Request		Normal Operation (CPU mode and IOSTOP Mode)	WAIT State	Refresh Cycle	Interrupt Acknowledge Cycle	DMA Cycle	BUS RELEASE Mode	SLEEP Mode	SYSTEM STOP Mode
$\overline{WAIT}$		Acceptable	Acceptable	Not acceptable	Acceptable	Acceptable	Not acceptable	Not acceptable	Not acceptable
Refresh Request Request of Refresh by the on-chip Refresh Controller		Refresh cycle begins at the end of Machine Cycle (MC)	Not acceptable	Not acceptable	Refresh cycle begins at the end MC	Refresh cycle begins at the end of MC	Not acceptable	Not acceptable	Not acceptable
$\overline{DREQ0}$ $\overline{DREQ1}$		DMA cycle begins at the end of MC	DMA cycle begins at the end of MC	Acceptable Refresh cycle precedes. DMA cycle begins at the end of one MC	Acceptable DMA cycle begins at the end of MC.	Acceptable Refer to "DMA Controller" for details.	Acceptable *After BUS RELEASE cycle, DMA cycle begins at the end of one MC	Not acceptable	Not acceptable
$\overline{BUSREQ}$		Bus is released at the end of MC	Not acceptable	Not acceptable	Bus is released at the end of MC	Bus is released at the end of MC	Continue BUS RELEASE mode	Acceptable	Acceptable
Interrupt	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$	Accepted after executing the current instruction.	Accepted after executing the current instruction	Not acceptable	Not acceptable	Not acceptable	Not acceptable	Acceptable Return from SLEEP mode to normal operation.	Acceptable Return from SYSTEM STOP mode to normal operation

I/O Registers

INTERNAL I/O REGISTERS

By programming IOA7 and IOA6 as the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

Table 57. Internal I/O Registers

Register	Mnemonics	Address		Remarks
ASCI Control Register A Channel 0:	CNTLA0	0	0	
ASCI Control Register A Channel 1:	CNTLA1	0	1	

MOD 2 1 0
0 0 0 Start + 7 bit Data + 1 Stop
0 0 1 Start + 7 bit Data + 2 Stop
0 1 0 Start + 7 bit Data + Parity + 1 Stop
0 1 1 Start + 7 bit Data + Parity + 2 Stop
1 0 0 Start + 8 bit Data + 1 Stop
1 0 1 Start + 8 bit Data + 2 Stop
1 1 0 Start + 8 bit Data + Parity + 1 Stop
1 1 1 Start + 8 bit Data + Parity + 2 Stop

A

B

C