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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010vsc

Central Processing Unit

The CPU is microcoded to provide a core that is object code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiply and divide. This core has been enhanced to allow many of the instructions to execute in fewer clock cycles.

DMA Controller

The DMA controller provides high speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O and I/O to I/O. Transfer modes supported are REQUEST, BURST, and CYCLE STEAL. DMA transfers can access the full 1MB addressing range with a block length up to 64KB, and can cross over 64K boundaries.

Asynchronous Serial Communications Interface (ASCI)

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communications format.

Programmable Reload Timer (PRT)

This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSIO)

The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer.

Table 7. I/O Address Map (Z8S180/Z8L180-Class Processors Only) (Continued)

	Register	Mnemonic	Address		
			Binary	Hex	Page
DMA	DMA Source Address Register Ch 0L	SAR0L	XX100000	20H	93
	DMA Source Address Register Ch 0H	SAR0H	XX100001	21H	93
	DMA Source Address Register Ch 0B	SAR0B	XX100010	22H	93
	DMA Destination Address Register Ch 0L	DAR0L	XX100011	23H	94
	DMA Destination Address Register Ch 0H	DAR0H	XX100100	24H	94
	DMA Destination Address Register Ch 0B	DAR0B	XX100101	25H	94
	DMA Byte Count Register Ch 0L	BCR0L	XX100110	26H	94
	DMA Byte Count Register Ch 0H	BCR0H	XX100111	27H	94
	DMA Memory Address Register Ch 1L	MAR1L	XX101000	28H	94
	DMA Memory Address Register Ch 1H	MAR1H	XX101001	29H	94
	DMA Memory Address Register Ch 1B	MAR1B	XX101010	2AH	94
	DMA I/O Address Register Ch 1L	IAR1L	XX101011	2BH	102
	DMA I/O Address Register Ch 1H	IAR1H	XX101100	2CH	102
	DMA I/O Address Register Ch 1	IAR1B	XX101101	2DH	94
	DMA Byte Count Register Ch 1L	BCR1L	XX101110	2EH	94
	DMA Byte Count Register Ch 1H	BCR1H	XX101111	2FH	94
	DMA Status Register	DSTAT	XX110000	30H	95
	DMA Mode Register	DMODE	XX110001	31H	97
	DMA/WAIT Control Register	DCNTL	XX110010	32H	101

Bit Position	Bit/Field	R/W	Value	Description
2	LNIO	R/W	0 1	Standard Drive 33% Drive on certain external I/O
1	LNCPUCTL	R/W	0 1	Standard Drive 33% Drive on CPU control signals
0	LNAD/ DATA	R/W	0 1	Standard Drive 33% drive on A10–A0, D7–D0

Memory Management Unit (MMU)

The Z8X180 features an on-chip MMU which performs the translation of the CPU 64KB (16-bit addresses 0000H to FFFFH) logical memory address space into a 1024KB (20-bit addresses 00000H to FFFFFH) physical memory address space. Address translation occurs internally in parallel with other CPU operation.

Logical Address Spaces

The 64KB CPU logical address space is interpreted by the MMU as consisting of up to three separate logical address areas, Common Area 0, Bank Area, and Common Area 1.

As depicted in Figure 23, a variety of logical memory configurations are possible. The boundaries between the Common and Bank Areas can be programmed with 4KB resolution.

MMU and RESET

During RESET, all bits of the CA field of CBAR are set to 1 while all bits of the BA field of CBAR, CBR and BBR are reset to 0. The logical 64KB address space corresponds directly with the first 64KB 0000H to FFFFH) of the 1024KB 00000H. to FFFFFH) physical address space. Thus, after RESET, the Z8X180 begins execution at logical and physical address 0.

MMU Register Access Timing

When data is written into CBAR, CBR or BBR, the value is effective from the cycle immediately following the I/O write cycle which updates these registers.

During MMU programming insure that CPU program execution is not disrupted. The next cycle following MMU register programming is normally an Op Code fetch from the newly translated address. One technique is to localize all MMU programming routines in a Common Area that is always enabled.

memory mapped I/O. transfers, the CKA0/$\overline{\text{DREQ0}}$ pin automatically functions as input pin or output pin even if it has been programmed as output pin for CKA0. And the CKA1/$\overline{\text{TEND0}}$ pin functions as an input or an output pin for $\overline{\text{TEND0}}$ by setting CKA1D to 1 in CNTLA1.

To initiate memory to/from I/O (and memory to/from memory mapped I/O) DMA transfer for channel 0, perform the following operations:

1. Load the memory and I/O or memory mapped I/O source and destination addresses into SAR0 and DAR0.

   I/O addresses (not memory mapped I/O are limited to 16 bits (A0–A15). Make sure that bits A16, A17 and A19 are 0 (A18 is a don't care) to correctly enable the external $\overline{\text{DREQ0}}$ input.

2. Specify memory to/from I/O or memory to/from memory mapped I/O mode and address increment/decrement in the SM0, SM1, DM0 and DM1 bits of DMODE.

3. Load the number of bytes to transfer in BCR0.

4. Specify whether $\overline{\text{DREQ0}}$ is edge- or level-sense by programming the DMS0 bit of DCNTL.

5. Enable or disable DMA termination interrupt with the DIE0 bit in DSTAT.

6. Program DE0: = 1 (with $\overline{\text{DWEO}}$ = 0 in the same access) in DSTAT and the DMA operation begins under the control of the $\overline{\text{DREQ0}}$ input.

Memory to ASCI - Channel 0

Channel 0 has extra capability to support DMA transfer to/from the on-chip two channel ASCI. In this case, the external $\overline{\text{DREQ0}}$ input is not used for DMA timing. Rather, the ASCI status bits are used to generate an internal $\overline{\text{DREQ0}}$ The TDRE (Transmit Data Register Empty) bit and the RDRF (Receive Data Register Full) bit are used to generate an internal

ASCI Control Register A0, 1 (CNTLA0, 1)

Each ASCI channel Control Register A configures the major operating modes such as receiver/transmitter enable and disable, data format, and multiprocessor communication mode.

ASCI Status Register 1 (STAT1: 05H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
R/W	R	R	R	R	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	RDRF	R		**Receive Data Register Full** — RDRF is set to 1 when an incoming data byte is loaded into RDR. Note that if a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into RDR. RDRF is cleared to 0 by reading RDR, when the DCD0 input is High, in IOSTOP mode, and during RESET.
6	OVRN	R		**Overrun Error** — OVRN is set to 1 when RDR is full and RSR becomes full. OVRN is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.
5	PE	R		**Parity Error** — PE is set to 1 when a parity error is detected on an incoming data byte and ASCI parity detection is enabled (the MOD1 bit of CNTLA is set to 1). PE is cleared to 0 when the EFR bit (Error Flag Reset) of CNTLA is written to 0, when DCD0 is High, in IOSTOP mode, and during RESET.

Bit Position	Bit/Field	R/W	Value	Description
2–0	MOD2–0	R/W		**ASCI Data Format Mode 2, 1, 0** — These bits program the ASCI data format as follows. **MOD2** 0: 7 bit data 1: 8 bit data **MOD1** 0: No parity 1: Parity enabled **MOD0** 0: 1 stop bit 1: 2 stop bits The data formats available based on all combinations of MOD2, MOD1 and MOD0 are described in Table 17.

Bit Position	Bit/Field	R/W	Value	Description
2	Break Feature Enable	R/W	0 1	Break Feature Enable On Break Feature Enable Off
1	Break Detect (RO)	R/W	0 1	Break Detect On Break Detect Off
0	Send Break	R/W	0 1	Normal Xmit Drive TXA Low

Each ASCI channel control register B configures multiprocessor mode, parity and baud rate selection.

ASCI0 Time Constant Low Register (I/O Address: 1AH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

ASCI0 Time Constant High Register (I/O Address: 1BH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

c. Poll the RE bit in CNTR until RE = 0.

d. Read the receive data from TRDR.

e. Repeat steps 2 to 4 for each receive data byte.

- Receive–Interrupts

a. Poll the RE bit in CNTR until RE is 0.

b. Set the RE and EIE bits in CNTR to 1.

c. When the receive interrupt occurs read the receive data from TRDR.

d. Set the RE bit in CNTR to 1.

e. Repeat steps 3 and 4 for each receive data byte.

CSI/O Operation Timing Notes

- Transmitter clocking and receiver sampling timings are different from internal and external clocking modes. Figure 59 to Figure 62 illustrate CSI/O Transmit/Receive Timing.
- The transmitter and receiver is disabled TE and RE = 0) when initializing or changing the baud rate.

CSI/O Operation Notes

- Disable the transmitter and receiver (TE and RE = 0) before initializing or changing the baud rate. When changing the baud rate after completion of transmission or reception, a delay of at least one bit time is required before baud rate modification.
- When RE or TE is cleared to 0 by software, a corresponding receive or transmit operation is immediately terminated. Normally, TE or RE is only cleared to 0 when EF is 1.
- Simultaneous transmission and reception is not possible. Thus, TE and RE are not both 1 at the same time.

Bit Position	Bit/Field	R/W	Value	Description
7–6	TIF1–0	R		**TIF1: Timer Interrupt Flag** — When TMDR1 decrements to 0, TIF1 is set to 1. This generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0. When TMDR0 decrements to 0, TIF0 is set to 1. This generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.
5–4	TIE1–0	R/W		**Timer Interrupt Enable** — When TIE1 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE1 is reset to 0, the interrupt request is inhibited. During RESET, TIE1 is cleared to 0. When TIE0 is set to 1, TIF0 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.
3–2	TOC1–0	R/W		**Timer Output Control** — TOC1, and TOC0 control the output of PRT1 using the multiplexed A18/TOUT pin as shown in Table 23. During RESET, TOC1 and TOC0 are cleared to 0. This selects the address function for A18/TOUT. By programming TOC1 and TOC0 the A18/TOUT pin can be forced HIGH, LOW, or toggled when TMDR1 decrements to 0. Reference Table 23.
1–0	TDE1–0	R/W		**Timer Down Count Enable** — TDE1 and TDE0 enable and disable down counting for TMDR1 and TMDR0 respectively. When TDEn (n = 0, 1) is set to 1, down counting is executed for TMDRn. When TDEn is reset to 0, down counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

These devices require connection with the Z8X180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z8X180 clock rate. Table 24, and Figure 67 through Figure 70 define E clock output timing.

Wait States are inserted in Op Code fetch, memory read/write, and I/O read/write cycles which extend the duration of E clock output High. During I/O read/write cycles with no Wait States (only occurs during on-chip I/O register accesses), E does not go High.

Table 24. E Clock Timing in Each Condition

Condition	**Duration of E Clock Output High**	
Op Code Fetch Cycle Memory Read/Write Cycle	T2 rise - T3 fall	(1.5 Phi + nw x Phi)
I/O read Cycle	1st Tw rise - T3 fall	(0.5Phi + nw x Phi)
I/O Write Cycle	1st Tw rise - T3 rise	In_w x Phi)
$\overline{NMI}$ Acknowledge 1st MC	T2 rise - T3 fall	(1.5 Phi)
$\overline{INT0}$ Acknowledge 1st MC	1st Tw rise - T3 fall	(0.50 + nw x Phi)
BUS RELEASE mode SLEEP mode SYSTEM STOP mode	Phi fall - Phi fall	(2 Phi or 1 Phi)
Note: nw = the number of Wait States; MC: Machine Cycle		

Software Architecture

INSTRUCTION SET

The Z80180 is object code-compatible with the Z80 CPU. Refer to the *Z80 CPU Technical Manual* or the *Z80 Assembly Language Programming Manual* for further details.

Table 26. Instruction Set Summary

New Instructions	Operation
SLP	Enter SLEEP mode
MLT	8-bit multiply with 16-bit result
INO g, (m)	Input contents of immediate I/O address
OUT0 (m), g	Output register contents to immediate I/O address
OTIM	Block output - increment
OTIMR	Block output - increment and repeat
OTDM	Block output - decrement
OTDMR	Block output - decrement and repeat
TSTIO m	Non-destructive AND, I/O port, and accumulator
TST g	Non-destructive AND, register, and accumulator
TST m	Non-destructive AND, immediate data, and accumulator
TST (HL)	Non-destructive AND, memory data, and accumulator

SLP - Sleep

The SLP instruction causes the Z80180 to enter the SLEEP low power consumption mode. See page 32 for a complete description of the SLEEP state.

8-bit Register

g or g field '	Register
0	B
0 0 1	C
0 1 0	D
0 1 1	E
1 0 0	H
1 0 1	L
1 1 0	—
1 1 1	A

ww field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	S P

xx field	Register
0 0	B C
0 1	D E
1 0	I X
1 1	S P

16-bit Register

zz field	Register
0 0	B C
0 1	D E
1 0	H L
1 1	A F

yy field	Register
0 0	B C
0 1	D E
1 0	I Y
1 1	S P

Suffixed H and L ww,xx,yy,zz (ex. wwH,IXL) indicate upper and lower 8-bit of the 16-bit register respectively.

Figure 75. Register Direct — Bit Field Definitions

Register Indirect (REG)

The memory operand address is contained in one of the 16-bit General Purpose Registers (BC, DE, and HL) as illustrated in Figure 76.

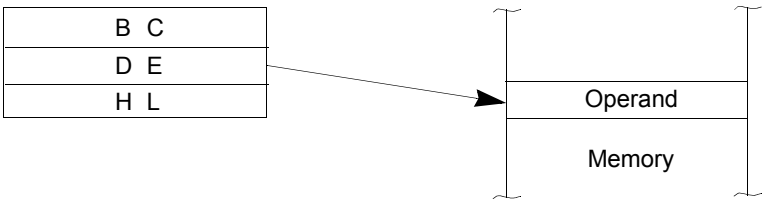

Figure 76. Register Indirect Addressing

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8-bit signed displacement specified in the instruction. Refer to Figure 77

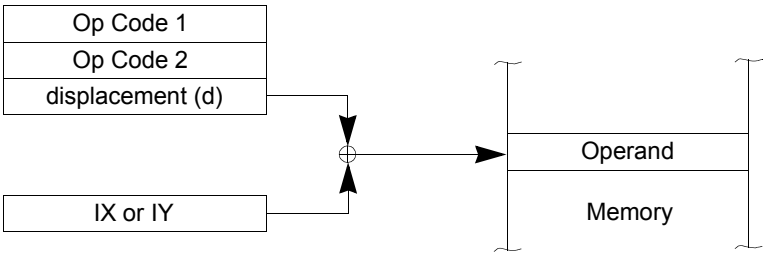

Figure 77. Indexed Addressing

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction, as depicted in Figure 78.

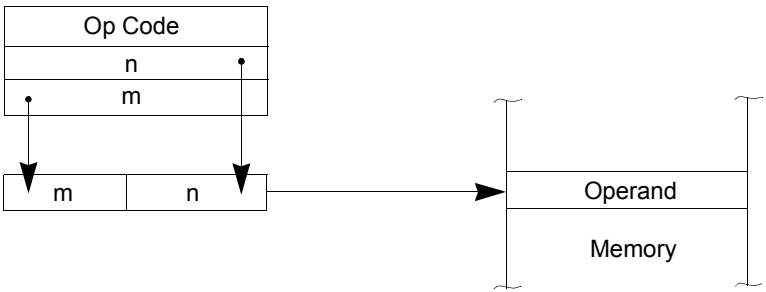

Figure 78. Extended Addressing

MNEMONICS	Bytes	Machine Cycles	States
	3	6	16 (If condition is true)
CALL mn	3	6	16
CCF	1	1	3
CPD	2	6	12
CPDR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If $BC_R = 0$ or $Ar = (HL)_M$
CP (HL)	1	2	6
CPI	2	6	12
CPIR	2	8	14 (If $BC_R \neq 0$ and $Ar \neq (HL)_M$
	2	6	12 (If BCR = 0 or $Ar = (HL)_M$
CP (IX+d)	3	6	14
CP (IY+d)	3	6	14
CPL	1	1	3
CP m	2	2	6
CP g	1	2	4
DAA	1	2	4
DEC (HL)	1	4	10
DEC IX	2	3	7
DEC IY	2	3	7
DEC (IX+d)	3	8	18
DEC (IY+d)	3	8	18
DEC g	1	2	4
DEC ww	1	2	4
DI	1	1	3
DJNZ j	2	5	9 (if Br ≠ 0)

MNEMONICS	Bytes	Machine Cycles	States
LD g,g'	1	2	4
LD SP,HL	1	2	4
LD SP,IX	2	3	7
LD SP,IY	2	3	7
MLT ww"	2	13	17
NEG	2	2	6
NOP	1	1	3
OR (HL)	1	2	6
OR (IX+d)	3	6	14
OR (IY+d)	3	6	14
OR m	2	2	6
OR g	1	2	4
OTDM**	2	6	14
OTDMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTDR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0
OTIM**	2	6	14
OTIMR**	2	8	16 (If Br ≠ 0)
	2	6	14 (If Br = 0)
OTIR	2	6	14 (If Br ≠ 0)
	2	4	12 (If Br = 0)
OUTD	2	4	12
OUTI	2	4	12
OUT (m),A	2	4	10
OUT (C),g	2	4	10
OUT0 (m),g **	3	5	13
POP IX	2	4	12
POP IY	2	4	12
POP zz	1	3	9

Table 51. Bus and Control Signal Condition in Each Machine Cycle (Continued)

Instruction	Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$	$\overline{HALT}$	ST
DJNZ j (If Br ≠ 0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti*2	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	1st operand Address	j-2	0	1	0	1	1	1	1
	MC4~MC5	TiTi	*	Z	1	1	1	1	1	1	1
DJNZ j (If Br=0)	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti*1	*	Z	1	1	1	1	1	1	1
	MC3	T1T2T3	1st operand Address	j-2	0	1	0	1	1	1	1
EI*3	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
EX DE, HL EXX	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
EX AF, AF'	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	Ti	*	Z	1	1	1	1	1	1	1
EX (SP), HL	MC1	T1T2T3	1st Op Code Address	1st Op Code	0	1	0	1	0	1	0
	MC2	T1T2T3	SP	DATA	0	1	0	1	1	1	1
	MC3	T1T2T3	SP+1	DATA	0	1	0	1	1	1	1
	MC4	Ti	*	Z	1	1	1	1	1	1	1
	MC5	T1T2T3	SP+1	H	1	0	0	1	1	1	1
	MC6	T1T2T3	SP	L	1	0	0	1	1	1	1

*2 DMA,REFRESH, or BUS RELEASE cannot be executed after this state. (Request is ignored)
*3 Interrupt request is not sampled.

Table 57. Internal I/O Registers (Continued)

Register	Mnemonics	Address		Remarks
ASCI Control Register B Channel 0:	CNTLB0	0	2	

bit	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
during RESET	invalid	0	*	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Source and Speed Select
Divide Ratio
Parity Even or Odd
Clear to send/Prescale
Multi Processor
Multi Processor Bit Transmit

* $\overline{CTS}$: Depending on the condition 0f $\overline{CTS}$ Pin.
PS: Cleared to 0.

ASCI Control Register B Channel 1:	CNTLB1	0	3

bit	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
during RESET	invalid	0	0	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Source and Speed Select
Divide Ratio
Parity Even or Odd
Clear to Send/Prescale
Multi Processor
Multi Processor Bit Transmit

General divide ratio	PS=0 (divide ratio=10)		PS=1 (divide ratio=30)	
SS2 1 0	DR=0 (X 16)	DR=1 (X 64)	DR=0 (X 16)	DR=1 (X 64)
0 0 0	$\phi \div 160$	$\phi \div 640$	$\phi \div 480$	$\phi \div 1920$
0 0 1	$\div 320$	$\div 1280$	$\div 960$	$\div 3840$
0 1 0	$\div 640$	$\div 2560$	$\div 1920$	$\div 7680$
0 1 1	$\div 1280$	$\div 5120$	$\div 3840$	$\div 15360$
1 0 0	$\div 2560$	$\div 10240$	$\div 7680$	$\div 30720$
1 0 1	$\div 5120$	$\div 20480$	$\div 15360$	$\div 61440$
1 1 0	$\div 10240$	$\div 40960$	$\div 30720$	$\div 122880$
1 1 1	External clock (frequency $< \phi \div 40$)			

N

O

P

R