Zilog - Z8018010VSG Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018010vsg

Table 2. Multiplexed Pin Descriptions

Multiplexed Pins	Descriptions
A18/TOUT	During RESET, this pin is initialized as A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A18 function is selected.
CKA0/$\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA_0 pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, $\overline{\text{DREQ0}}$ function is always selected.
CKA1/$\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1 pin. If CKA1D bit in ASCI control register ch 1 (CNTLA1) is set to 1, $\overline{\text{TEND0}}$ function is selected. If CKA1D bit is set to 0, CKA1 function is selected.
RXS/$\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch 1 (STAT1) is set to 1, $\overline{\text{CTS1}}$ function is selected. If CTS1E bit is 0, RXS function is selected.

ARCHITECTURE

The Z8X180 combines a high performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller (including dynamic memory refresh), interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks:

- Direct Memory Access (DMA) Control (2 channels)
- Asynchronous Serial Communications Interface (ASCI, 2 channels),

Table 8. State of IEF1 and IEF2 (Continued)

CPU Operation	IEF1	IEF2	REMARKS
DI	0	0	
LD A, I	not affected	not affected	Transfers the contents of IEF1 to P/V
LID A, R	not affected	not affected	Transfers the contents of IEF1 to P/V

TRAP Interrupt

The Z8X180 generates a non-maskable (not affected by the state of IEF1) TRAP interrupt when an undefined Op Code fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during Op Code fetch cycles and also if an undefined Op Code is fetched during the interrupt acknowledge cycle for $\overline{\text{INT0}}$ when Mode 0 is used.

When a TRAP interrupt occurs the Z8X180 operates as follows:

1. The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to `1`.
2. The current PC (Program Counter) value, reflecting location of the undefined Op Code, is saved on the stack.
3. The Z8X180 vectors to logical address 0. Note that if logical address `0000H` is mapped to physical address `00000H`. the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address `00000H` was caused by RESET or TRAP.

The state of the UFO (Undefined Fetch Object) bit in ITC allows TRAP manipulation software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the Op Code generated the TRAP. If UFO is `0`, the starting address of the invalid instruction is equal to the

Refresh cycles may be programmed to be either two or three clock cycles in duration by programming the REFW (Refresh Wait) bit in the Refresh Control Register (RCR). The external $\overline{\text{WAIT}}$ input and the internal Wait State generator are not effective during refresh.

Figure 44 depicts the timing of a refresh cycle with a refresh wait (TRW) cycle.

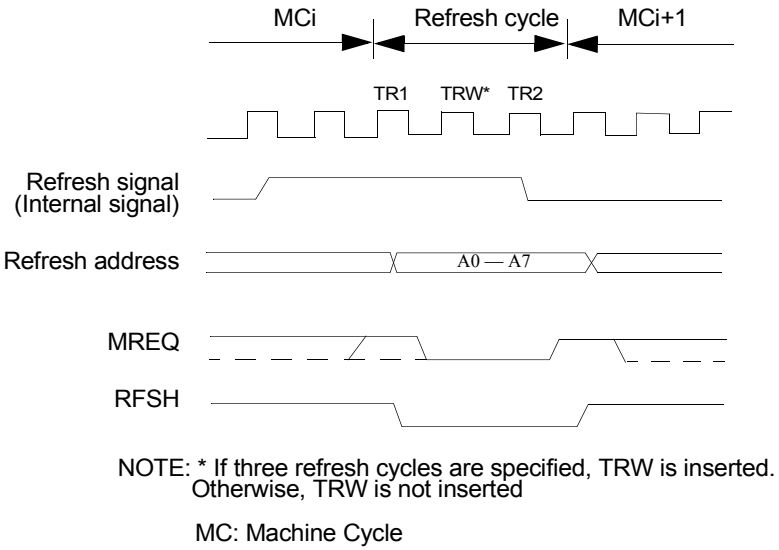


Figure 44. Refresh Cycle Timing Diagram

Channel 0

- SAR0–Source Address Register
- DAR0–Destination Address Register
- BCR0–Byte Count Register

Channel 1

- MAR1–Memory Address Register
- IAR1–I/O Address Register
- BCR1–Byte Count Register

The two channels share the following three additional registers in common:

- DSTAT–DMA Status Register
- DMODE–DMA Mode Register
- DCNTL–DMA Control Register

DMAC Block Diagram

Figure 45 depicts the Z8X180 DMAC Block Diagram.

rising edge of the clock prior to T3 at which time the DMA operation (re)starts. Figure 48 depicts the edge-sense DMA timing.

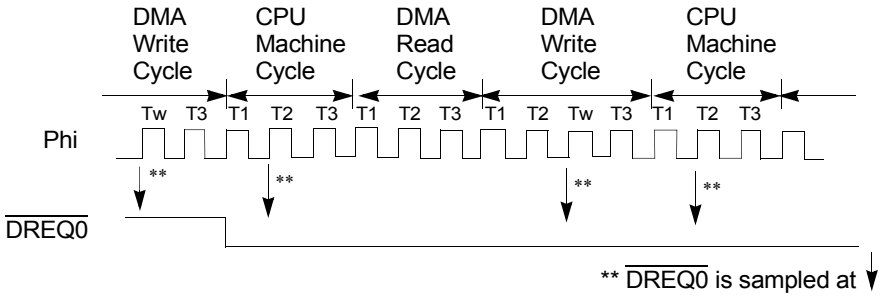


Figure 48. CPU Operation and DMA Operation $\overline{\text{DREQ0}}$ is Programmed for Edge-Sense

During the transfers for channel 0, the $\overline{\text{TEND0}}$ output goes Low synchronous with the write cycle of the last (BCR0 = 00H) DMA transfer (Reference Figure 49).

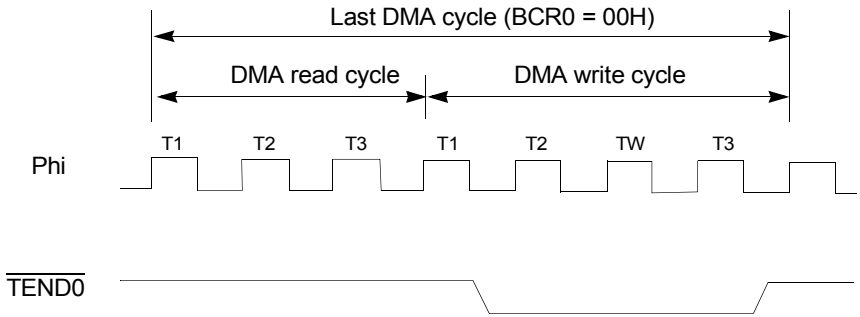


Figure 49. $\overline{\text{TEND0}}$ Output Timing Diagram

The $\overline{\text{DREQ0}}$ and $\overline{\text{TEND0}}$ pins are programmably multiplexed with the CKA0 and CKA1 ASCI clock input/outputs. However, when DMA channel 0 is programmed for memory to/from I/O (and memory to/from

ASCI Control Register A 1 (CNTLA1: 01H)

Bit	7	6	5	4	3	2	1	0
Bit/Field	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	X	0	0	0

R = Read W = Write X = Indeterminate ? = Not Applicable

Bit Position	Bit/Field	R/W	Value	Description
7	MPE	R/W		**Multi-Processor Mode Enable** — The ASCI has a multiprocessor communication mode which utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the wakeup feature as follows. If MPE is set to 1, only received bytes in which the MPB (multiprocessor bit) is 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are ignored by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the RDRF and error flags.
6	RE	R/W		**Receiver Enable** — When RE is set to 1, the ASCI receiver is enabled. When RE is reset to 0, the receiver is disabled and any receive operation in progress is interrupted. However, the RDRF and error flags are not reset and the previous contents of RDRF and error flags are held. RE is cleared to 0 in IOSTOP mode, and during RESET.

Bit Position	Bit/Field	R/W	Value	Description
5	$\overline{\text{CTS}}$/PS	R/W		**Clear to Send/Prescale** — When read, $\overline{\text{CTS}}$/PS reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}$/PS is read as 1. When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0). For channel 1, the $\overline{\text{CTS1}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}$/PS is only valid when read if the channel 1 CTS1E bit is 1 and the CST1 input pin function is selected. The read data of $\overline{\text{CTS}}$/PS is not affected by RESET. When written, CT /PS specifies the baud rate generator prescale factor. If $\overline{\text{CTS}}$/PS is set to 1, the system clock is prescaled by 30 while if $\overline{\text{CTS}}$/PS is cleared to 0, the system clock is prescaled by 10.CTS/PS is cleared to 0 during RESET.
4	PEO	R/W		**Parity Even Odd** — PE0 selects even or odd parity. PE0 does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PE0 is cleared to 0, even parity is selected. If PE0 is set to 1, odd parity is selected.PE0 is cleared to 0 during RESET.
3	DR	R/W		**Divide Ratio** — DR specifies the divider used to obtain baud rate from the data sampling clock If DR is reset to 0, divide by 16 is used, while if DR is set to 1, divide by 64 is used. DR is cleared to 0 during RESET.
2–0	SS2–0	R/W		**Source/Speed Select** — Specifies the data clock source (internal or external) and baud rate prescale factor. SS2, SS1, and SS0 are all set to 1 during RESET. Table 18 describes the divide ratio corresponding to SS2, SS1 and SS0

The external ASCI channel 0 data clock pins are multiplexed with DMA control lines (CKA0/$\overline{\text{DREQ}}$ and CKA1/$\overline{\text{TEND0}}$). During RESET, these

ASCI1 Time Constant Low Register (I/O Address: 1CH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

ASCI1 Time Constant High Register (I/O Address: 1DH) (Z8S180/L180-Class Processors Only)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate ? = Not Applicable

Modem Control Signals

ASCI channel 0 has $\overline{\text{CTS0}}$, $\overline{\text{DCD0}}$ and $\overline{\text{RTS0}}$ external modem control signals. ASCI channel 1 has a $\overline{\text{CTS1}}$ modem control signal which is multiplexed with Clocked Serial Receive Data (RXS).

$\overline{\text{CTS0}}$: Clear to Send 0 (Input)

The $\overline{\text{CTS0}}$ input allows external control (start/stop) of ASCI channel 0 transmit operations. When $\overline{\text{CTS0}}$ is High, the channel 0 TDRE bit is held at 0 whether or not the TDR0 (Transmit Data Register) is full or empty. When $\overline{\text{CTS0}}$ is Low, TDRE reflects the state of TDR0. The actual transmit operation is not disabled by CT High, only TDRE is inhibited:

$\overline{\text{DCD0}}$: Data Carrier Detect 0 (Input)

The $\overline{\text{DCD0}}$ input allows external control (start/stop) of ASCI channel 0 receive operations. When DCD0 is High, the channel 0 RDRF bit is held at 0 whether or not the RDR0, (Receive Data Register) is full or empty.

ASCI to/from DMAC Operation

Operation of the ASCI with the on-chip DMAC channel 0 requires that the DMAC be correctly configured to use the ASCI flags as DMA request signals.

ASCI and RESET

During RESET, the ASCI status and control registers are initialized as defined in the individual register descriptions.

Receive and Transmit operations are stopped during RESET. However, the contents of the transmit and receive data registers (TDR and RDR) are not changed by RESET.

ASCI Clock

When in external clock input mode, the external clock is directly input to the sampling rate (÷16/÷64) as depicted in Figure 56.

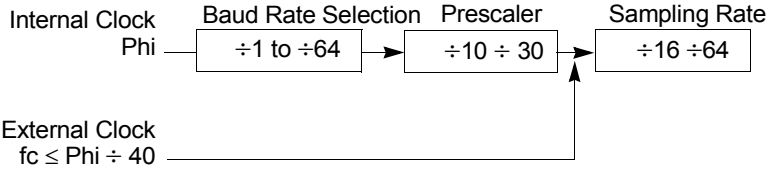


Figure 56. ASCI Clock

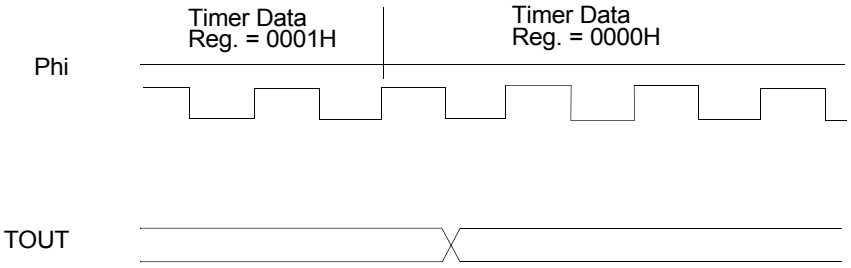


Figure 65. Timer Output Timing Diagram

PRT Interrupts

The PRT interrupt request circuit is illustrated in Figure 66.

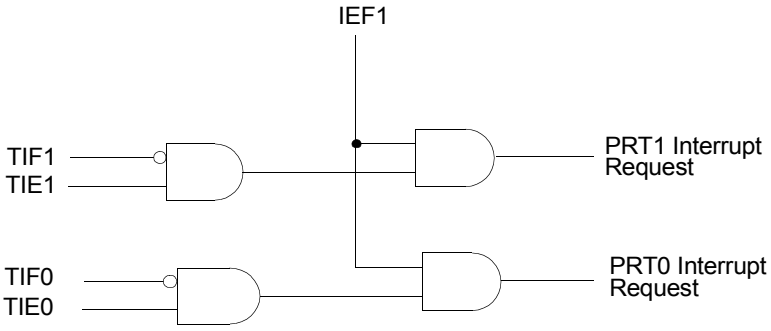


Figure 66. PRT Interrupt Request Generation

PRT and RESET

During RESET, the bits in TCR are initialized as defined in the TCR register description. Down counting is stopped and the TMDR and RLDR registers are initialized to FFFFH. The A18/TOUT pin reverts to the address output function.

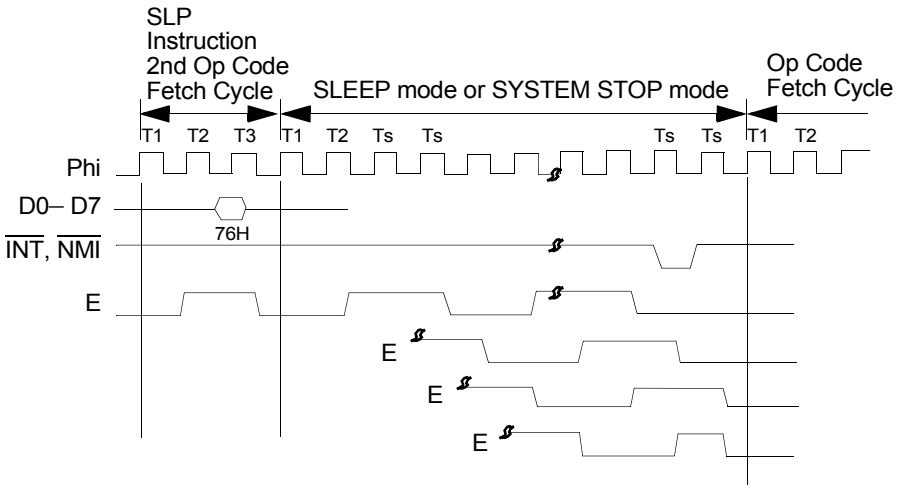


Figure 69. E Clock Timing in SLEEP Mode and SYSTEM STOP Mode

On-Chip Clock Generator

The Z8X180 contains a crystal oscillator and system clock generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock is equal to one-half the input clock. For example, a crystal or external clock input of 8 MHz corresponds with a system clock rate of 4 MHz.

Z8S180 and Z8L180-class processors also have the ability to run at X1 and X2 input clock.

Table 25 describes the AT cut crystal characteristics (Co, Rs) and the load capacitance (CL1, CL2) required for various frequencies of Z8X180 operation.

Flag Registers (F, F')

The flag registers store status bits (described in the next section) resulting from executed instructions.

General Purpose Registers (BC, BC', DE, DE', HL, HL')

The General Purpose Registers are used for both address and data operation. Depending on the instruction, each half (8 bits) of these registers (B, C, D, E, H, and I) may also be used.

Interrupt Vector Register (I)

For interrupts that require a vector table address to be calculated ($\overline{\text{INT0}}$ Mode 2, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, and internal interrupts), the Interrupt Vector Register (I) provides the most significant byte of the vector table address. I is cleared to 00H during reset.

R Counter (R)

The least significant seven bits of the R counter (R) count the number of instructions executed by the Z80180. R increments for each CPU Op Code fetch cycle (each $\overline{\text{M1}}$ cycle). R is cleared to 00H during reset.

Index Registers (IX, and IY)

The Index Registers are used for both address and data operations. For addressing, the contents of a displacement specified in the instruction are added to or subtracted from the Index Register to determine an effective operand address.

Table 31. Z8S180 AC Characteristics (Continued) V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
No.	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns

Memory Read/Write Cycle timing is the sam as I/O Read/Write Cycle except there are no automatica Wait States (TW), and MREQ is active instead of IORQ.

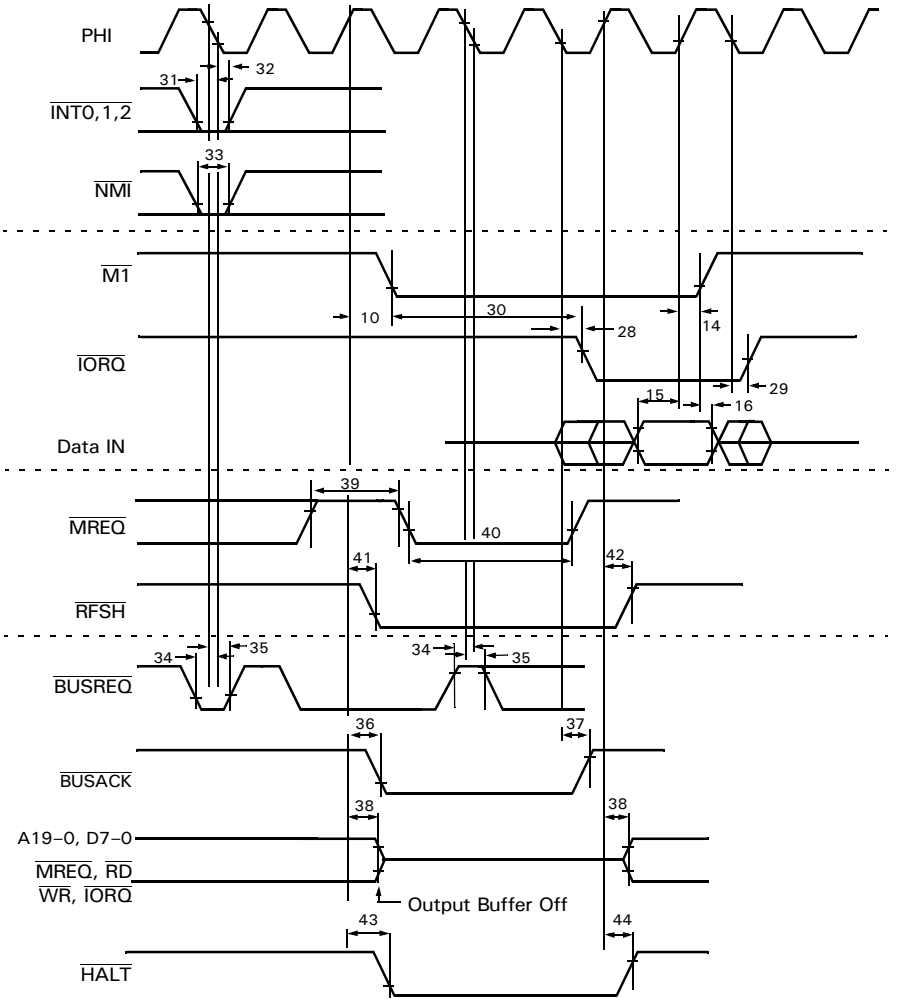


Figure 82. AC Timing Diagram 2

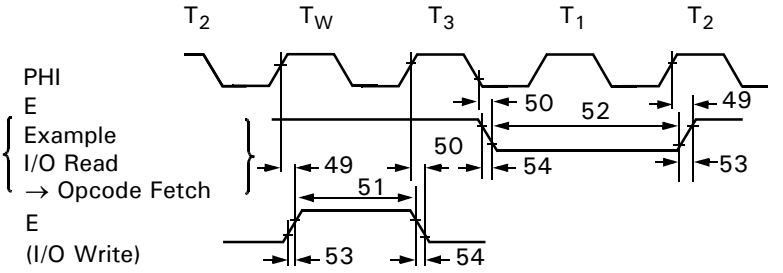


Figure 87. E Clock Timing (Minimum Timing Example of PWEL and PWEH)

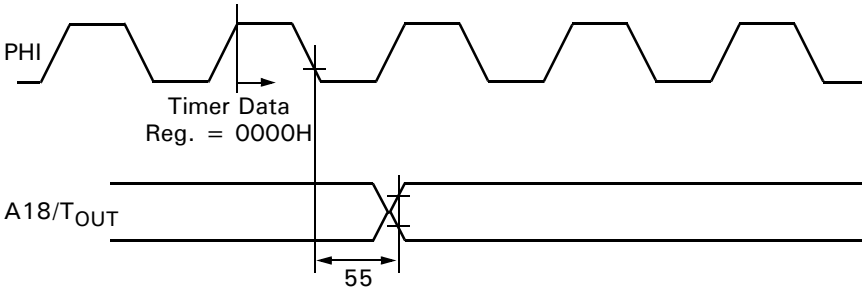


Figure 88. Timer Output Timing

STANDARD TEST CONDITIONS

The previous DC Characteristics and Capacitance sections apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

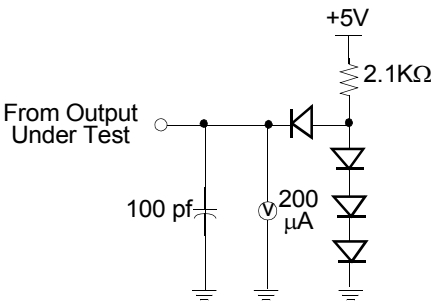


Figure 93. Test Setup

Table 41. 8-Bit Load (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 8-Bit Data	LD (IX + d),m	11 011 101 00 110 110 <d>	S		D					4	15	$m \rightarrow (IX + d)_M$	•	•	•	•	•	•
	LD (IY + d),m	11 111 101 01 110 g <d> <m>	S		D					4	15	$m \rightarrow (IY + d)_M$	•	•	•	•	•	•
	LD (HL),g	01 110 g				S	D			1	7	$gr \rightarrow (HL)_M$	•	•	•	•	•	•
	LD (IX + d),g	11 011 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IX+d)_M$	•	•	•	•	•	•
	LD (IY + d),g	11 111 101 01 110 g <d>			D	S				3	15	$gr \rightarrow (IY + d)_M$	•	•	•	•	•	•
(1) In the case of R1 and Z Mask, interrupts are not sampled at the end of LD A, I or LD A,R.																		

Table 42. 16-Bit Load

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	RegI	Imp	Rel				7 S	6 Z	4 H	2 P/V	1 N	0 C
Load 16-Bit Data	LD ww,mn	00 ww0 001 <n> <m>	S			D				3	9	$mn \rightarrow ww_R$	•	•	•	•	•	•
	LD IX,mn	11 011 101 00 100 001 <n> <m>	S					D		4	12	$mn \rightarrow IX_R$	•	•	•	•	•	•

Table 43. Block Transfer (Continued)

Operation Name	Mnemonics	Op Code	Addressing							Bytes	States	Operation	Flags					
			Immed	Ext	Ind	Reg	Regl	Imp	Rel				7	6	4	2	1	0
													S	Z	H	P/V	N	C
	CPI	11101101					S	S		2	12	Ar-$(HL)_M$	↑	↑	↑	↑	S	•
		10100001										BC_R-1→BC_R						
												HL_R + 1→HL_R		(3)		(2)		
	CPIR	11101101					S	S		2	14	$BC_R \neq 0$ Ar*$(HL)_M$	↑	↑	↑	↑	S	•
		10110001									12	BC_R = 0 or Ar = $(HL)_M$						
												Q: Ar-$(HL)_M$; BC_R-1→BC_R; HL_R + 1→HL_R						
												Repeat Q until						
												Ar = $(HL)_M$ or BC_R = 0				(2)		
	LDD	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_M$	•	•	R	↑	R	•
		10 101 000										BC_R -1→BC_R						
												DE_R-1→DE_R						
												HL_R-1→HL_R						
	LDDR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R -1 → BC_R; DE_R -1 → DE_R; HL_R -1 → HL_R	•	•	R	R	R	•
		10 111 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0				(2)		
	LDI	11 101 101					S/D			2	12	$(HL)_M \rightarrow (DE)_R$	•	•	R	↑	R	•
		10 100 000										BC_R-1→BC_R						
												DE_R + 1→DE_R						
												HL_R + 1→HL_R						
	LDIR	11 101 101					S/D			2	14($BC_R \neq 0$)	Q: $(HL)_M \rightarrow (DE)_M$; BC_R-1→BC_R; DE_R + 1→DE_R; HL_R + 1→HL_R	•	•	R	R	R	•
		10 110 000									12(BC_R = 0)	Repeat Q until						
												BC_R = 0						

(2) P/V = 0: BC_R-1 = 0
P/V = 1: BC_R-1 ≠ 0
(3) Z = 1: Ar = $(HL)_M$
Z = 0 :Ar ≠ $(HL)_M$

Table 55. Pin Outputs in Each Operating Mode (Continued)

Mode		$\overline{M1}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{RD}$	$\overline{WR}$	$\overline{RFSH}$	$\overline{HALT}$	$\overline{BUSACK}$	ST	Address BUS	Data BUS
Internal DMA	Memory Read	1	0	1	0	1	1	*	1	0	A	IN
	Memory Write	1	0	1	1	0	1	*	1	0	A	OUT
	I/O Read	1	1	0	0	1	1	*	1	0	A	IN
	I/O Write	1	1	0	1	0	1	*	1	0	A	OUT
RESET		1	1	1	1	1	1	1	1	1	Z	IN

- 1 : High
- 0 : Low
- A : Programmable
- Z : High Impedance
- IN : Input
- OUT : Output
- * : Invalid

PIN STATUS

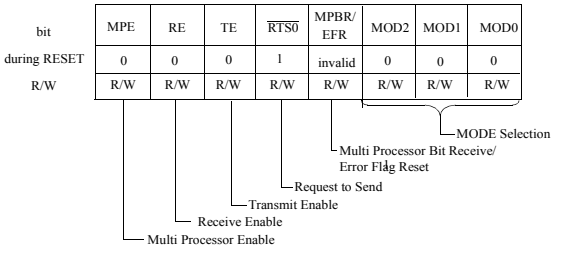
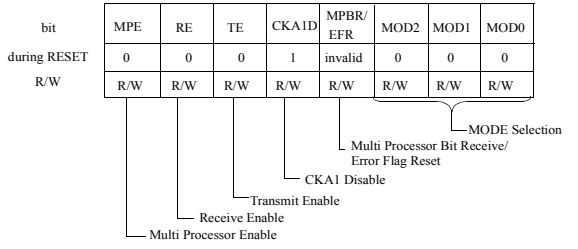
Tables 56 describes the status of each ping during RESET and LOW POWER OPERATION modes.

I/O Registers

INTERNAL I/O REGISTERS

By programming IOA7 and IOA6 as the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

Table 57. Internal I/O Registers

Register	Mnemonics	Address		Remarks
ASCI Control Register A Channel 0:	CNTLA0	0	0	
ASCI Control Register A Channel 1:	CNTLA1	0	1	

MOD 2 1 0
0 0 0 Start + 7 bit Data + 1 Stop
0 0 1 Start + 7 bit Data + 2 Stop
0 1 0 Start + 7 bit Data + Parity + 1 Stop
0 1 1 Start + 7 bit Data + Parity + 2 Stop
1 0 0 Start + 8 bit Data + 1 Stop
1 0 1 Start + 8 bit Data + 2 Stop
1 1 0 Start + 8 bit Data + Parity + 1 Stop
1 1 1 Start + 8 bit Data + Parity + 2 Stop