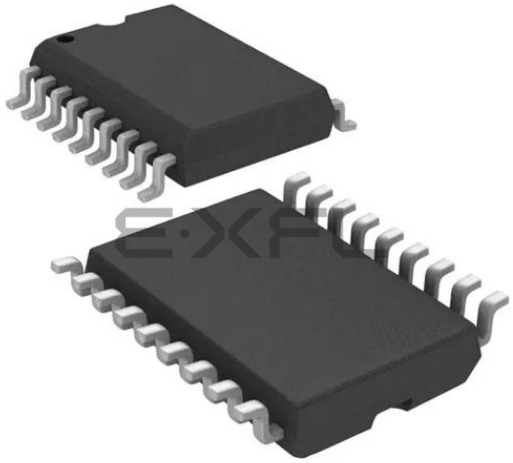

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 13 |
| Program Memory Size | 896B (512 x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 80 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 18-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 18-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c554-20-so |

## Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

| | |
|---|---|
| **Note:** | For additional information on enhancements, see Appendix A |

## CMOS Technology:

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range
  - 2.5V to 5.5V
- Commercial, Industrial and Extended temperature range
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 μA typical 3.0V, 32 kHz
  - < 1.0 μA typical standby current @ 3.0V

## Device Differences

| Device | Voltage Range | Oscillator |
|---|---|---|
| PIC16C554 | 2.5 - 5.5 | **(Note 1)** |
| PIC16C557 | 2.5 - 5.5 | **(Note 1)** |
| PIC16C558 | 2.5 - 5.5 | **(Note 1)** |

**Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.

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**TABLE 1-1: PIC16C55X FAMILY OF DEVICES**

| | | PIC16C554 | PIC16C557 | PIC16C558 |
|---|---|---|---|---|
| **Clock** | Maximum Frequency of Operation (MHz) | 20 | 20 | 20 |
| **Memory** | EPROM Program Memory (x14 words) | 512 | 2K | 2K |
| | Data Memory (bytes) | 80 | 128 | 128 |
| **Peripherals** | Timer Module(s) | TMR0 | TMR0 | TMR0 |
| **Features** | Interrupt Sources | 3 | 3 | 3 |
| | I/O Pins | 13 | 22 | 13 |
| | Voltage Range (Volts) | 2.5-5.5 | 2.5-5.5 | 2.5-5.5 |
| | Brown-out Reset | — | — | — |
| | Packages | 18-pin DIP, SOIC; 20-pin SSOP | 28-pin DIP, SOIC; 28-pin SSOP | 18-pin DIP, SOIC, SSOP |
| All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C55X Family devices use serial programming with clock pin RB6 and data pin RB7. | | | | |

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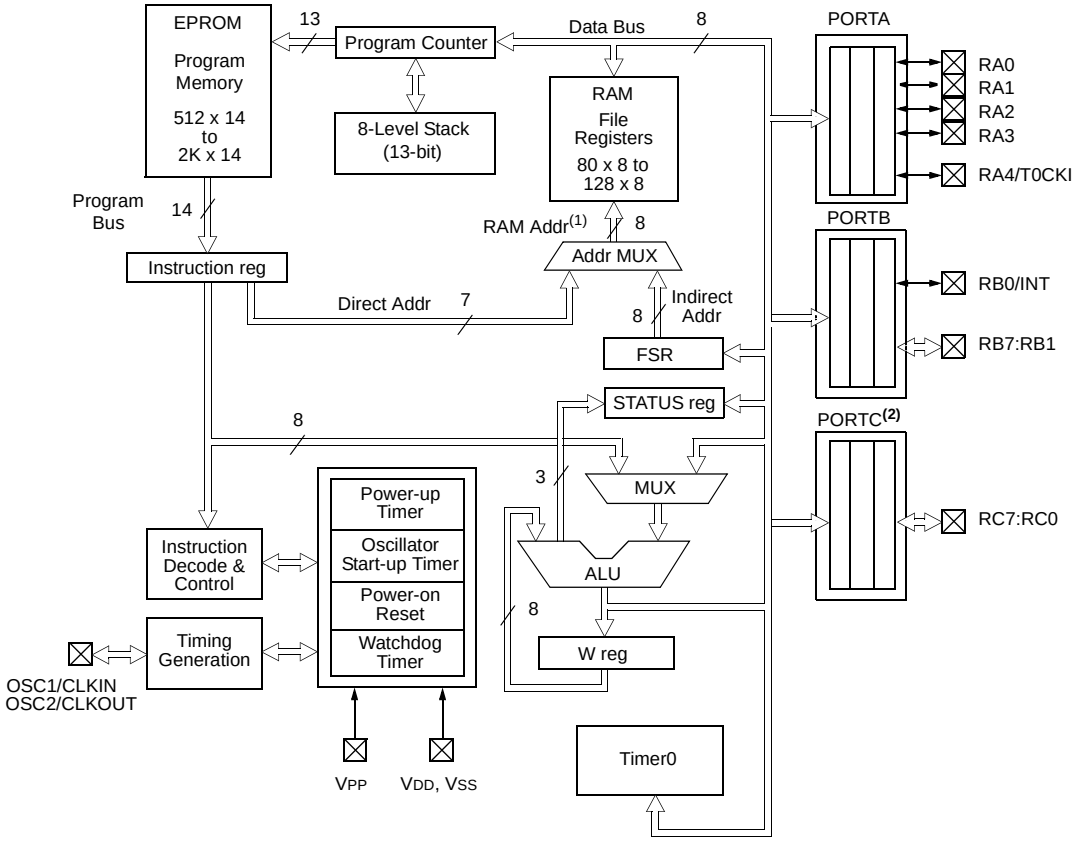
**FIGURE 3-1: BLOCK DIAGRAM**

| Device | Program Memory | Data Memory |
|---|---|---|
| PIC16C554 | 512 x 14 | 80 x 8 |
| PIC16C557 | 2 K x 14 | 128 x 8 |
| PIC16C558 | 2 K x 14 | 128 x 8 |




**Note 1:** Higher order bits are from STATUS Register.
**2:** PIC16C557 only.

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**TABLE 3-1: PIC16C55X PINOUT DESCRIPTION**

| Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | SOIC | SSOP | | | |
| OSC1/CLKIN | 16 | 16 | 18 | I | ST/CMOS | Oscillator crystal input/external clock source output. |
| OSC2/CLKOUT | 15 | 15 | 17 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| $\overline{MCLR}$/VPP | 4 | 4 | 4 | I/P | ST | Master clear (Reset) input/programming voltage input. This pin is an active low RESET to the device. |
| RA0 | 17 | 17 | 19 | I/O | ST | Bi-directional I/O port |
| RA1 | 18 | 18 | 20 | I/O | ST | Bi-directional I/O port |
| RA2 | 1 | 1 | 1 | I/O | ST | Bi-directional I/O port |
| RA3 | 2 | 2 | 2 | I/O | ST | Bi-directional I/O port |
| RA4/T0CKI | 3 | 3 | 3 | I/O | ST | Bi-directional I/O port or external clock input for TMR0. Output is open drain type. |
| RB0/INT | 6 | 6 | 7 | I/O | TTL/ST(1) | Bi-directional I/O port can be software programmed for internal weak pull-up. RB0/INT can also be selected as an external interrupt pin. |
| RB1 | 7 | 7 | 8 | I/O | TTL | Bi-directional I/O port can be software programmed for internal weak pull-up. |
| RB2 | 8 | 8 | 9 | I/O | TTL | Bi-directional I/O port can be software programmed for internal weak pull-up. |
| RB3 | 9 | 9 | 10 | I/O | TTL | Bi-directional I/O port can be software programmed for internal weak pull-up. |
| RB4 | 10 | 10 | 11 | I/O | TTL | Bi-directional I/O port can be software programmed for internal weak pull-up. Interrupt-on-change pin. |
| RB5 | 11 | 11 | 12 | I/O | TTL | Bi-directional I/O port can be software programmed for internal weak pull-up. Interrupt-on-change pin. |
| RB6 | 12 | 12 | 13 | I/O | TTL/ST(2) | Bi-directional I/O port can be software programmed for internal weak pull-up. Interrupt-on-change pin. Serial programming clock. |
| RB7 | 13 | 13 | 14 | I/O | TTL/ST(2) | Bi-directional I/O port can be software programmed for internal weak pull-up. Interrupt-on-change pin. Serial programming data. |
| RC0(3) | 18 | 18 | 18 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC1(3) | 19 | 19 | 19 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC2(3) | 20 | 20 | 20 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC3(3) | 21 | 21 | 21 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC4(3) | 22 | 22 | 22 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC5(3) | 23 | 23 | 23 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC6(3) | 24 | 24 | 24 | I/O | TTL | Bi-directional I/O port input buffer. |
| RC7(3) | 25 | 25 | 25 | I/O | TTL | Bi-directional I/O port input buffer. |
| VSS | 5 | 5 | 5,6 | P | — | Ground reference for logic and I/O pins. |
| VDD | 14 | 14 | 15,16 | P | — | Positive supply for logic and I/O pins. |

Legend: O = Output, I/O = Input/output, P = Power, — = Not used, I = Input, ST = Schmitt Trigger input, TTL = TTL input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.
**2:** This buffer is a Schmitt Trigger input when used in Serial Programming mode.
**3:** PIC16C557 only.

**TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C55X**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR Reset | Detail on Page: |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 0** | | | | | | | | | | | |
| 00h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 21 |
| 01h | TMR0 | Timer0 Module's Register | | | | | | | | xxxx xxxx | 47 |
| 02h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 21 |
| 03h | STATUS | IRP(2) | RP1(2) | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 17 |
| 04h | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | 21 |
| 05h | PORTA | — | — | — | RA4 | RA3 | RA2 | RA1 | RA0 | ---x xxxx | 23 |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | 25 |
| 07h | PORTC(4) | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | 27 |
| 08h | — | Unimplemented | | | | | | | | — | — |
| 09h | — | Unimplemented | | | | | | | | — | — |
| 0Ah | PCLATH | — | — | — | Write buffer for upper 5 bits of program counter | | | | | ---0 0000 | 21 |
| 0Bh | INTCON | GIE | (3) | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 19 |
| 0Ch | — | Unimplemented | | | | | | | | — | — |
| 0Dh-1Eh | — | Unimplemented | | | | | | | | — | — |
| 1Fh | — | Unimplemented | | | | | | | | — | — |
| **Bank 1** | | | | | | | | | | | |
| 80h | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 21 |
| 81h | OPTION | $\overline{RBPU}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 18 |
| 82h | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 21 |
| 83h | STATUS | — | — | RP0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 17 |
| 84h | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | 21 |
| 85h | TRISA | — | — | — | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | ---1 1111 | 23 |
| 86h | TRISB | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | 1111 1111 | 25 |
| 87h | TRISC(4) | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 1111 1111 | 27 |
| 88h | — | Unimplemented | | | | | | | | — | — |
| 89h | — | Unimplemented | | | | | | | | — | — |
| 8Ah | PCLATH | — | — | — | Write buffer for upper 5 bits of program counter | | | | | ---0 0000 | 21 |
| 8Bh | INTCON | GIE | (3) | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 19 |
| 8Ch | — | Unimplemented | | | | | | | | — | — |
| 8Dh | — | Unimplemented | | | | | | | | — | — |
| 8Eh | PCON | — | — | — | — | — | — | $\overline{POR}$ | — | ---- --0- | 20 |
| 8Fh-9Eh | — | Unimplemented | | | | | | | | — | — |
| 9Fh | — | Unimplemented | | | | | | | | — | — |

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

**2:** IRP & RP1 bits are reserved, always maintain these bits clear.

**3:** Bit 6 of INTCON register is reserved for future use. Always maintain this bit as clear.

**4:** PIC16C557 only.

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## 5.0 I/O PORTS

The PIC16C554 and PIC16C558 have two ports, PORTA and PORTB. The PIC16C557 has three ports, PORTA, PORTB and PORTC.

### 5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open-drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

**Note 1:** On RESET, the TRISA register is set to all inputs.

**FIGURE 5-1: BLOCK DIAGRAM OF PORT PINS RA<3:0>**

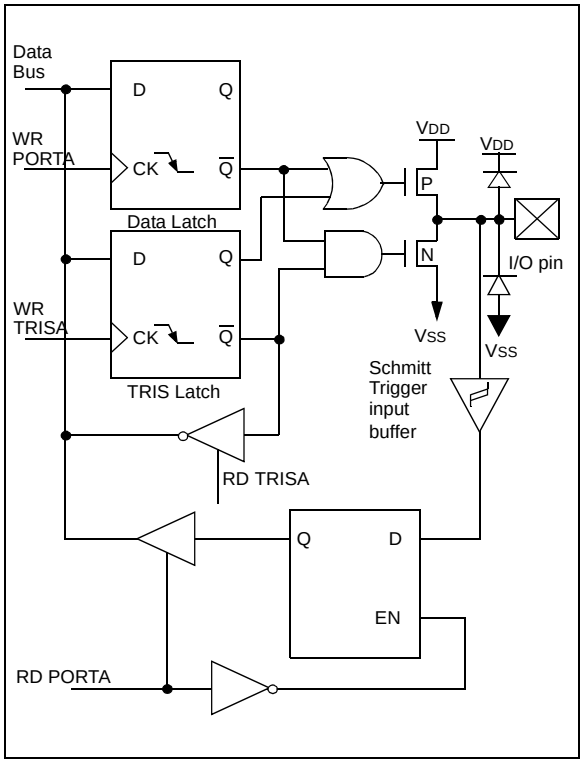
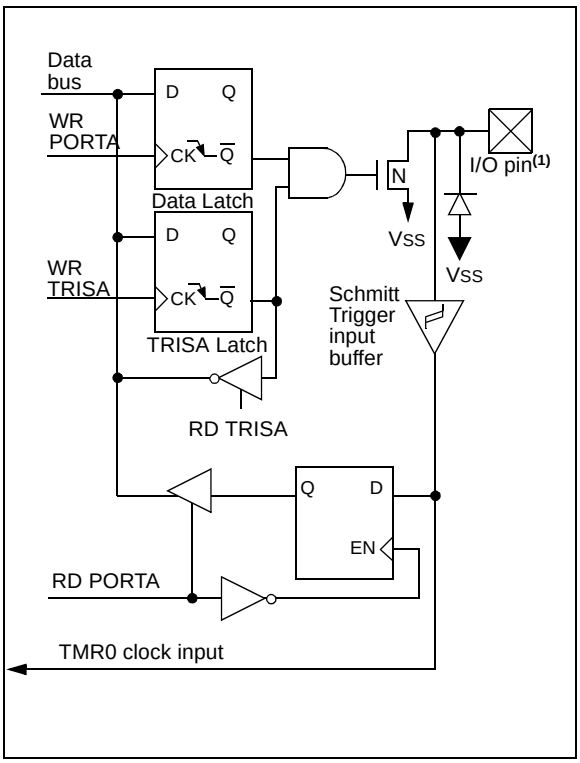



**FIGURE 5-2: BLOCK DIAGRAM OF RA4 PIN**



## 6.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16C55X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

1. OSC selection
2. RESET
3. Power-on Reset (POR)
4. Power-up Timer (PWRT)
5. Oscillator Start-Up Timer (OST)
6. Interrupts
7. Watchdog Timer (WDT)
8. SLEEP
9. Code protection
10. ID Locations
11. In-circuit serial programming™

The PIC16C55X has a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), which is intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

### 6.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h – 3FFFh), which can be accessed only during programming.

**NOTES:**

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**BTFSS** **Bit Test f, Skip if Set**

Syntax: [ *label* ] BTFSS f,b

Operands: $0 \le f \le 127$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 01 | 11bb | bfff | ffff |

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address HERE
After Instruction
if FLAG<1> = 0,
PC = address FALSE
if FLAG<1> = 1,
PC = address TRUE

**CALL** **Call Subroutine**

Syntax: [ *label* ] CALL k

Operands: $0 \le k \le 2047$

Operation: (PC)+ 1→ TOS,
k → PC<10:0>,
(PCLATH<4:3>) → PC<12:11>

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 10 | 0kkk | kkkk | kkkk |

Description: Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example

```
HERE    CALL    THERE
```

Before Instruction
PC = Address HERE
After Instruction
PC = Address THERE
TOS = Address HERE+1

**CLRF** **Clear f**

Syntax: [ *label* ] CLRF f

Operands: $0 \le f \le 127$

Operation: 00h → (f)
1 → Z

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 0001 | 1fff | ffff |

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example

```
CLRF    FLAG_REG
```

Before Instruction
FLAG_REG=0x5A
After Instruction
FLAG_REG=0x00
Z =1

## 10.0 ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings †**

Ambient Temperature under bias ..... -40° to +125°C

Storage Temperature ..... -65° to +150°C

Voltage on any pin with respect to $V_{SS}$ (except $V_{DD}$ and $\overline{MCLR}$) ..... -0.6V to $V_{DD}$ +0.6V

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V

Total power Dissipation **(Note 1)** ..... 1.0W

Maximum Current out of $V_{SS}$ pin ..... 300 mA

Maximum Current into $V_{DD}$ pin ..... 250 mA

Input Clamp Current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) ..... ±20 mA

Output Clamp Current, $I_{OK}$ ($V0 < 0$ or $V0 > V_{DD}$) ..... ±20 mA

Maximum Output Current sunk by any I/O pin ..... 25 mA

Maximum Output Current sourced by any I/O pin ..... 25 mA

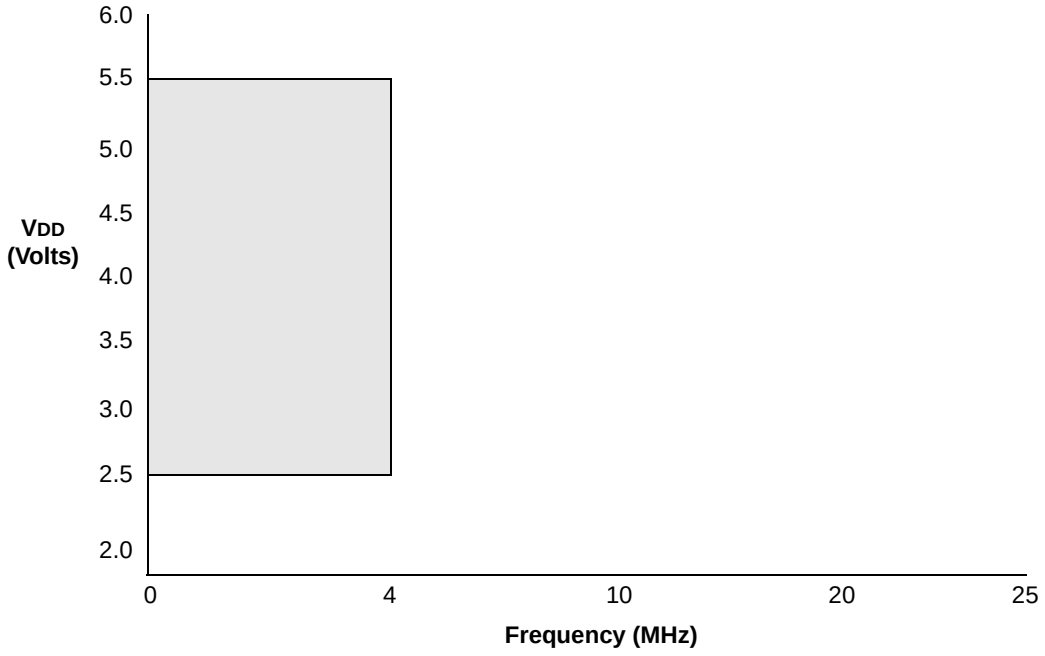
Maximum Current sunk by PORTA, PORTB and PORTC ..... 200 mA

Maximum Current sourced by PORTA, PORTB and PORTC ..... 200 mA

**Note 1:** Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(Vol \times I_{OL})$

† **NOTICE**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

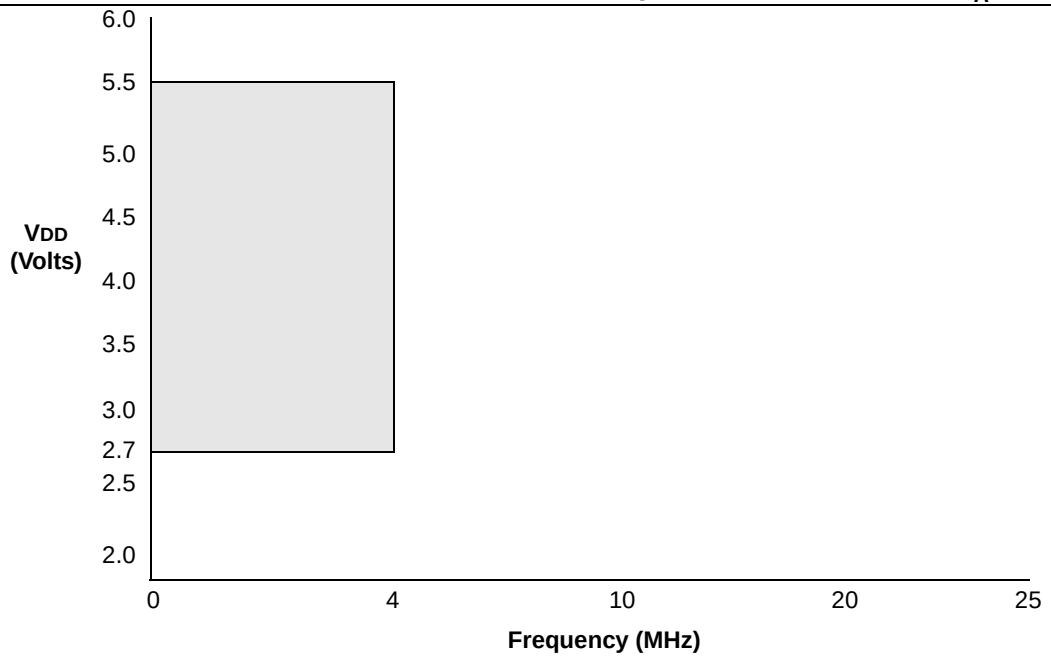
**FIGURE 10-3: VOLTAGE-FREQUENCY GRAPH, 0°C ≤ $T_A$ ≤ +85°C**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 10-4: PIC16LC554/557/558 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ $T_A$ ≤ 0°C**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 10-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**

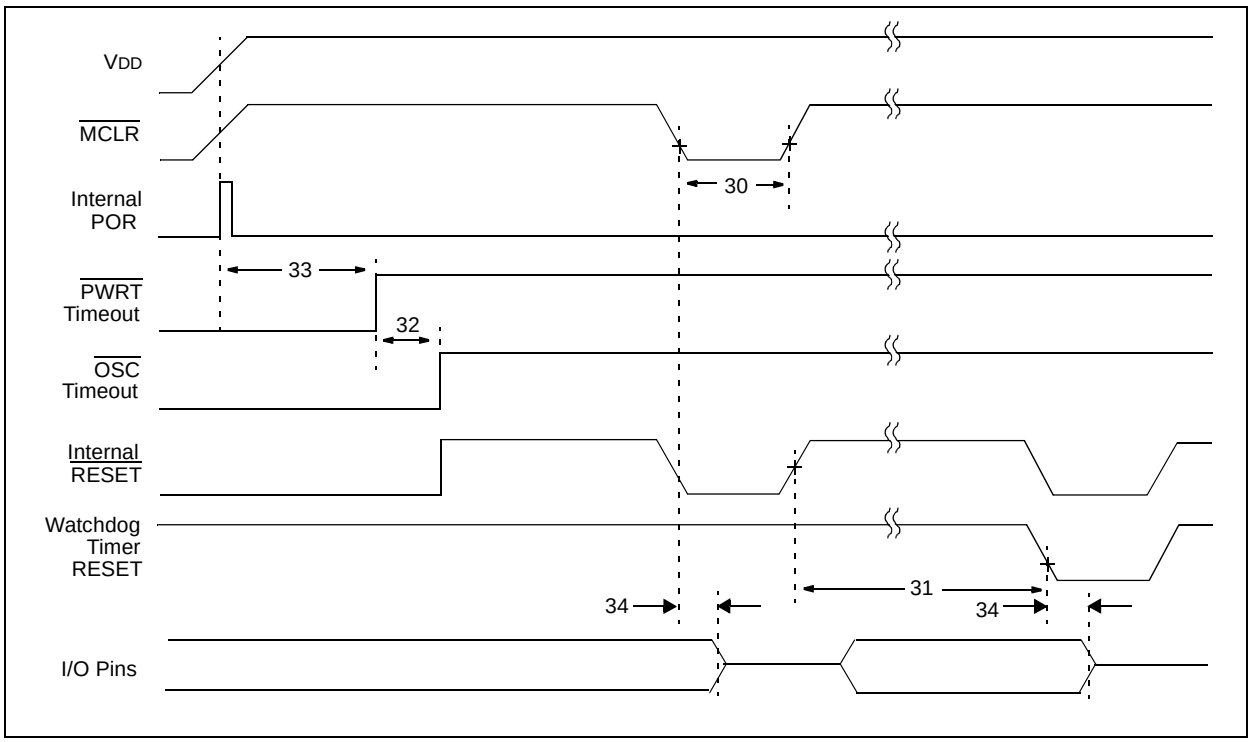



**TABLE 10-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000 | — | — | ns | -40° to +85°C |
| 31 | Twdt | Watchdog Timer Timeout Period (No Prescaler) | 7* | 18 | 33* | ms | VDD = 5.0V, -40° to +85°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| 33 | Tpwrt | Power-up Timer Period | 28* | 72 | 132* | ms | VDD = 5.0V, -40° to +85°C |
| 34 | TIOZ | I/O hi-impedance from $\overline{\text{MCLR}}$ low | | — | 2.0* | µs | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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**NOTES:**

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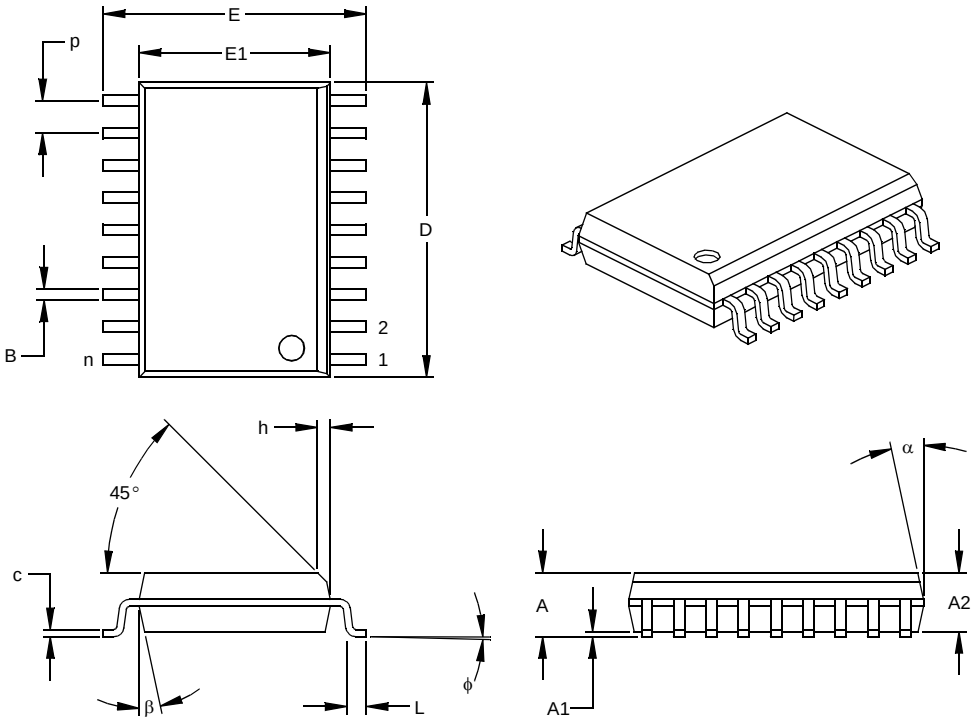
### 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



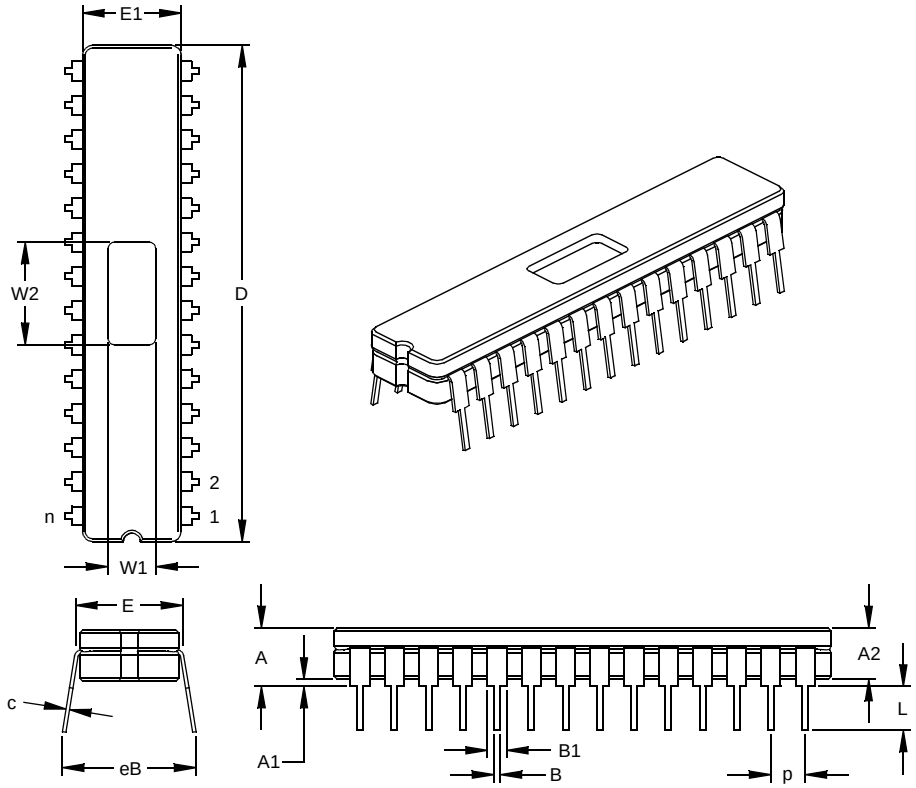

| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .446 | .454 | .462 | 11.33 | 11.53 | 11.73 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .012 | 0.23 | 0.27 | 0.30 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

### 28-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .170 | .183 | .195 | 4.32 | 4.64 | 4.95 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .023 | .030 | 0.38 | 0.57 | 0.76 |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Ceramic Pkg. Width | E1 | .285 | .290 | .295 | 7.24 | 7.37 | 7.49 |
| Overall Length | D | 1.430 | 1.458 | 1.485 | 36.32 | 37.02 | 37.72 |
| Tip to Seating Plane | L | .135 | .140 | .145 | 3.43 | 3.56 | 3.68 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .058 | .065 | 1.27 | 1.46 | 1.65 |
| Lower Lead Width | B | .016 | .019 | .021 | 0.41 | 0.47 | 0.53 |
| Overall Row Spacing § | eB | .345 | .385 | .425 | 8.76 | 9.78 | 10.80 |
| Window Width | W1 | .130 | .140 | .150 | 3.30 | 3.56 | 3.81 |
| Window Length | W2 | .290 | .300 | .310 | 7.37 | 7.62 | 7.87 |

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-058
Drawing No. C04-080

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## APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
3. Data memory paging is slightly redefined. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. RESET vector is changed to 0000h.
9. RESET of all registers is revised. Three different RESET (and wake-up) types are recognized. Registers are reset differently.
10. Wake-up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt-on-change feature.
13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
14. FSR is made a full 8-bit register.
15. “In-circuit programming” is made possible. The user can program PIC16C55X devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on Reset ($\overline{\text{POR}}$) status bit.
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. PORTA inputs are now Schmitt Trigger inputs.

## APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16C55X, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to 0000h.

## APPENDIX C: REVISION HISTORY

**Revision E (January 2013)**

Added a note to each package outline drawing.

# INDEX

**NOTES:**

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