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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	80 × 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c554t-04i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 PIC16C55X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C55X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART[®] and PROMATE[®] programmers both support programming of the PIC16C55X.

2.2 One-Time Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium-to-high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices, but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP[™]) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.





5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up ($\approx 200 \ \mu A$ typical). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB (this will end the mismatch condition)
- Clear flag bit RBIF

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on mismatch feature, together with software configurable pull-ups on these four pins, allows easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the Microchip *Embedded Control Handbook*.)

Note 1: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.



FIGURE 5-3: BLOCK DIAGRAM OF RB7:RB4 PINS

5.3 PORTC and TRISC Registers⁽¹⁾

PORTC is a 8-bit wide latch. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

A '1' in the TRISC register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISC register puts the contents of the output latch on the selected pin(s).

Reading the PORTC register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch

FIGURE 5-5: BLOCK DIAGRAM OF



Name	Bit #	Buffer Type	Function	
RC0	Bit 0	TTL	Bi-directional I/O port.	
RC1	Bit 1	TTL	Bi-directional I/O port.	
RC2	Bit 2	TTL	Bi-directional I/O port.	
RC3	Bit 3	TTL	Bi-directional I/O port.	
RC4	Bit 4	TTL	Bi-directional I/O port.	
RC5	Bit 5	TTL	Bi-directional I/O port.	
RC6	Bit 6	TTL	Bi-directional I/O port.	
RC7	Bit 7	TTL	Bi-directional I/O port.	

Legend: ST = Schmitt Trigger, TTL = TTL input

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC AND TRISC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged Note 1: PIC16C557 ONLY.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;	Initial PORT settings: PORTB<7:4> Inputs
;	
;	PORTB<3:0> Outputs
;	PORTB<7:6> have external pull-up and are
;	not connected to other circuitry
;	
;	PORT latch PORT pins
;	
;	
	BCF PORTB, 7 ; 01pp pppp 11pp pppp
	BCF PORTB, 6 ; 10pp pppp 11pp pppp
	BSF STATUS, RPO ;
	BCF TRISB, 7 ; 10pp pppp 11pp pppp
	BCF TRISB, 6 ; 10pp pppp 10pp pppp

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle, as shown in Figure 5-6. Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with an NOP or another instruction not accessing this I/O port.

	Q1 Q2 Q3 Q4	$Q_1 Q_2 Q_3 Q_4$	Q1 Q2 Q3 Q4	$Q_1 Q_2 Q_3 Q_4$
PC	PC	PC + 1	X PC + 2	PC + 3
Instruction fetched	MOVWF PORTB Write to	MOVF PORTB, W Read PORTB	NOP	NOP
RB <7:0>				i
		Tpd 🔶	Port pin sampled here	1 1 1
	1 I	Execute MOVWF PORTB	Execute MOVF PORTB, W	Execute NOP

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6.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a pre-packaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with series resonance, or one with parallel resonance.

Figure 6-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 6-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 6-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 6-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



6.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 6-5 shows how the R/C combination is connected to the PIC16C55X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).



FIGURE 6-5: RC OSCILLATOR MODE

6.3 RESET

The PIC16C55X differentiates between various kinds of RESET:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during SLEEP
- WDT Reset (normal operation)
- WDT wake-up (SLEEP)

Some registers are not affected in any RESET condition; their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset, on MCLR or WDT Reset and on MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 6-4. These bits are used in software to determine the nature of the RESET. See Table 6-6 for a full description of RESET states of all registers. A simplified block diagram of the on-chip RESET circuit is shown in Figure 6-6.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See Table 10-3 for pulse width specification.





6.4.5 POWER CONTROL/STATUS REGISTER (PCON)

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET if POR is '0', it will indicate that a Poweron Reset must have occurred (VDD may have gone too low).

TABLE 6-3: TIMEOUT IN VARIOUS SITUATIONS

Oscillator	Pow	Wake-up from		
Configuration	PWRTE = 0	PWRTE = 1	SLEEP	
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	1024 Tosc	
RC	72 ms	—	—	

TABLE 6-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	то	PD		
0	1	1	Power-on Reset	
0	0	Х	Illegal, TO is set on POR	
0	Х	0	egal, PD is set on POR	
1	0	u	VDT Reset	
1	0	0	VDT Wake-up	
1	u	u	MCLR Reset during normal operation	
1	1	0	MCLR Reset during SLEEP	





Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other RESETS
2007h	Config. bits		Reserved	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0		
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to WDT. Lines 5-7 are required only if the desired postscaler rate is 1:1 (PS<2:0> = 000) or 1:2 (PS<2:0> = 001).

EXAMPLE 7-1:	CHANGING PRESCALER
	(TIMER0→WDT)

	•	/
BCF	STATUS, RPO	;Skip if already in
		;Bank 0 CLRWDT Clear WDT
CLRF	TMR0	;Clear TMR0 & Prescaler
BSF	STATUS, RPO	;Bank 1
MOVLW	'00101111 <i>'</i> b	;These 3 lines (5, 6, 7)
MOVWF	OPTION	;Are required only if
		;Desired PS<2:0> are
		;CLRWDT 000 or 001
MOVLW	'00101xxx'b	;Set Postscaler to
MOVWF	OPTION	;Desired WDT rate
BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 7-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

	•	
CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		;prescale value and
		;clock source
MOVWF	OPTION	
BCF	STATUS, RPO	

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	TMR0	Timer0 m	odule's registe	r						xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	Reserved	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0',

Note 1: Shaded bits are not used by TMR0 module.

NOTES:

RRF	Rotate R	light f	throu	gh (Carry
Syntax:	[label]	RRF 1	,d		
Operands:	$0 \le f \le 127$ d \in [0,1]				
Operation:	See description below				
Status Affected:	С				
Encoding:	00	1100	dff	f	ffff
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.				
	C Register f				
Words:	1				
Cycles:	1				
Example	RRF		REG	1,0	
	Before Instruction				
	REG1	= 1	L110	011	.0
	С	= ()		
	After Instru	uction			
	REG1	= 1	L110	011	.0
	W	= (0111	001	.1
	С	= ()		

SLEEP

Syntax:	[label]	SLEEP					
Operands:	None						
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \ prescaler, \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$						
Status Affected:	$\overline{\text{TO}}, \overline{\text{PD}}$						
Encoding:	00	0000	0110	0011			
Description:	The power-down status bit, <u>PD</u> is cleared. Timeout status bit, <u>TO</u> is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 6.8 for more details.						
Words:	1						
Cycles:	1						
Example:	SLEEP						

SUBLW	Subtract W from Literal				
Syntax:	[<i>label</i>] SUBLW k				
Operands:	$0 \le k \le 255$				
Operation:	k - (W) \rightarrow	$k - (W) \to (W)$			
Status Affected:	C, DC, Z	C, DC, Z			
Encoding:	11	110x	kkkk kkkk		
Description:	The W reg plement m 'k'. The res	The W register is subtracted (2's com- plement method) from the eight bit literal 'k'. The result is placed in the W register.			
Words:	1				
Cycles:	1				
Example 1:	SUBLW	0x02			
	Before In	structio	n		
	W	=	1		
	С	=	?		
	After Inst	After Instruction			
	W	=	1		
	С	=	1; result is positive		
Example 2:	Before Instruction				
	W	=	2		
	С	=	?		
	After Inst	ruction			
	W	=	0		
	С	=	1; result is zero		
Example 3:	Before Instruction				
	W	=	3		
	С	=	?		
	After Inst	ruction			
	W	=	0xFF		
	С	=	u; result is nega-		

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9.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

9.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

9.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily re configured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows environment were chosen to best make these features available to you, the end user.

9.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †	
Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{\text{MCLR}}$)	0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into VDD pin	250 mA
Input Clamp Current, Iik (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (V0 < 0 or V0 > VDD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA, PORTB and PORTC	200 mA
Maximum Current sourced by PORTA, PORTB and PORTC	200 mA
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum	$\Sigma \{(VDD-VOH) \times IOH\} + \Sigma(VOI \times IOL)\}$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16C55X



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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	x <u>xx xxx</u>	Examples:
Device	Temperature Package Pattern Range	a) PIC17C756–16L Commercial Temp., PLCC package, 16 MHz, normal VDD limits
Device	PIC17C756: Standard VDD range PIC17C756T: (Tape and Reel) PIC17LC756: Extended VDD range	 b) PIC17LC756–08/PT Commercial Temp., TQFP package, 8MHz, extended VDD limits c) PIC17C756–33I/PT Industrial Temp., TQFP is a set that a set that the set the se
Temperature Range	$- = 0^{\circ}C \text{ to } +70^{\circ}C$ I = -40°C to +85°C	I QFP package, 33 MHz, normal VDD limits
Package	CL = Windowed LCC PT = TQFP L = PLCC	
Pattern	QTP, SQTP, ROM Code (factory specified) or Special Requirements. Blank for OTP and Windowed devices.	

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

2. The Microchip Worldwide Site (www.microchip.com)

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