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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c558-04-ss

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NOTES:

NOTES:

FIGURE 4-3:

DATA MEMORY MAP FOR THE PIC16C554

File Address	3		File Address	
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h	
01h	TMR0	OPTION	81h	
02h	PCL	PCL	82h	
03h	STATUS	STATUS	83h	
04h	FSR	FSR	84h	
05h	PORTA	TRISA	85h	
06h	PORTB	TRISB	86h	
07h			87h	
08h			88h	
09h			89h	
0Ah	PCLAIH	PCLAIH	8Ah	
0Bh	INTCON	INICON	8Bh	
0Ch			8Ch	
		DCON		
0En		PCON	8En	
10h				
1011 11h			9011	
12h			92h	
13h			- 93h	
14h			94h	
15h			95h	
16h			96h	
17h			97h	
18h			98h	
19h			99h	
1Ah			9Ah	
1Bh			9Bh	
1Ch			9Ch	
1Dh			9Dh	
1Eh			9Eh	
1Fh			9Fh	
20h	General Purpose		A0h	
6Fh	Register			
70h				
ı I			\neg	
7Fh			FFh	
7111	Bank 0	Bank 1		
Unimp Note 1:	Unimplemented data memory locations, read as '0'. Note 1: Not a physical register.			

FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C557

File Address	5		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch			8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh			9Fh
20h			A0h
-	General	General	7.011
	Purpose Register	Purpose	
	register		BFh
			C0h
ſ			
7Eh			FFh
1 611 4	Bank 0	Bank 1	
Unimp	lemented data mer	mory locations	ad as '0'
Note 1: Not a physical register.			

FIGURE 4-5: DATA MEMORY MAP FOR THE PIC16C558

File Address	3		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch			8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h		_	97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh		_	9Eh
1Fh			9Fh
20h			A0h
	General	General	71011
	Purpose Register	Purpose Register	
	regiotor	rtogiotor	BFh
			C0h
			\neg
756			FFb
7 - 11 -	Bank 0	Bank 1	
Unimp Note 1:	lemented data mer Not a physical reg	nory locations, re ister.	ead as '0'.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The Special Function Registers can be classified into two sets (core and peripheral). The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature. bit 5

4.2.2.2 OPTION Register

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note 1: To achieve a 1:1 prescaler assignment for
TMR0, assign the prescaler to the WDT
(PSA = 1).

REGISTER 4-2:	OPTION REGISTER	(ADDRESS 81H)
---------------	------------------------	---------------

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

- bit 7 **RBPU**: PORTB Pull-up Enable bit
 - 1 = PORTB pull-ups are disabled
 - 0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit

- 1 = Interrupt on rising edge of RB0/INT pin
- 0 = Interrupt on falling edge of RB0/INT pin
- TOCS: TMR0 Clock Source Select bit
 - 1 = Transition on RA4/T0CKI pin
 - 0 = Internal instruction cycle clock (CLKOUT)
- bit 4 TOSE: TMR0 Source Edge Select bit
 - 1 = Increment on high-to-low transition on RA4/T0CKI pin
 - 0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

- 1 = Prescaler is assigned to the WDT
- 0 = Prescaler is assigned to the Timer0 module

bit 2-0 PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1 : 128	1:64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2.2.4 PCON Register

The PCON register contains a flag bit to differentiate between a Power-on Reset, an external MCLR Reset or WDT Reset. See Section 6.3 and Section 6.4 for detailed RESET operation.

REGISTER 4-4: PCON REGISTER (ADDRESS 8Eh) U-0 U-0 U-0 R/W-0 U-0 U-0 U-0 U-0 POR bit7 bit 7-2 Unimplemented: Read as '0' bit 1 POR: Power-on Reset status bit 1 = No Power-on Reset occurred 0 = Power-on Reset occurred bit 0 Unimplemented: Read as '0' Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit0

6.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)

6.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6V - 1.8V). To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607 "Power-up Trouble Shooting".

6.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) timeout on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the <u>VDD</u> to rise to an acceptable level. A configuration bit, <u>PWRTE</u> can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-Up Time delay will vary from chip to chip and due to VDD, temperature and process variation. See DC parameters for details.

6.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST timeout is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

6.4.4 TIMEOUT SEQUENCE

On power-up, the timeout sequence is as follows: First PWRT timeout is invoked after POR has expired, then OST is activated. The total timeout will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (PWRT disabled), there will be no timeout at all. Figure 6-7, Figure 6-8 and Figure 6-9 depict timeout sequences.

Since the timeouts occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the timeouts will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 6-8). This is useful for testing purposes or to synchronize more than one PIC16C55X device operating in parallel.

Table 6-5 shows the RESET conditions for some special registers, while Table 6-6 shows the RESET conditions for all the registers.

6.4.5 POWER CONTROL/STATUS REGISTER (PCON)

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET if POR is '0', it will indicate that a Poweron Reset must have occurred (VDD may have gone too low).

TABLE 6-3: TIMEOUT IN VARIOUS SITUATIONS

Oscillator	Pow	Wake-up from	
Configuration	PWRTE = 0	PWRTE = 1	SLEEP
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	1024 Tosc
RC	72 ms	—	—

TABLE 6-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	то	PD	
0	1	1	Power-on Reset
0	0	Х	Illegal, TO is set on POR
0	Х	0	Illegal, PD is set on POR
1	0	u	WDT Reset
1	0	0	WDT Wake-up
1	u	u	MCLR Reset during normal operation
1	1	0	MCLR Reset during SLEEP

6.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This will have to be implemented in software.

Example 6-1 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 6-1:

- Stores the W register
- Stores the STATUS register in Bank 0
- · Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 6-1: SAVING THE STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;copy W to TEMP ;register, could be in
		;either bank
SWAPF	STATUS,W	;swap STATUS to be
		;saved into W
BCF	STATUS, RPO	;change to bank0
		;regardless of
		;current bank
MOVWF	STATUS_TEMP	;save STATUS to bank0
		;register
:		
:		
:		
SWAPF	STATUS_TEMP, W	;swap STATUS_TEMP
		;register into W, sets
		;bank to original state
MOVWF	STATUS	;move W into STATUS
		;register
SWAPF	W_TEMP,F	;swap W_TEMP
SWAPF	W_TEMP,W	;swap W_TEMP into W

6.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT timeout generates a device RESET. If the device is in SLEEP mode, a WDT timeout causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 6.1).

6.7.1 WDT PERIOD

The WDT has a nominal timeout period of 18 ms, (with no prescaler). The timeout periods vary with temperature, VDD and process variations from part-to-part (see DC specs). If longer timeout periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, timeout periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer timeout.

6.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

7.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the TOSE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before reenabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.



FIGURE 7-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER



NOTES:

PIC16C55X

BCF	Bit Clea	ar f						
Syntax:	[label]	BCF 1	f,b					
Operands:	$0 \le f \le 1$ $0 \le b \le 1$	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$						
Operation:	$0 \rightarrow (f < b >)$							
Status Affected:	None							
Encoding:	01	00bb	bfff	ffff				
Description:	Bit 'b' in register 'f' is cleared.							
Words:	1							
Cycles:	1							
Example	BCF	FLAG_F	REG, 7					
	Before Instruction FLAG_REG = 0xC7 After Instruction FLAG_REG = 0x47							

Bit S	et f
-------	------

BSF

Syntax:	[<i>label</i>] B	SF f,b							
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ 0 \leq b \leq 7 \end{array}$	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$							
Operation:	$1 \rightarrow (f < b;$	$1 \rightarrow (f < b >)$							
Status Affected:	None								
Encoding:	01	01bb	bfff	ffff					
Description:	Bit 'b' in re	Bit 'b' in register 'f' is set.							
Words:	1								
Cycles:	1								
Example	BSF	FLAG_F	REG, 7	,					
	Before In	struction	1						
	FLA	G_REG	= 0x	0A					
	After Inst	ruction							
	FLA	G_REG	= 0x	8A					

BTFSC	Bit Test, Skip if Clear								
Syntax:	[<i>label</i>] B	[label] BTFSC f,b							
Operands:	$\begin{array}{l} 0 \leq f \leq 12 \\ 0 \leq b \leq 7 \end{array}$.7							
Operation:	skip if (f<	b>) = 0							
Status Affected:	None								
Encoding:	01	10bb	bfff	ffff					
Description:	If bit 'b' in instruction the next in current ins carded, ar making thi	If bit 'b' in register 'f' is '0' then the next instruction is skipped. If bit 'b' is '0' then the next instruction fetched during the current instruction execution is dis- carded, and a NOP is executed instead, making this a two-cycle instruction							
Words:	1								
Cycles:	1(2)								
Example	HERE FALSE TRUE	FLAG,1 PROCES	S_CODE						
	Before In	struction							
	PC	= ad	ldress HE	RE					
	After Inst	ruction							
	if FL	AG<1> = (), Idress TD	TTF					
	if FL	_ au AG<1> = [/]	1,						
	PC = address FALSE								

10.2 DC Characteristics: PIC16C55X (Commercial, Industrial, Extended) PIC16LC55X(Commercial, Industrial, Extended)

			Standard Operating tem	perating	Conditions (re -40°C ≤ T	u nless A ≤ +8	s otherwise stated) 5°C for industrial and
DC Cha	racteris	stics	1 0	•	$0^{\circ}C \leq 1$	A ≤ +7	70°C for commercial and
				\ /-	-40°C ≤ T	4 ≤ +1 	25°C for automotive
			Operating volt	age vo	D range as de	scribed	a in DC spec Table 10-1
Param. No.	Sym	Characteristic	Min	Тур†	Max	Unit	Conditions
	VIL	Input Low Voltage					
		I/O ports					
D030		with TTL buffer	Vss	—	0.8V 0.15 Vdd	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	Vss		0.2 Vdd	V	
D032		MCLR, RA4/T0CKI,OSC1 (in RC mode)	Vss	-	0.2 Vdd	V	(Note1)
D033		OSC1 (in XT* and HS)	Vss	—	0.3 Vdd	V	
		OSC1 (in LP*)	Vss	—	0.6 Vdd-1.0	V	
	Vін	Input High Voltage		1			1
		I/O ports		—			
D040		with TTL buffer	2.0V 0.8 + 0.25 VDD		Vdd Vdd	V V	VDD = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8V		Vdd		
D042		MCLR RA4/T0CKI	0.8 Vdd	—	Vdd	V	
D043 D043A		OSC1 (XT*, HS and LP*) OSC1 (in RC mode)	0.7 Vdd 0.9 Vdd	—	Vdd	V	(Note1)
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS
	lı∟	Input Leakage Current ⁽²⁾⁽³⁾					
		I/O ports (Except PORTA)			±1.0	μA	VSS \leq VPIN \leq VDD, pin at hi-impedance
D060		PORTA	—	_	±0.5	μA	$Vss \le VPIN \le VDD$, pin at hi-impedance
D061		RA4/T0CKI	—	—	±1.0	μΑ	$Vss \leq V \text{PIN} \leq V \text{DD}$
D063		OSC1, MCLR	—	_	±5.0	μA	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration
	Vol	Output Low Voltage					
D080		I/O ports	—	-	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C
			—	—	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C
D083		OSC2/CLKOUT	—	—	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C
		(RC only)	—	—	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C
	Vон	Output High Voltage ⁽³⁾					
D090		I/O ports (Except RA4)	Vdd-0.7	_		V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C55X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

10.2 DC Characteristics: PIC16C55X (Commercial, Industrial, Extended) PIC16LC55X(Commercial, Industrial, Extended) (Continued)

DC Cha	racteris	tics	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial and $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial and $-40^{\circ}C \le TA \le +125^{\circ}C$ for automotiveOperating voltage VDD range as described in DC spec Table 10-1					
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Unit	Conditions	
			Vdd-0.7	_	—	V	Iон=-2.5 mA, Vdd=4.5V, +125°С	
D092		OSC2/CLKOUT	Vdd-0.7	_	—	V	IOH=-1.3 mA, VDD=4.5V, -40° to +85°С	
		(RC only)	Vdd-0.7	_	—	V	IOH=-1.0 mA, VDD=4.5V, +125°С	
*	Vod	Open-Drain High Voltage			10*	V	RA4 pin	
		Capacitive Loading Specs on	Output Pins					
D100	COSC 2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.	
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C55X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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10.3 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

Т			
F	Frequency	Т	Time
Lowercas	e subscripts (pp) and their meanings:		
рр			
ck	CLKOUT	OS	OSC1
io	I/O port	t0	ТОСКІ
mc	MCLR		
Uppercas	e letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-5: LOAD CONDITIONS



Package Marking Information (Cont'd)



Example PIC16C558 -04I / S0218 S0218 9818 CDK

 \cap



18-Lead CERDIP Windowed



Example



28-Lead CERDIP Windowed



Example



28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MO-095

Drawing No. C04-070

28-Lead Ceramic Dual In-line with Window (JW) - 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Tip to Seating Plane	L	.135	.140	.145	3.43	3.56	3.68
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.290	.300	.310	7.37	7.62	7.87

Significant Characteristic JEDEC Equivalent: MO-058 Drawing No. C04-080

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	А	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	ф	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units		INCHES MILLIMETE			IILLIMETERS	S*
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-150

Drawing No. C04-073

A2