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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K × 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c558-04i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTES:

# PIC16C55X

# FIGURE 3-1: BLOCK DIAGRAM



### 4.2.2.1 STATUS Register

The STATUS register, shown in Figure 4-2, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as the destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000uu1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions be used to alter the STATUS register because these instructions do not affect any status bits. For other instructions, not affecting any status bits, see the "Instruction Set Summary".

- Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16C55X and should be programmed as '0'. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
  - 2: The <u>C</u> and <u>DC</u> bits operate as a Borrow and <u>Digit</u> Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 4-1:	STATUS REGISTER (ADDRESS 03h OR 83h	h)
---------------	-------------------------------------	----

	Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
	IRP	RP1	RP0	TO	PD	Z	DC	С
	bit7							bit0
bit 7	<b>IRP</b> : Register 1 = Bank 2, 3 0 = Bank 0, 1 The IRP bit is	r Bank Select b 3 (100h - 1FFh) 1 (00h - FFh) s reserved on th	it (used for Ir ne PIC16C55	ndirect addre X, always m	ssing) aintain this bit	clear		
bit 6-5	<b>RP1:RP0</b> : Re 11 = Bank 3 10 = Bank 2 01 = Bank 1 00 = Bank 0 Each bank is	egister Bank Se (180h - 1FFh) (100h - 17Fh) (80h - FFh) (00h - 7Fh) 128 bytes. The	elect bits (use RP1 bit is re	d for Direct a	addressing) ne PIC16C553	K, always main	tain this bit cl	ear.
bit 4	<b>TO</b> : Timeout 1 = After pow 0 = A WDT ti	bit /er-up, CLRWDT meout occurred	instruction, d	Or SLEEP ins	truction			
bit 3	<b>PD</b> : Power-de 1 = After pow 0 = By execu	own bit /er-up or by the /tion of the SLE	CLRWDT ins	truction				
bit 2	<b>Z</b> : Zero bit 1 = The resu 0 = The resu	It of an arithme	tic or logic op tic or logic op	peration is ze	ro t zero			
bit 1	DC: Digit ca reversed) 1 = A carry-o 0 = No carry-	rry/borrow bit ( ut from the 4th out from the 4tl	ADDWF, AI	of the result it of the result	LW, SUBWF occurred It	instructions) (	for borrow th	e polarity is
bit 0	<b>C</b> : Carry/borr 1 = A carry-o 0 = No carry-	ow bit (ADDWF , ut from the Mos out from the Mo	ADDLW, SU st Significant ost Significar	BLW, SUBWF bit of the res at bit of the re	instructions) ult occurred sult occurred			
Note 1:	For borrow the operand. For source registe	e polarity is reve rotate (RRF, RL er.	ersed. A subt F) instructior	raction is exe as, this bit is	ecuted by add loaded with ei	ing the two's c ther the high o	omplement of r low order bi	the second t of the
	Legend:							
	R = Readabl	e bit	W = Wri	table bit	U = Unim	plemented bit,	read as '0'	

- n = Value at POR reset

'0' = Bit is cleared

'1' = Bit is set

x = Bit is unknown

# 5.0 I/O PORTS

The PIC16C554 and PIC16C558 have two ports, PORTA and PORTB. The PIC16C557 has three ports, PORTA, PORTB and PORTC.

# 5.1 PORTA and TRISA Registers

PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open-drain output. Port RA4 is multiplexed with the T0CKI clock input. All other RA port pins have Schmitt Trigger input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as input or output.

A '1' in the TRISA register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISA register puts the contents of the output latch on the selected pin(s).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Note 1: On RESET, the TRISA register is set to all inputs.

FIGURE 5-1: BLOCK DIAGRAM OF PORT PINS RA<3:0>



# FIGURE 5-2: BL

BLOCK DIAGRAM OF RA4



# 5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' in the TRISB register puts the corresponding output driver in a Hi-impedance mode. A '0' in the TRISB register puts the contents of the output latch on the selected pin(s).

Reading PORTB register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

Each of the PORTB pins has a weak internal pull-up ( $\approx 200 \ \mu A$  typical). A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RBIF interrupt (flag latched in INTCON<0>). This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB (this will end the mismatch condition)
- Clear flag bit RBIF

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on mismatch feature, together with software configurable pull-ups on these four pins, allows easy interface to a key pad and make it possible for wake-up on key-depression. (See AN552 in the Microchip *Embedded Control Handbook*.)

**Note 1:** If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.



### FIGURE 5-3: BLOCK DIAGRAM OF RB7:RB4 PINS

# 6.3 RESET

The PIC16C55X differentiates between various kinds of RESET:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during SLEEP
- WDT Reset (normal operation)
- WDT wake-up (SLEEP)

Some registers are not affected in any RESET condition; their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset, on MCLR or WDT Reset and on MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 6-4. These bits are used in software to determine the nature of the RESET. See Table 6-6 for a full description of RESET states of all registers. A simplified block diagram of the on-chip RESET circuit is shown in Figure 6-6.

The  $\overline{\text{MCLR}}$  Reset path has a noise filter to detect and ignore small pulses. See Table 10-3 for pulse width specification.









Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other RESETS
2007h	Config. bits		Reserved	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0		
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

#### 6.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the  $\overline{TO}$  bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hiimpedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated
	by a WDT timeout does not drive MCLR
	pin low.

#### 6.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- External RESET input on MCLR pin 1
- Watchdog Timer Wake-up (if WDT was enabled) 2.
- Interrupt from RB0/INT pin or RB Port change 3.

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up is cleared when SLEEP is invoked. TO bit is cleared if WDT Wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes-up from SLEEP, regardless of the source of wake-up.

#### Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q1 Q2 Q3 Q4 OSC1 MMM Tost<sup>(2)</sup> CLKOUT(4) INT pin INTF flag (INTCON<1>) Interrupt Latency<sup>(2)</sup> GIE bit (INTCON<7>) Processor in SLEEP **INSTRUCTION FLOW** PC PC+2 PC + 2PC+' PC+2 0004h 0005 Instruction fetched Inst(PC + 1) Inst(PC + 2) Inst(0004h) Inst(0005h) Inst(PC) = SLEEPInstruction executed Inst(PC - 1) SLEEP Inst(PC + 1) Dummy cycle Dummy cycle Inst(0004h) Note

#### **FIGURE 6-14:** WAKE-UP FROM SLEEP THROUGH INTERRUPT

1: XT, HS or LP Oscillator mode assumed.

TOST = 1024Tosc (drawing not to scale). This delay will not be there for RC osc mode. 2:

GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line. 3:

CLKOUT is not available in these osc modes, but shown here for timing reference. 4:

NOTES:

# 8.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[ <i>label</i> ] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Encoding:	11 111x kkkk kkkk
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.
Words:	1
Cycles:	1
Example	ADDLW 0x15
	Before Instruction
	W = 0x10
	After Instruction
	W = 0x25

ADDWF	Add W and f
Syntax:	[label] ADDWF f,d
Operands:	$0 \le f \le 127$
	$d \in [0,1]$
Operation:	$(W) + (f) \to (dest)$
Status Affected:	C, DC, Z
Encoding:	00 0111 dfff ffff
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example	ADDWF FSR, 0
	Before Instruction
	W = 0x17
	FSR = 0xC2
	After Instruction
	W = 0xD9
	FSR = 0xC2

ANDLW	AND Li	teral wit	h W	
Syntax:	[ <i>label</i> ] ANDLW k			
Operands:	$0 \le k \le 2$	255		
Operation:	(W) .AN	ID. (k) →	→ (W)	
Status Affected:	Z			
Encoding:	11	1001	kkkk	kkkk
Description:	The conter AND'ed wi result is pla	nts of W r th the eig aced in th	egister are ht bit literal e W regist	'k'. The er.
Words:	1			
Cycles:	1			
Example	ANDLW	0x5F		
	Before I	nstructio	on	
	W	=	0xA3	
	After Ins	struction		
	W	=	0x03	

ANDWF	AND W with f	
Syntax:	[label] ANDWF f,d	
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$	
Operation:	(W) .AND. (f) $\rightarrow$ (dest)	
Status Affected:	Z	
Encoding:	00 0101 dfff ffff	
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.	
Words:	1	
Cycles:	1	
Example	ANDWF FSR, 1	
	Before Instruction	
	W = 0x17	
	FSR = 0xC2	
	After Instruction	
	W = 0x17	
	FSR = 0x02	

-

DECFSZ	Decrement f, Skip if 0						
Syntax:	[label] DECFSZ f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$						
Operation:	(f) - 1 $\rightarrow$ (dest); skip if result = 0						
Status Affected:	None						
Encoding:	00 1011 dfff ffff						
Description:	The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.						
Words:	1						
Cycles:	1(2)						
Example	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • •						
	Before Instruction						
	PC = address HERE						
	After Instruction						
	CNT = CNT - 1						
	if $CNT = 0$ ,						
	PC = address CONTINUE						
	if CNT $\neq$ 0,						
	PC = address HERE+1						

GOTO	Unconditional Branch					
Syntax:	[ <i>label</i> ] GOTO k					
Operands:	$0 \le k \le 2047$					
Operation:	$k \rightarrow PC<10:0>$ PCLATH<4:3> $\rightarrow$ PC<12:11>					
Status Affected:	None					
Encoding:	10 1kkk kkkk kkkk					
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.					
Words:	1					
Cycles:	2					
Example	GOTO THERE					
INCF	PC = Address THERE					
Svntax:	[ <i>label</i> ] INCF f.d					
Operands:	$0 \le f \le 127$ $d \in [0,1]$					
Operation:	(f) + 1 $\rightarrow$ (dest)					
Status Affected:	Z					
Encoding:	00 1010 dfff ffff					
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.					
Words:	1					
Cycles:	1					
Example	INCF CNT, 1					

INCF CNT, 1 Before Instruction CNT = 0xFFZ = 0After Instruction CNT = 0x00Z = 1

RRF	Rotate Right f through Carry								
Syntax:	[label]	RRF 1	,d						
Operands:	$0 \le f \le 127$ $d \in [0,1]$	,							
Operation:	See description below								
Status Affected:	С								
Encoding:	00 1100 dfff ffff								
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.								
	C	<b>→</b>	Regist	er f	]->				
Words:	1								
Cycles:	1								
Example	RRF		REG	1,0					
	Before Ins	tructio	า						
	REG1	= 1	L110	011	.0				
	С	= (	)						
	After Instru	After Instruction							
	REG1	= 1	L110	011	.0				
	W	= (	0111	001	.1				
	С	= (	)						

### SLEEP

Syntax:	[ <i>label</i> ]	SLEEP						
Operands:	None							
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$							
Status Affected:	TO, PD							
Encoding:	00	0000	0110	0011				
Description:	The power-down status bit, <u>PD</u> is cleared. Timeout status bit, <u>TO</u> is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 6.8 for more details.							
Words:	1							
Cycles:	1							
Example:	SLEEP							

SUBLW	Subtract W from Literal									
Syntax:	[ label ]	SUBLW	/ k							
Operands:	$0 \le k \le 255$									
Operation:	$k - (W) \to (W)$									
Status Affected:	C, DC, Z									
Encoding:	11	110x	kkkk kkkk							
Description:	The W reg plement m 'k'. The res	The W register is subtracted (2's com- plement method) from the eight bit literal 'k'. The result is placed in the W register.								
Words:	1									
Cycles:	1									
Example 1:	SUBLW	0x02								
	Before In	structio	n							
	W	=	1							
	С	=	?							
	After Inst	ruction								
	W	=	1							
	С	=	1; result is positive							
Example 2:	Before In	structio	n							
	W	=	2							
	С	=	?							
	After Inst	ruction								
	W	=	0							
	С	=	1; result is zero							
Example 3:	Before In	structio	n							
	W	=	3							
	С	=	?							
	After Inst	ruction								
	W	=	0xFF							
	С	=	u; result is nega-							

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# 9.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

# 9.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

# 9.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters. NOTES:

# 10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †	
Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and $\overline{\text{MCLR}}$ )	0.6V to VDD +0.6V
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into VDD pin	250 mA
Input Clamp Current, Iik (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (V0 < 0 or V0 > VDD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA, PORTB and PORTC	200 mA
Maximum Current sourced by PORTA, PORTB and PORTC	200 mA
<b>Note 1:</b> Power dissipation is calculated as follows: PDIS = VDD x {IDD - $\sum$ IOH} + $\sum$	$\Sigma \{(VDD-VOH) \times IOH\} + \Sigma(VOI \times IOL)\}$

**† NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

NOTES:

### 18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18		
Pitch	р		.050			1.27		
Overall Height	А	.093	.099	.104	2.36	2.50	2.64	
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39	
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30	
Overall Width	E	.394	.407	.420	10.01	10.34	10.67	
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59	
Overall Length	D	.446	.454	.462	11.33	11.53	11.73	
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74	
Foot Length	L	.016	.033	.050	0.41	0.84	1.27	
Foot Angle	ф	0	4	8	0	4	8	
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30	
Lead Width	В	.014	.017	.020	0.36	0.42	0.51	
Mold Draft Angle Top	α	0	12	15	0	12	15	
Mold Draft Angle Bottom	β	0	12	15	0	12	15	

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013

Drawing No. C04-051

### 28-Lead Ceramic Dual In-line with Window (JW) - 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Tip to Seating Plane	L	.135	.140	.145	3.43	3.56	3.68
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.290	.300	.310	7.37	7.62	7.87

Significant Characteristic JEDEC Equivalent: MO-058 Drawing No. C04-080

### 20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	А	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	ф	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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### 28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units	INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	Е	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

**Controlling Parameter** § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-150

Drawing No. C04-073

A2