



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c558-20i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## PIC16C55X

## FIGURE 3-1: BLOCK DIAGRAM



## FIGURE 4-3:

## DATA MEMORY MAP FOR THE PIC16C554

File Address	3		File Address			
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h			
01h	TMR0	OPTION	81h			
02h	PCL	PCL	82h			
03h	STATUS	STATUS	83h			
04h	FSR	FSR	84h			
05h	PORTA	TRISA	85h			
06h	PORTB	TRISB	86h			
07h			87h			
08h			88h			
09h			89h			
0Ah	PCLAIH	PCLAIH	8Ah			
0Bh	INTCON	INICON	8Bh			
0Ch			8Ch			
		DCON				
0En		PCON	8En			
10h						
1011 11h			9011			
12h			92h			
13h			- 93h			
14h			94h			
15h			95h			
16h			96h			
17h			97h			
18h			98h			
19h			99h			
1Ah			9Ah			
1Bh			9Bh			
1Ch			9Ch			
1Dh			9Dh			
1Eh			9Eh			
1Fh			9Fh			
20h	General Purpose		A0h			
6Fh	Register					
70h						
ı I			$\neg$			
7Fh			FFh			
7111	Bank 0	Bank 1				
Unimplemented data memory locations, read as '0'. <b>Note 1:</b> Not a physical register.						

#### FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C557

File Address	5		File Address			
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h			
01h	TMR0	OPTION	81h			
02h	PCL	PCL	82h			
03h	STATUS	STATUS	83h			
04h	FSR	FSR	84h			
05h	PORTA	TRISA	85h			
06h	PORTB	TRISB	86h			
07h	PORTC	TRISC	87h			
08h			88h			
09h			89h			
0Ah	PCLATH	PCLATH	8Ah			
0Bh	INTCON	INTCON	8Bh			
0Ch			8Ch			
0Dh			8Dh			
0Eh		PCON	8Eh			
0Fh			8Fh			
10h			90h			
11h			91h			
12h			92h			
13h			93h			
14h						
15h			95h			
16h			96h			
17h			97h			
18h			98h			
19h			99h			
1Ah			9Ah			
1Bh			9Bh			
1Ch			9Ch			
1Dh			9Dh			
1Eh			9Eh			
1Fh			9Fh			
20h			A0h			
-	General	General	7.011			
	Purpose Register	Purpose				
	register		BFh			
			C0h			
ſ						
7Eh			FFh			
1 ETT 4	Bank 0					
Unimp	lemented data mer	mory locations	ad as '0'			
<b>Note 1:</b> Not a physical register.						

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on	Detail on
Address	Hume	Bitt	Bitto	Bitto	Dit 4	DRO	DRZ	DRT	BRU	POR Reset	Page:
Bank 0										÷	
00h	INDF	Address physical	ing this loca register)	ation uses	contents	of FSR to	address d	lata memo	ory (not a	XXXX XXXX	21
01h	TMR0	Timer0 N	/lodule's Re	egister						XXXX XXXX	47
02h	PCL	Program	Counter's	(PC) Leas	st Significa	ant Byte				0000 0000	21
03h	STATUS	IRP <sup>(2)</sup>	RP1 <sup>(2)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	17
04h	FSR	Indirect of	data memo	ry address	s pointer					XXXX XXXX	21
05h	PORTA	_		_	RA4	RA3	RA2	RA1	RA0	x xxxx	23
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	25
07h	PORTC <sup>(4)</sup>	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	27
08h	—	Unimple	mented							—	_
09h	—	Unimple	mented							—	_
0Ah	PCLATH	_		_	Write bu	ffer for up	per 5 bits	of prograr	n counter	0 0000	21
0Bh	INTCON	GIE	(3)	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
0Ch	—	Unimple	mented							—	_
0Dh-1Eh	—	Unimple	mented							—	_
1Fh	_	Unimple	mented							—	-
Bank 1											
80h	INDF	Address physical	ing this loca register)	ation uses	contents	of FSR to	address d	lata memo	ory (not a	XXXX XXXX	21
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	18
82h	PCL	Program	Counter's	(PC) Leas	st Significa	ant Byte				0000 0000	21
83h	STATUS			RP0	TO	PD	Z	DC	С	0001 1xxx	17
84h	FSR			Indirect d	lata memo	ory addres	s pointer			XXXX XXXX	21
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	23
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	25
87h	TRISC <sup>(4)</sup>	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	27
88h	—	Unimplemented								—	_
89h	—	Unimple	mented							—	_
8Ah	PCLATH	—			Write bu	ffer for upp	per 5 bits	of prograr	n counter	0 0000	21
8Bh	INTCON	GIE	(3)	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	19
8Ch	—	Unimplemented							—	_	
8Dh	_	Unimplemented							—	_	
8Eh	PCON	—	—	_	_	_	—	POR		0-	20
8Fh-9Eh	—	Unimple	mented							—	
9Fh	— Unimplemented						_	_			

## TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C55X

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: IRP & RP1 bits are reserved, always maintain these bits clear.

3: Bit 6 of INTCON register is reserved for future use. Always maintain this bit as clear.

4: PIC16C557 only.

#### 4.2.2.4 PCON Register

The PCON register contains a flag bit to differentiate between a Power-on Reset, an external MCLR Reset or WDT Reset. See Section 6.3 and Section 6.4 for detailed RESET operation.

#### **REGISTER 4-4:** PCON REGISTER (ADDRESS 8Eh) U-0 U-0 U-0 R/W-0 U-0 U-0 U-0 U-0 POR bit7 bit 7-2 Unimplemented: Read as '0' bit 1 POR: Power-on Reset status bit 1 = No Power-on Reset occurred 0 = Power-on Reset occurred bit 0 Unimplemented: Read as '0' Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit0

## 5.4 I/O Programming Considerations

#### 5.4.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-1 shows the effect of two sequential read-modify-write instructions (ex.,  ${\tt BCF}$ ,  ${\tt BSF}$ , etc.) on an I/O port.

A pin actively outputting a low or high should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

### 6.4.5 POWER CONTROL/STATUS REGISTER (PCON)

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET if POR is '0', it will indicate that a Poweron Reset must have occurred (VDD may have gone too low).

## TABLE 6-3: TIMEOUT IN VARIOUS SITUATIONS

Oscillator	Pow	Power-up					
Configuration	PWRTE = 0	PWRTE = 1	SLEEP				
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	1024 Tosc				
RC	72 ms	—	—				

## TABLE 6-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	то	PD	
0	1	1	Power-on Reset
0	0	Х	Illegal, TO is set on POR
0	Х	0	Illegal, PD is set on POR
1	0	u	WDT Reset
1	0	0	WDT Wake-up
1	u	u	MCLR Reset during normal operation
1	1	0	MCLR Reset during SLEEP

# PIC16C55X



### FIGURE 6-10: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

## 6.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This will have to be implemented in software.

Example 6-1 stores and restores the STATUS and W registers. The user register, W\_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W\_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS\_TEMP, must be defined in Bank 0. The Example 6-1:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

#### EXAMPLE 6-1: SAVING THE STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;copy W to TEMP ;register, could be in
		;either bank
SWAPF	STATUS,W	;swap STATUS to be
		;saved into W
BCF	STATUS, RPO	;change to bank0
		;regardless of
		;current bank
MOVWF	STATUS_TEMP	;save STATUS to bank0
		;register
:		
:		
:		
SWAPF	STATUS_TEMP, W	i;swap STATUS_TEMP
		;register into W, sets
		;bank to original state
MOVWF	STATUS	;move W into STATUS
		;register
SWAPF	W_TEMP,F	;swap W_TEMP
SWAPF	W_TEMP,W	;swap W_TEMP into W

## 6.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT timeout generates a device RESET. If the device is in SLEEP mode, a WDT timeout causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 6.1).

## 6.7.1 WDT PERIOD

The WDT has a nominal timeout period of 18 ms, (with no prescaler). The timeout periods vary with temperature, VDD and process variations from part-to-part (see DC specs). If longer timeout periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, timeout periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The  $\overline{\text{TO}}$  bit in the STATUS register will be cleared upon a Watchdog Timer timeout.

## 6.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

## 7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



## 7.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet.

Note: There is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa. The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

© 1996-2013 Microchip Technology Inc.

NOTES:

## TABLE 8-2: PIC16C55X INSTRUCTION SET

Mnemonic, Operands		Description		14-Bit Opcode				Status	Notes
		Description	Cycles	MSb			LSb	Affected	Notes
		BYTE-ORIENTED FILE REGIS	STER OF	PERAT	IONS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST	ER OPER	RATION	IS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

## 9.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 9.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

## 9.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily re configured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft<sup>®</sup> Windows environment were chosen to best make these features available to you, the end user.

## 9.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

# PIC16C55X





**2**: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.







**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

## 10.3 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

#### 1. TppS2ppS

2. TppS

Т			
F	Frequency	Т	Time
Lowercas	e subscripts (pp) and their meanings:		
рр			
ck	CLKOUT	OS	OSC1
io	I/O port	t0	ТОСКІ
mc	MCLR		
Uppercas	e letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

## FIGURE 10-5: LOAD CONDITIONS



Watchdog Timer RESET

I/O Pins



#### **FIGURE 10-8:** RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP

#### **TABLE 10-3**: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

34 —

31

34

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
30	TmcL	MCLR Pulse Width (low)	2000		—	ns	-40° to +85°C			
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C			
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc	—	—	Tosc = OSC1 period			
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	$VDD = 5.0V, -40^{\circ} \text{ to } +85^{\circ}C$			
34	Tioz	I/O hi-impedance from MCLR low			2.0*	μs				
*	Those pr	remotors are observatorized but not	* These normative are characterized but not forded							

These parameters are characterized but not tested.

Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

NOTES:

### 18-Lead Ceramic Dual In-line with Window (JW) - 300 mil (CERDIP)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

Significant Characteristic JEDEC Equivalent: MO-036 Drawing No. C04-010

NOTES:

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- General Technical Support Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- Business of Microchip Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

## **READER RESPONSE**

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: RE:	Technical Publications Manager Reader Response	Total Pages Sent
From	). Name	
1 1011	Company	
	Address	
	City / State / ZIP / Country	
	Telephone: ()	FAX: ()
Appl	ication (optional):	
Wou	ld you like a reply?YN	
Devi	ce:	Literature Number: DS40143E
Ques	stions:	
1. \	What are the best features of this document?	
-		
- 2. H	How does this document meet your hardware and softwar	re development needs?
_		
_		
3. E	Do you find the organization of this document easy to follo	ow? If not, why?
-		
-		
4. \	What additions to the document do you think would enhar	nce the structure and subject?
-		
5 \	What deletions from the document could be made without	affecting the overall usefulness?
0. 1		
-		
6. I	s there any incorrect or misleading information (what and	where)?
_		
-		
7. H	How would you improve this document?	
-		
-		