



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc558-04-ss

Table of Contents

1.0	General Description.....	5
2.0	PIC16C55X Device Varieties	7
3.0	Architectural Overview	9
4.0	Memory Organization	13
5.0	I/O Ports	23
6.0	Special Features of the CPU	31
7.0	Timer0 Module	47
8.0	Instruction Set Summary	53
9.0	Development Support.....	67
10.0	Electrical Specifications.....	73
11.0	Packaging Information.....	87
Appendix A:	Enhancements.....	97
Appendix B:	Compatibility	97
Index		99
On-Line Support.....		101
Systems Information and Upgrade Hot Line		101
Reader Response		102
Product Identification System		103

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@mail.microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (480) 792-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com/cn to receive the most current information on all of our products.

PIC16C55X

TABLE 1-1: PIC16C55X FAMILY OF DEVICES

		PIC16C554	PIC16C557	PIC16C558
Clock	Maximum Frequency of Operation (MHz)	20	20	20
Memory	EPROM Program Memory (x14 words)	512	2K	2K
	Data Memory (bytes)	80	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
Features	Interrupt Sources	3	3	3
	I/O Pins	13	22	13
	Voltage Range (Volts)	2.5-5.5	2.5-5.5	2.5-5.5
	Brown-out Reset	—	—	—
	Packages	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC, SSOP
All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C55X Family devices use serial programming with clock pin RB6 and data pin RB7.				

PIC16C55X

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C55X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C55X uses a Harvard architecture in which program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently from 8-bit wide data words. Instruction opcodes are 14-bit wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single-cycle (200 ns @ 20 MHz) except for program branches. The table below lists the memory (EPROM and RAM).

Device	Program Memory (EPROM)	Data Memor (RAM)
PIC16C554	512	80
PIC16C557	2 K	128
PIC16C558	2 K	128

The PIC16C554 addresses 512 x 14 on-chip program memory. The PIC16C557 and PIC16C558 addresses 2 K x 14 program memory. All program memory is internal.

The PIC16C55X can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped into the data memory. The PIC16C55X has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any Addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C55X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C55X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

PIC16C55X

FIGURE 3-1: BLOCK DIAGRAM

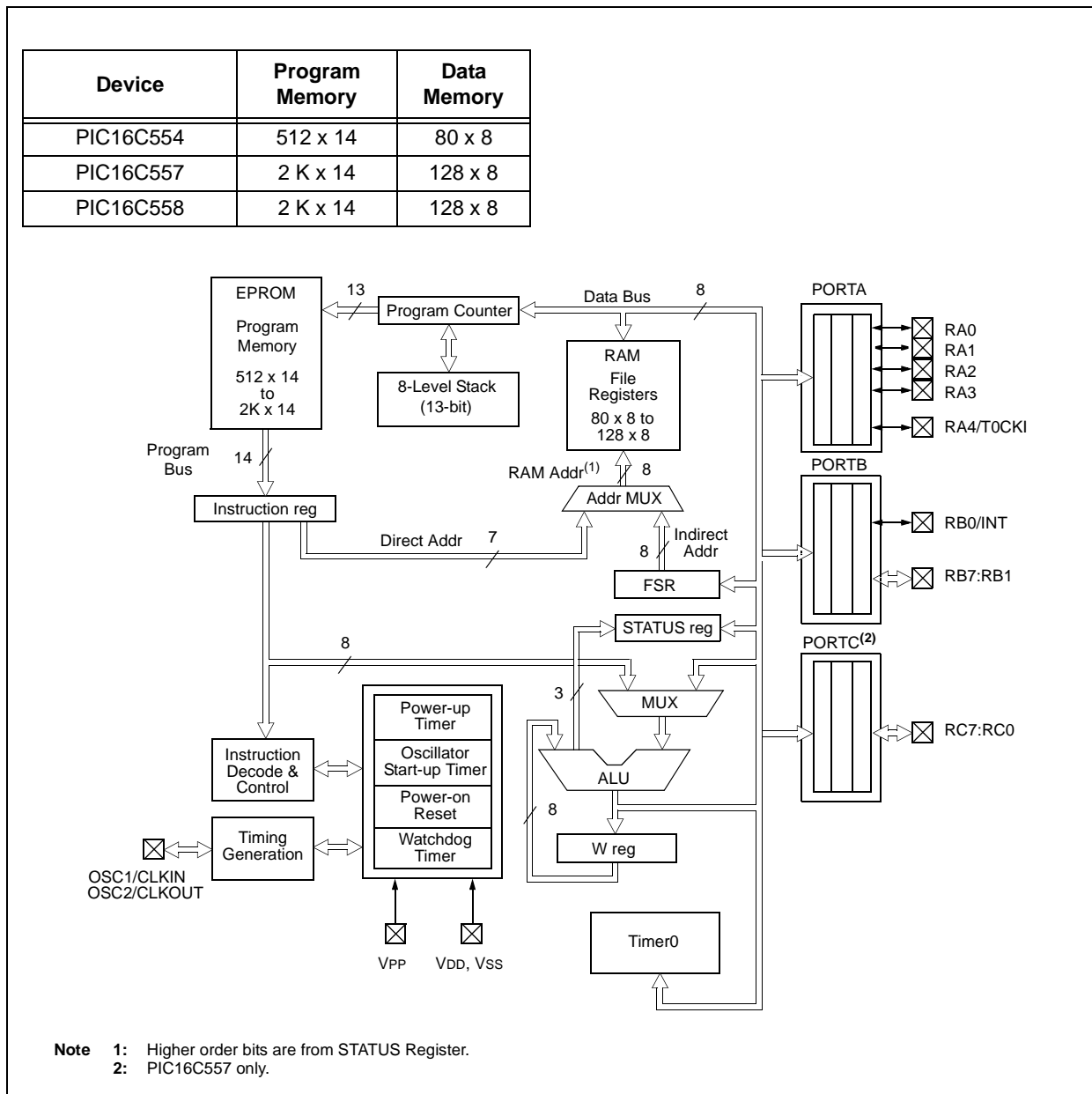


FIGURE 4-5: DATA MEMORY MAP FOR THE PIC16C558

File Address			File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch			8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh			9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
7Fh	Bank 0	Bank 1	FFh
<div><div></div> Unimplemented data memory locations, read as '0'.</div> <div>Note 1: Not a physical register.</div>			

4.2.2 SPECIAL FUNCTION REGISTERS

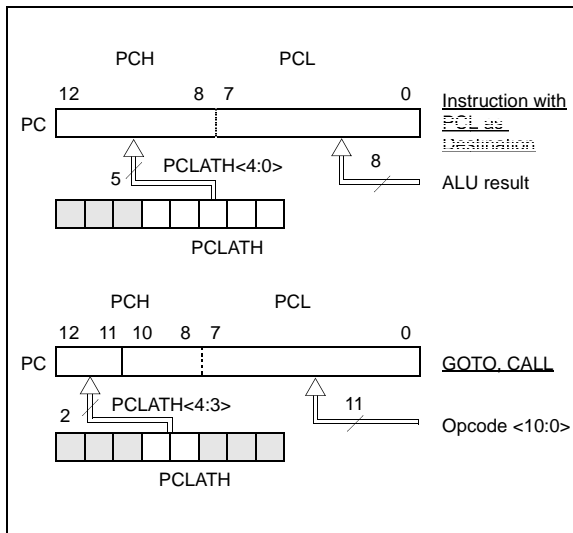
The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The Special Function Registers can be classified into two sets (core and peripheral). The special function registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high bits (PC<12:8>) are not directly readable or writable and come from PCLATH. On any RESET, the PC is cleared. Figure 4-6 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 4-6 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-6: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Implementing a Table Read" (AN556).

4.3.2 STACK

The PIC16C55X family has an 8-level deep x 13-bit wide hardware stack (Figure 4-1 and Figure 4-2). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or vectoring to an interrupt address.

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-7. However, IRP is not used in the PIC16C55X.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```

                                movlw    0x20    ;initialize pointer
                                movwf    FSR      ;to RAM
NEXT    clrf    INDF      ;clear INDF register
                                incf     FSR      ;inc pointer
                                btfss    FSR,4    ;all done?
                                goto     NEXT     ;no clear next
                                                ;yes continue

```

CONTINUE:

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The `BCF` and `BSF` instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a `BSF` operation on bit5 of `PORTB` will cause all eight bits of `PORTB` to be read into the CPU. Then the `BSF` operation takes place on bit5 and `PORTB` is written to the output latches. If another bit of `PORTB` is used as a bi-directional I/O pin (e.g., bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. `BCF`, `BSF`, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-1 shows the effect of two sequential read-modify-write instructions (ex., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a low or high should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

6.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)

6.4.1 POWER-ON RESET (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.6V – 1.8V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607 “Power-up Trouble Shooting”.

6.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) timeout on power-up only, from POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, $\overline{\text{PWRTE}}$ can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-Up Time delay will vary from chip to chip and due to VDD, temperature and process variation. See DC parameters for details.

6.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST timeout is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

6.4.4 TIMEOUT SEQUENCE

On power-up, the timeout sequence is as follows: First PWRT timeout is invoked after POR has expired, then OST is activated. The total timeout will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in RC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no timeout at all. Figure 6-7, Figure 6-8 and Figure 6-9 depict timeout sequences.

Since the timeouts occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the timeouts will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 6-8). This is useful for testing purposes or to synchronize more than one PIC16C55X device operating in parallel.

Table 6-5 shows the RESET conditions for some special registers, while Table 6-6 shows the RESET conditions for all the registers.

PIC16C55X

TABLE 6-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0-
MCLR Reset during normal operation	000h	000u uuuu	---- --u-
MCLR Reset during SLEEP	000h	0001 0uuu	---- --u-
WDT Reset	000h	0000 uuuu	---- --u-
WDT Wake-up	PC + 1	uuu0 0uuu	---- --u-
Interrupt Wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 6-6: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	MCLR Reset during normal operation MCLR Reset during SLEEP WDT Reset	Wake-up from SLEEP through interrupt Wake-up from SLEEP through WDT timeout
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC ⁽⁴⁾	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC ⁽⁴⁾	86h	1111 1111	1111 1111	uuuu uuuu
PCON	8Eh	---- --0-	---- --u-	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 6-5 for RESET value for specific condition.

4: PIC16C557 only.

8.1 Instruction Descriptions

ADDLW Add Literal and W

Syntax:	[<i>label</i>] ADDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$(W) + k \rightarrow (W)$				
Status Affected:	C, DC, Z				
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>	11	111x	kkkk	kkkk
11	111x	kkkk	kkkk		
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	ADDLW 0x15 Before Instruction W = 0x10 After Instruction W = 0x25				

ANDLW AND Literal with W

Syntax:	[<i>label</i>] ANDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	(W) .AND. (k) \rightarrow (W)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>	11	1001	kkkk	kkkk
11	1001	kkkk	kkkk		
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	ANDLW 0x5F Before Instruction W = 0xA3 After Instruction W = 0x03				

ADDWF Add W and f

Syntax:	[<i>label</i>] ADDWF <i>f</i> , <i>d</i>												
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$												
Operation:	$(W) + (f) \rightarrow (dest)$												
Status Affected:	C, DC, Z												
Encoding:	<table border="1"><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>	00	0111	dfff	ffff								
00	0111	dfff	ffff										
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.												
Words:	1												
Cycles:	1												
Example	<pre>ADDWF FSR, 0</pre> <p>Before Instruction</p> <table><tr><td>W</td><td>=</td><td>0x17</td></tr><tr><td>FSR</td><td>=</td><td>0xC2</td></tr></table> <p>After Instruction</p> <table><tr><td>W</td><td>=</td><td>0xD9</td></tr><tr><td>FSR</td><td>=</td><td>0xC2</td></tr></table>	W	=	0x17	FSR	=	0xC2	W	=	0xD9	FSR	=	0xC2
W	=	0x17											
FSR	=	0xC2											
W	=	0xD9											
FSR	=	0xC2											

ANDWF AND W with f

Syntax:	[<i>label</i>] ANDWF <i>f</i> , <i>d</i>				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(W) .AND. (f) \rightarrow (dest)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>	00	0101	dfff	ffff
00	0101	dfff	ffff		
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	ANDWF FSR, 1 Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0x17 FSR = 0x02				

PIC16C55X

CLR W	Clear W				
Syntax:	[<i>label</i>] CLRW				
Operands:	None				
Operation:	00h → (W) 1 → Z				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>0001</td><td>0000</td><td>0011</td></tr></table>	00	0001	0000	0011
00	0001	0000	0011		
Description:	W register is cleared. Zero bit (Z) is set.				
Words:	1				
Cycles:	1				
Example	CLRW Before Instruction W = 0x5A After Instruction W = 0x00 Z = 1				

COMF	Complement f				
Syntax:	[<i>label</i>] COMF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(\bar{f}) \rightarrow (\text{dest})$				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>1001</td><td>dfff</td><td>ffff</td></tr></table>	00	1001	dfff	ffff
00	1001	dfff	ffff		
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	COMF REG1,0 Before Instruction REG1 = 0x13 After Instruction REG1 = 0x13 W = 0xEC				

CLRWD T	Clear Watchdog Timer				
Syntax:	[<i>label</i>] CLRWD T				
Operands:	None				
Operation:	00h → WDT 0 → WDT prescaler, 1 → \overline{TO} 1 → \overline{PD}				
Status Affected:	\overline{TO} , \overline{PD}				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0100</td></tr></table>	00	0000	0110	0100
00	0000	0110	0100		
Description:	CLRWD T instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.				
Words:	1				
Cycles:	1				
Example	<div>CLRWD T</div> <div>Before Instruction</div> <div>WDT counter = ?</div> <div>After Instruction</div> <div>WDT counter = 0x00</div> <div>WDT prescaler = 0</div> <div>\overline{TO} = 1</div> <div>\overline{PD} = 1</div>				

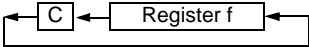
DECF	Decrement f				
Syntax:	[<i>label</i>] DECF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(f) - 1 \rightarrow (\text{dest})$				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>0011</td><td>dfff</td><td>ffff</td></tr></table>	00	0011	dfff	ffff
00	0011	dfff	ffff		
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	DECF CNT, 1 Before Instruction CNT = 0x01 Z = 0 After Instruction CNT = 0x00 Z = 1				

PIC16C55X

RETFIE		Return from Interrupt							
Syntax:	[<i>label</i>] RETFIE								
Operands:	None								
Operation:	TOS → PC, 1 → GIE								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>00</td><td>0000</td><td>0000</td><td>1001</td></tr></table>				00	0000	0000	1001	
00	0000	0000	1001						
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.								
Words:	1								
Cycles:	2								
Example	RETFIE								
	After Interrupt								
	PC = TOS								
	GIE = 1								

RETURN	Return from Subroutine				
Syntax:	[<i>label</i>] RETURN				
Operands:	None				
Operation:	TOS → PC				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0000</td><td>1000</td></tr></table>	00	0000	0000	1000
00	0000	0000	1000		
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.				
Words:	1				
Cycles:	2				
Example	RETURN After Interrupt PC = TOS				

RETLW		Return with Literal in W							
Syntax:	[<i>label</i>] RETLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	$k \rightarrow (W)$; TOS \rightarrow PC								
Status Affected:	None								
Encoding:	<table><tr><td>11</td><td>01xx</td><td>kkkk</td><td>kkkk</td></tr></table>					11	01xx	kkkk	kkkk
11	01xx	kkkk	kkkk						
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.								
Words:	1								
Cycles:	2								
Example	<pre>CALL TABLE;W contains table ;offset value ;W now has table value . . . ADDWF PC ;W = offset TABLE RETLW k1 ;Begin table RETLW k2 ; . . RETLW kn ; End of table</pre> <p>Before Instruction</p> <p>W = 0x07</p> <p>After Instruction</p> <p>W = value of k8</p>								

RLF	Rotate Left f through Carry				
Syntax:	[<i>label</i>] RLF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	See description below				
Status Affected:	C				
Encoding:	<table><tr><td>00</td><td>1101</td><td>dfff</td><td>ffff</td></tr></table>	00	1101	dfff	ffff
00	1101	dfff	ffff		
Description:	<p>The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.</p> 				
Words:	1				
Cycles:	1				
Example	<pre>RLF REG1,0</pre> <p>Before Instruction</p> <pre>REG1 = 1110 0110 C = 0</pre> <p>After Instruction</p> <pre>REG1 = 1110 0110 W = 1100 1100 C = 1</pre>				

PIC16C55X

SUBWF	Subtract W from f				
Syntax:	[<i>label</i>] SUBWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(f) - (W) \rightarrow (\text{dest})$				
Status Affected:	C, DC, Z				
Encoding:	<table><tr><td>00</td><td>0010</td><td>dfff</td><td>ffff</td></tr></table>	00	0010	dfff	ffff
00	0010	dfff	ffff		
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example 1:	<div>SUBWF REG1,1</div> <div>Before Instruction</div> <div>REG1 = 3 W = 2 C = ?</div> <div>After Instruction</div> <div>REG1 = 1 W = 2 C = 1; result is positive</div>				
Example 2:	<div>Before Instruction</div> <div>REG1 = 2 W = 2 C = ?</div> <div>After Instruction</div> <div>REG1 = 0 W = 2 C = 1; result is zero</div>				
Example 3:	<div>Before Instruction</div> <div>REG1 = 1 W = 2 C = ?</div> <div>After Instruction</div> <div>REG1 = 0xFF W = 2 C = 0; result is negative</div>				

SWAPF		Swap Nibbles in f						
Syntax:	[<i>label</i>] SWAPF f,d							
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]							
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)							
Status Affected:	None							
Encoding:	<table><tr><td>00</td><td>1110</td><td>dfff</td><td>ffff</td></tr></table>				00	1110	dfff	ffff
00	1110	dfff	ffff					
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.							
Words:	1							
Cycles:	1							
Example	SWAPF REG, 0							
Before Instruction								
REG1 = 0xA5								
After Instruction								
REG1 = 0xA5								
W = 0x5A								

TRIS		Load TRIS Register						
Syntax:	[<i>label</i>] TRIS f							
Operands:	5 ≤ f ≤ 7							
Operation:	(W) → TRIS register f;							
Status Affected:	None							
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0fff</td></tr></table>				00	0000	0110	0fff
00	0000	0110	0fff					
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.							
Words:	1							
Cycles:	1							
Example	<div>To maintain upward compatibility with future PIC MCU products, do not use this instruction.</div>							

9.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

9.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

9.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

9.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

9.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

PIC16C55X

10.3 Timing Parameter Symbolology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time

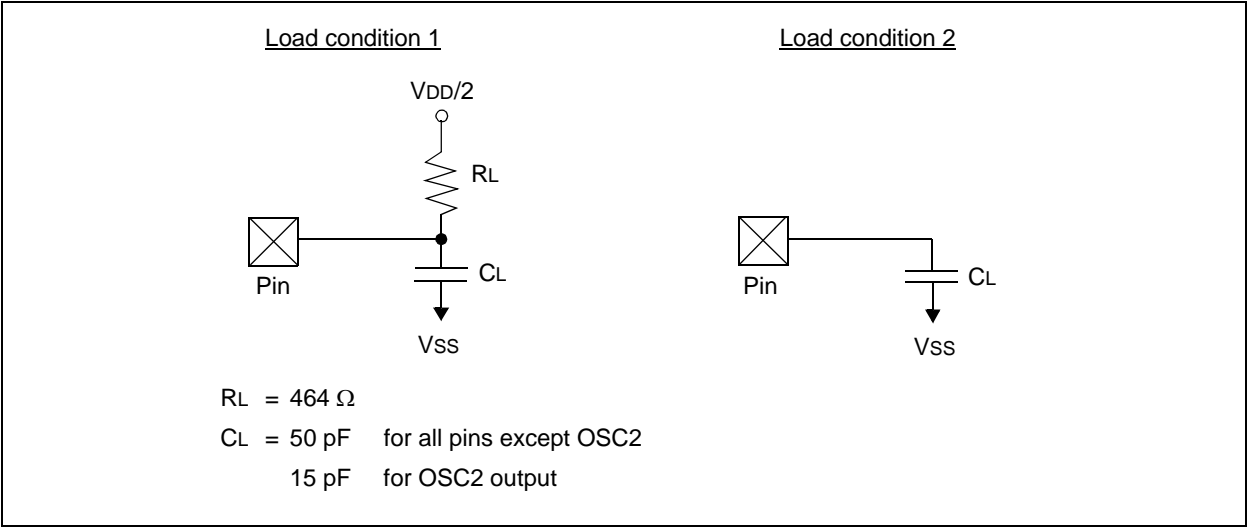
Lowercase subscripts (pp) and their meanings:

pp			
ck	CLKOUT	os	OSC1
io	I/O port	t0	T0CKI
mc	MCLR		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-5: LOAD CONDITIONS



PIC16C55X

FIGURE 10-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

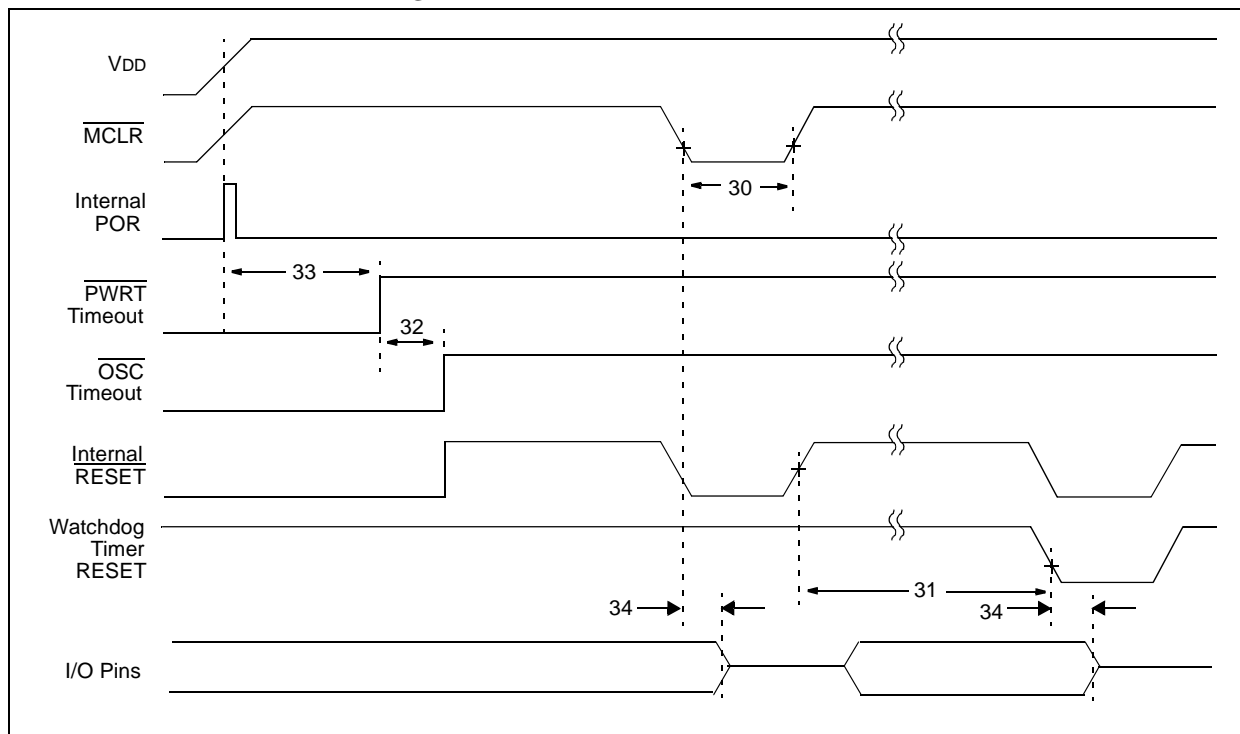


TABLE 10-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

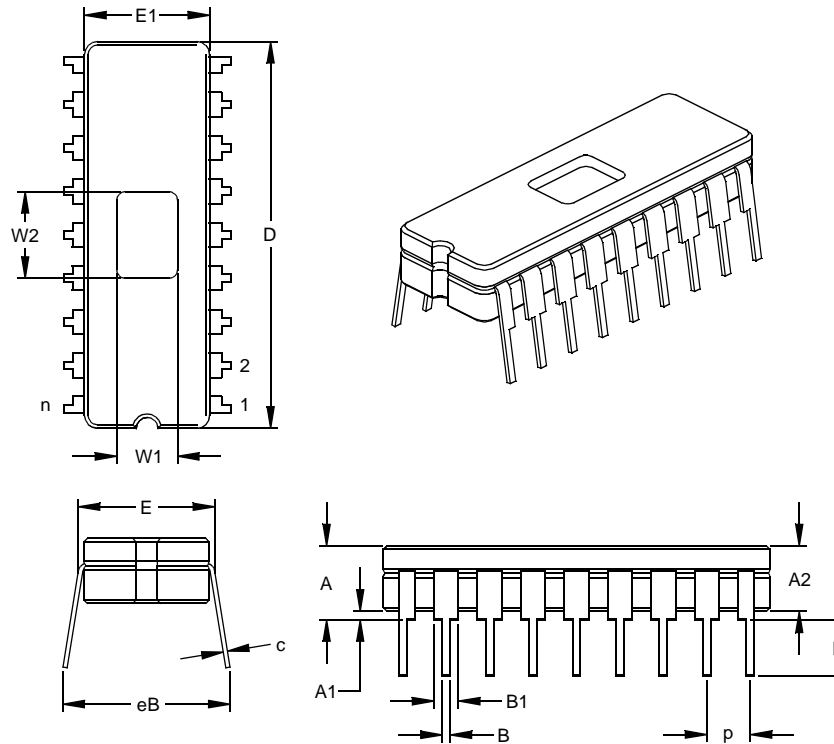
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	Tioz	I/O hi-impedance from MCLR low	—	—	2.0*	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



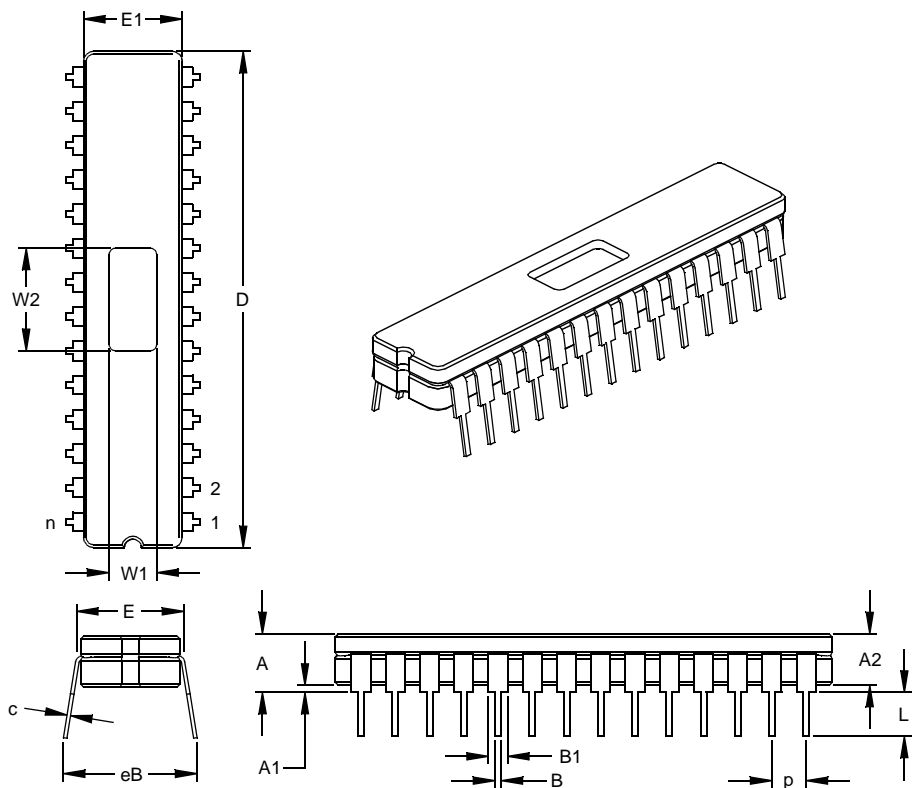
Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	§ eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

* Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-036
 Drawing No. C04-010

PIC16C55X

28-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	INCHES*			MILLIMETERS		
Dimension Limits			MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n			28			28	
Pitch	p			.100			2.54	
Top to Seating Plane	A		.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2		.155	.160	.165	3.94	4.06	4.19
Standoff	A1		.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E		.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1		.285	.290	.295	7.24	7.37	7.49
Overall Length	D		1.430	1.458	1.485	36.32	37.02	37.72
Tip to Seating Plane	L		.135	.140	.145	3.43	3.56	3.68
Lead Thickness	c		.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1		.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	B		.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	§ eB		.345	.385	.425	8.76	9.78	10.80
Window Width	W1		.130	.140	.150	3.30	3.56	3.81
Window Length	W2		.290	.300	.310	7.37	7.62	7.87

* Controlling Parameter

§ Significant Characteristic

JEDEC Equivalent: MO-058

Drawing No. C04-080

NOTES: