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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc558t-04-so

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FIGURE 3-1: BLOCK DIAGRAM



bit 5

4.2.2.2 OPTION Register

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note 1: To achieve a 1:1 prescaler assignment for							
TMR0, assign the prescaler to the WDT							
(PSA = 1).							

REGISTER 4-2:	OPTION REGISTER	(ADDRESS 81H)
---------------	------------------------	---------------

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

- bit 7 **RBPU**: PORTB Pull-up Enable bit
 - 1 = PORTB pull-ups are disabled
 - 0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit

- 1 = Interrupt on rising edge of RB0/INT pin
- 0 = Interrupt on falling edge of RB0/INT pin
- TOCS: TMR0 Clock Source Select bit
 - 1 = Transition on RA4/T0CKI pin
 - 0 = Internal instruction cycle clock (CLKOUT)
- bit 4 TOSE: TMR0 Source Edge Select bit
 - 1 = Increment on high-to-low transition on RA4/T0CKI pin
 - 0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

- 1 = Prescaler is assigned to the WDT
- 0 = Prescaler is assigned to the Timer0 module

bit 2-0 PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1 : 128	1:64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 5-1: PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0	Bit 0	ST	Bi-directional I/O port.
RA1	Bit 1	ST	Bi-directional I/O port.
RA2	Bit 2	ST	Bi-directional I/O port.
RA3	Bit 3	ST	Bi-directional I/O port.
RA4/T0CKI	Bit 4	ST	Bi-directional I/O port or external clock input for TMR0. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
05h	PORTA	—			RA4	RA3	RA2	RA1	RA0	x xxxx	u uuuu
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0', x = unknown, u = unchanged

Note 1: Shaded bits are not used by PORTA.

NOTES:

REGISTER 6-1: CONFIGURATION WORD

	CP1	CP0	CP1	CP0	CP1	CP0	_	Reserved	CP1	CP0	PWRTE	WDTE	F0SC1	F0SC0
	bit 13	0.0		0.0	0. 1	0.0				0.0				bit 0
bit 13-8 bit 5-4	CP<1:0> : Code protection bits ⁽¹⁾ 11 = Program Memory code protection off 10 = 0400h - 07FFh code protected 01 = 0200h - 07FFh code protected 11 = 0000h - 07FFh code protected													
bit 7	Unimpl	Unimplemented: Read as '1'												
bit 6	Reserv	ed: Do no	ot use											
bit 3	PWRTE : Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled													
bit 2	WDTE:	Watchdo	g Timer E	nable bit										
	1 = WD 0 = WD	T enableo T disable	b b											
bit 1-0	FOSC1:FOSC0: Oscillator Selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator													
	Note	1: All o	f the CP1	:CP0 pair	rs have to	be given	the same	e value to ena	ble the o	code pro	tection sche	eme listed.		
	Legend	1:												

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read a	as 'O'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 6-5:INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0-
MCLR Reset during normal operation	000h	000u uuuu	u-
MCLR Reset during SLEEP	000h	0001 Ouuu	u-
WDT Reset	000h	0000 uuuu	u-
WDT Wake-up	PC + 1	uuu0 0uuu	u-
Interrupt Wake-up from SLEEP	PC + 1 ⁽¹⁾	uuul Ouuu	u-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. **Note 1:** When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

Register	Address	Power-on Reset	MCLR Reset during normal operation MCLR Reset during SLEEP WDT Reset	Wake-up from SLEEP through interrupt Wake-up from SLEEP through WDT timeout
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	x xxxx	u uuuu	u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC ⁽⁴⁾	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	0 0000	0 0000	u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	1 1111	1 1111	u uuuu
TRISB	86h	1111 1111	1111 1111	นนนน นนนน
TRISC ⁽⁴⁾	86h	1111 1111	1111 1111	uuuu uuuu
PCON	8Eh	0-	u-	u-

TABLE 6-6: INITIALIZATION CONDITION FOR REGISTERS

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 6-5 for RESET value for specific condition.

4: PIC16C557 only.



FIGURE 6-10: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).









T0IF interrupt flag is sampled here (every Q1). Note 1:

Interrupt latency = 4 Tcr, where Tcr = instruction cycle time. CLKOUT is available only in RC Oscillator mode. 2:

3:

7.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.



7.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 7-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet.

Note: There is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa. The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

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7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to WDT. Lines 5-7 are required only if the desired postscaler rate is 1:1 (PS<2:0> = 000) or 1:2 (PS<2:0> = 001).

EXAMPLE 7-1:	CHANGING PRESCALER
	(TIMER0→WDT)

	•	/
BCF	STATUS, RPO	;Skip if already in
		;Bank 0 CLRWDT Clear WDT
CLRF	TMR0	;Clear TMR0 & Prescaler
BSF	STATUS, RPO	;Bank 1
MOVLW	'00101111 <i>'</i> b	;These 3 lines (5, 6, 7)
MOVWF	OPTION	;Are required only if
		;Desired PS<2:0> are
		;CLRWDT 000 or 001
MOVLW	'00101xxx'b	;Set Postscaler to
MOVWF	OPTION	;Desired WDT rate
BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module use the sequence shown in Example 7-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

	•	
CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		;prescale value and
		;clock source
MOVWF	OPTION	
BCF	STATUS, RPO	

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	TMR0	Timer0 m	odule's registe	r						xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	Reserved	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0',

Note 1: Shaded bits are not used by TMR0 module.

NOTES:

TABLE 8-2: PIC16C55X INSTRUCTION SET

Mnemonic,		Description		14-Bit Opcode				Status	Notes
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
		BYTE-ORIENTED FILE REGIS	STER OF	PERAT	IONS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST	ER OPER	RATION	IS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

BTFSS	Bit Test f, Skip if Set	CALL	Call Subroutine			
Syntax:	[label] BTFSS f,b	Syntax:	[<i>label</i>] CALL k			
Operands:	$0 \le f \le 127$	Operands:	$0 \leq k \leq 2047$			
Operation:	0 ≤ b < 7 skip if (f) = 1	Operation:	$(PC)+1 \rightarrow TOS, k \rightarrow PC<10:0>, (PC)(ATM +4:2*) \rightarrow PC +12:11*$			
Status Affected:	None	Otatua Affaatadu	$(PCLATH<4:3>) \rightarrow PC<12:11>$			
Encoding:	01 11bb bfff ffff	Status Affected:				
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two- cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruc-			
Words:	1	Words:	1			
Cycles:	1(2)	Cycles:	2			
Example	HERE BTFSS FLAG,1 FALSE GOTO PROCESS CODE	Evample	L			
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE		Before Instruction PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1			
	if FLAG<1> = 1,	CLRF	Clear f			
	PC = address TRUE	Syntax:	[label] CLRF f			
		Operands:	$0 \leq f \leq 127$			
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$			
		Status Affected:	Z			
		Encoding:	00 0001 1fff ffff			
		Description:	The contents of register 'f' are cleared and the Z bit is set.			
		Words:	1			
		Cycles:	1			
		Example	CLRF FLAG_REG			
			Before Instruction FLAG_REG=0x5A After Instruction FLAG_REG=0x00 Z =1			

SUBWF	Subtract W from f									
Syntax:	[<i>label</i>] SUBWF f,d									
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$									
Operation:	(f) - (W) \rightarrow (dest)									
Status Affected:	C, DC, Z									
Encoding:	00 0010 dfff ffff									
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.									
Words:	1									
Cycles:	1									
Example 1:	SUBWF REG1,1									
	Before Instruction									
	REG1 = 3									
	W = 2									
	C = ?									
	After Instruction									
	REG1 = 1									
	W = 2									
Example 2	C = 1; result is positive									
Example 2:	Before Instruction									
	REG1 = 2									
	VV = 2 C = 2									
	After Instruction									
	BFG1 = 0									
	W = 2									
	C = 1; result is zero									
Example 3:	Before Instruction									
	REG1 = 1									
	W = 2									
	C = ?									
	After Instruction									
	REG1 = 0xFF									
	W = 2									
	C = 0; result is negative									

SWAPF	Swap Nibbles in f									
Syntax:	[label]	[label] SWAPF f,d								
Operands:	$0 \le f \le 12$	$0 \le f \le 127$								
	d ∈ [0,1]									
Operation:	(f<3:0>) - (f<7:4>) -	\rightarrow (dest< \rightarrow (dest<	7:4>), 3:0>)							
Status Affected:	None									
Encoding:	00	1110	dfff	ffff						
Description:	The upper register 'f' the result i is 1 the res	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.								
Words:	1	1								
Cycles:	1									
Example	SWAPF	REG,	0							
	Before In	struction								
	RE	G1 =	0xA5							
	After Inst	ruction								
	RE	G1 =	0xA5							
	W	=	0x5A							
TRIS	Load TF	RIS Regi	ster							
Syntax:	[label]	TRIS	f							
Operands:	$5 \leq f \leq 7$									
Operation:	$(W) \rightarrow TF$	RIS regis	ter f;							
Status Affected:	None									
Encoding:	00	0000	0110	Offf						
Description:	The instru- compatibil products. readable a directly ad	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.								
Words:	1									
Cycles:	1									
Example										
	To maintain upward compatibility									

To maintain upward compatibility with future PIC MCU products, do not use this instruction. NOTES:





2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.







2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

10.2 DC Characteristics: PIC16C55X (Commercial, Industrial, Extended) PIC16LC55X(Commercial, Industrial, Extended)

			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial and								
DC Cha	racteris	stics	1 0	•	$0^{\circ}C \leq 1$	A ≤ +7	70°C for commercial and				
			$-40^{\circ}C \le TA \le +125^{\circ}C$ for automotive								
			Operating volt	perating voltage VOU range as described in DC spec							
Param. No.	Sym	Characteristic	Min	Тур†	Max	Unit	Conditions				
	VIL	Input Low Voltage									
		I/O ports									
D030		with TTL buffer	Vss	—	0.8V 0.15 Vdd	V	VDD = 4.5V to 5.5V otherwise				
D031		with Schmitt Trigger input	Vss		0.2 Vdd	V					
D032		MCLR, RA4/T0CKI,OSC1 (in RC mode)	Vss	-	0.2 Vdd	V	(Note1)				
D033		OSC1 (in XT* and HS)	Vss	—	0.3 Vdd	V					
		OSC1 (in LP*)	Vss	—	0.6 Vdd-1.0	V					
	Vін	Input High Voltage		1			1				
		I/O ports		—							
D040		with TTL buffer	2.0V 0.8 + 0.25 VDD		Vdd Vdd	V V	VDD = 4.5V to 5.5V otherwise				
D041		with Schmitt Trigger input	0.8V		Vdd						
D042		MCLR RA4/T0CKI	0.8 Vdd	—	Vdd	V					
D043 D043A		OSC1 (XT*, HS and LP*) OSC1 (in RC mode)	0.7 Vdd 0.9 Vdd	—	Vdd	V	(Note1)				
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS				
	lı∟	Input Leakage Current ⁽²⁾⁽³⁾									
		I/O ports (Except PORTA)			±1.0	μA	VSS \leq VPIN \leq VDD, pin at hi-impedance				
D060		PORTA	—	_	±0.5	μA	$Vss \leq VPIN \leq VDD, pin at hi-impedance$				
D061		RA4/T0CKI	—	—	±1.0	μΑ	$Vss \leq V \text{PIN} \leq V \text{DD}$				
D063		OSC1, MCLR	—	_	±5.0	μA	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration				
	Vol	Output Low Voltage									
D080		I/O ports	—	-	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C				
			—	—	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C				
D083		OSC2/CLKOUT	—	—	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C				
		(RC only)	—	—	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C				
	Vон	Output High Voltage ⁽³⁾									
D090		I/O ports (Except RA4)	VDD-0.7	_		V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C55X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

Watchdog Timer RESET

I/O Pins



FIGURE 10-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP

TABLE 10-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

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Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2000		—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Timeout Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc	—	—	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	$VDD = 5.0V, -40^{\circ} \text{ to } +85^{\circ}C$
34 TIOZ I/O hi-impedance from MCLR low				2.0*	μs		
*	Those pr	remotore are oberectorized but not	tootod				

These parameters are characterized but not tested.

Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

Package Marking Information (Cont'd)



Example PIC16C558 -04I / S0218 S0218 9818 CDK

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18-Lead CERDIP Windowed



Example



28-Lead CERDIP Windowed



Example



18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		18			18		
Pitch	р		.100			2.54		
Top to Seating Plane	А	.140	.155	.170	3.56	3.94	4.32	
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26	
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60	
Overall Length	D	.890	.898	.905	22.61	22.80	22.99	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78	
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-007