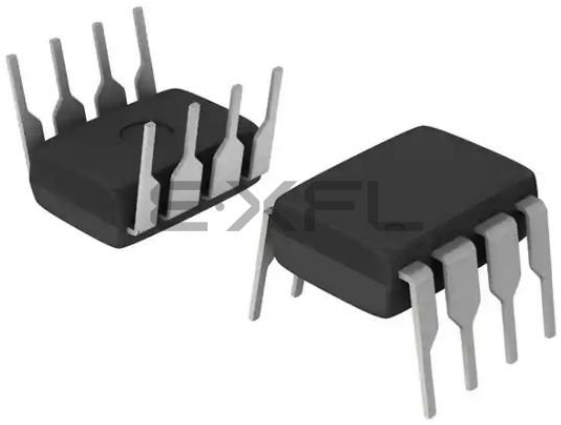

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c25122-24pi

Getting Started in the PSoC World!

The award winning PSoC Designer software and PSoC silicon are an integrated unit. The quickest path to understanding the PSoC silicon is through the PSoC Designer software GUI. This data sheet is useful for understanding the details of the PSOC integrated circuit, but is not a good starting point for a new PSoC developer seeking to get a general overview of this new technology.

PSoC developers are NOT required to build their own ADCs, DACs, and other peripherals. Embedded in the PSoC Designer software are the individual data sheets, performance graphs, and PSoC User Modules (graphically selected code packets) for the peripherals, such as the incremental ADCs, DACs, LCD controllers, op amps, low-pass filters, etc. **With simple GUI-based selection, placement, and connection, the basic architecture of a design may be developed within PSoC Designer software without ever writing a single line of code**.

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store also contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

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The PSoC™ CY8C25122/CY8C26233/CY8C26443/CY8C26643 family of programmable system-on-chip devices replace multiple MCU-based system components with one single-chip, configurable device. A PSoC device includes configurable analog and digital peripheral blocks, a fast CPU, Flash program memory, and SRAM data memory in a range of convenient pin-outs and memory sizes. The driving force behind this innovative programmable system-on-chip comes from user configurability of the analog and digital arrays: the PSoC blocks.

Programmable System-on-Chip (PSoC™) Blocks

- On-chip, user configurable analog and digital peripheral blocks
- PSoC blocks can be used individually or in combination
- 12 Analog PSoC blocks provide:
  - Up to 11-bit Delta-Sigma ADC
  - Up to 8-bit Successive Approximation ADC
  - Up to 12-bit Incremental ADC
  - Up to 9-bit DAC
  - Programmable gain amplifier
  - Programmable filters
  - Differential comparators
- 8 Digital PSoC blocks provide:
  - Multipurpose timers: event timing, real-time clock, pulse width modulation (PWM) and PWM with deadband
  - CRC modules
  - Full-duplex UARTs
  - SPI™ master or slave configuration
  - Flexible clocking sources for analog PSoC blocks

Powerful Harvard Architecture Processor with Fast Multiply/Accumulate

- M8C processor instruction set
- Processor speeds to 24 MHz
- Register speed memory transfers
- Flexible addressing modes
- Bit manipulation on I/O and memory
- 8x8 multiply, 32-bit accumulate

Flexible On-Chip Memory

- Flash program storage, 4K to 16K bytes, depending on device
- 50,000 erase/write cycles
- 256 bytes SRAM data storage
- In-System Serial Programming (ISSP™)
- Partial Flash updates
- Flexible protection modes
- EEPROM emulation in Flash, up to 2,304 bytes

Programmable Pin Configurations

- Schmitt trigger TTL I/O pins
- Logic output drive to 25 mA with internal pull-up or pull-down resistors, High Z, or strong driver
- Interrupt on pin change
- Analog output drive to 40 mA

Precision, Programmable Clocking

- Internal 24/48 MHz Oscillator (+/- 2.5%, no external components)
- External 32.768 kHz Crystal Oscillator (optional precision source for PLL)
- Internal Low Speed Oscillator for Watchdog and Sleep

Dedicated Peripherals

- Watchdog and Sleep Timers
- Low Voltage Detection with user-configurable threshold voltages
- On-chip voltage reference

Fully Static CMOS Devices using advanced Flash technology

- Low power at high speed
- Operating voltage from 3.0 to 5.25 V
- Operating voltage down to 1.0 V using on-chip switch mode voltage pump
- Wide temperature range: -40 °C to + 85 °C

Complete Development Tools

- Powerful integrated development environment (PSoC™ Designer)
- Low-cost, in-circuit emulator and programmer

4.3 Register Bank 1 Map

Table 27: Bank 1

Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access
PRT0DM0	00h	32	W	Reserved	40h			ASA10CR0	80h	88	RW	Reserved	C0h		
PRT0DM1	01h	33	W		41h			ASA10CR1	81h	90	RW		C1h		
PRT0IC0	02h	33	W		42h			ASA10CR2	82h	92	RW		C2h		
PRT0IC1	03h	34	W		43h			ASA10CR3	83h	93	RW		C3h		
PRT1DM0	04h	32	W		44h			ASB11CR0	84h	95	RW		C4h		
PRT1DM1	05h	33	W		45h			ASB11CR1	85h	97	RW		C5h		
PRT1IC0	06h	33	W		46h			ASB11CR2	86h	99	RW		C6h		
PRT1IC1	07h	34	W		47h			ASB11CR3	87h	100	RW		C7h		
PRT2DM0	08h	32	W		48h			ASA12CR0	88h	88	RW		C8h		
PRT2DM1	09h	33	W		49h			ASA12CR1	89h	90	RW		C9h		
PRT2IC0	0Ah	33	W		4Ah			ASA12CR2	8Ah	92	RW		CAh		
PRT2IC1	0Bh	34	W		4Bh			ASA12CR3	8Bh	93	RW		CBh		
PRT3DM0	0Ch	32	W		4Ch			ASB13CR0	8Ch	95	RW		CCh		
PRT3DM1	0Dh	33	W		4Dh			ASB13CR1	8Dh	97	RW		CDh		
PRT3IC0	0Eh	33	W		4Eh			ASB13CR2	8Eh	99	RW		CEh		
PRT3IC1	0Fh	34	W		4Fh			ASB13CR3	8Fh	100	RW		CFh		
PRT4DM0	10h	32	W		50h			ASB20CR0	90h	95	RW		D0h		
PRT4DM1	11h	33	W		51h			ASB20CR1	91h	97	RW		D1h		
PRT4IC0	12h	33	W		52h			ASB20CR2	92h	99	RW		D2h		
PRT4IC1	13h	34	W		53h			ASB20CR3	93h	100	RW		D3h		
PRT5DM0	14h	32	W		54h			ASA21CR0	94h	88	RW		D4h		
PRT5DM1	15h	33	W		55h			ASA21CR1	95h	90	RW		D5h		
PRT5IC0	16h	33	W		56h			ASA21CR2	96h	92	RW		D6h		
PRT5IC1	17h	34	W		57h			ASA21CR3	97h	93	RW		D7h		
Reserved	18h				58h			ASB22CR0	98h	95	RW		D8h		
	19h				59h			ASB22CR1	99h	97	RW		D9h		
	1Ah				5Ah			ASB22CR2	9Ah	99	RW		DAh		
	1Bh				5Bh			ASB22CR3	9Bh	100	RW		DBh		
	1Ch				5Ch			ASA23CR0	9Ch	88	RW		DCh		
	1Dh				5Dh			ASA23CR1	9Dh	90	RW		DDh		
	1Eh				5Eh			ASA23CR2	9Eh	92	RW		DEh		
	1Fh				5Fh			ASA23CR3	9Fh	93	RW		DFh		
DBA00FN	20h	50	RW	CLK_CR0	60h	76	RW	Reserved	A0h			OSC_CR0	E0h	40	RW
DBA00IN	21h	51	RW	CLK_CR1	61h	77	RW		A1h			OSC_CR1	E1h	40	RW
DBA00OU	22h	53	RW	ABF_CR	62h	106	W		A2h			Reserved	E2h		
Reserved	23h			AMD_CR	63h	107	RW		A3h			VLT_CR	E3h	118	RW
DBA01FN	24h	50	RW	Reserved	64h				A4h			Reserved	E4h		
DBA01IN	25h	51	RW		65h				A5h			Reserved	E5h		
DBA01OU	26h	53	RW		66h				A6h			Reserved	E6h		
Reserved	27h				67h				A7h			Reserved	E7h		
DBA02FN	28h	50	RW		68h				A8h			IMO_TR	E8h	35	W
DBA02IN	29h	51	RW		69h				A9h			ILO_TR	E9h	36	W
DBA02OU	2Ah	53	RW		6Ah				AAh			BDG_TR	EAh	120	W
Reserved	2Bh				6Bh				ABh			ECO_TR	EBh	37	W
DBA03FN	2Ch	50	RW		6Ch				ACh			Reserved	ECh		
DBA03IN	2Dh	51	RW		6Dh				ADh				EDh		
DBA03OU	2Eh	53	RW		6Eh				AEh				EEh		
Reserved	2Fh				6Fh				AFh				EFh		
DCA04FN	30h	50	RW		70h				B0h				F0h		
DCA04IN	31h	51	RW	ACA00CR0	71h	82	RW		B1h				F1h		
DCA04OU	32h	53	RW	ACA00CR1	72h	83	RW		B2h				F2h		
Reserved	33h			ACA00CR2	73h	84	RW		B3h				F3h		
DCA05FN	34h	50	RW	Reserved	74h				B4h				F4h		
DCA05IN	35h	51	RW	ACA01CR0	75h	82	RW		B5h				F5h		
DCA05OU	36h	53	RW	ACA01CR1	76h	83	RW		B6h				F6h		
Reserved	37h			ACA01CR2	77h	84	RW		B7h				F7h		
DCA06FN	38h	50	RW	Reserved	78h				B8h				F8h		
DCA06IN	39h	51	RW	ACA02CR0	79h	82	RW		B9h				F9h		
DCA06OU	3Ah	53	RW	ACA02CR1	7Ah	83	RW		BAh				FAh		
Reserved	3Bh			ACA02CR2	7Bh	84	RW		BBh				FBh		
DCA07FN	3Ch	50	RW	Reserved	7Ch				BCh				FCh		
DCA07IN	3Dh	51	RW	ACA03CR0	7Dh	82	RW		BDh				FDh		
DCA07OU	3Eh	53	RW	ACA03CR1	7Eh	83	RW		BEh				FEh		
Reserved	3Fh			ACA03CR2	7Fh	84	RW		BFh			CPU_SCR	FFh	114	[1]

1. Read/Write access is bit-specific or varies by function. See register.

6.3.2 Port Drive Mode 1 Registers

Table 32: Port Drive Mode 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	DM1 [7]	DM1 [6]	DM1 [5]	DM1 [4]	DM1 [3]	DM1 [2]	DM1 [1]	DM1 [0]
Bit [7:0]: **DM1 [7:0]** See truth table for Port Drive Mode 0 Registers, above								

Port 0 Drive Mode 1 Register (PRT0DM1, Address = Bank 1, 01h)
Port 1 Drive Mode 1 Register (PRT1DM1, Address = Bank 1, 05h)
Port 2 Drive Mode 1 Register (PRT2DM1, Address = Bank 1, 09h)
Port 3 Drive Mode 1 Register (PRT3DM1, Address = Bank 1, 0Dh)
Port 4 Drive Mode 1 Register (PRT4DM1, Address = Bank 1, 11h)
Port 5 Drive Mode 1 Register (PRT5DM1, Address = Bank 1, 15h) **Note**: Port 5 is 4-bits wide

6.3.3 Port Interrupt Control 0 Registers

Table 33: Port Interrupt Control 0 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	IC0 [7]	IC0 [6]	IC0 [5]	IC0 [4]	IC0 [3]	IC0 [2]	IC0 [1]	IC0 [0]
Bit [7:0]: **IC0 [7:0]** The two Interrupt Control bits that control a particular port pin are treated as a pair and are decoded as follows: IC1 [x], IC0 [x] = 0 0 = Disabled (Default) IC1 [x], IC0 [x] = 0 1 = Falling Edge (-) IC1 [x], IC0 [x] = 1 0 = Rising Edge (+) IC1 [x], IC0 [x] = 1 1 = Change from Last Direct Read								

Port 0 Interrupt Control 0 Register (PRT0IC0, Address = Bank 1, 02h)
Port 1 Interrupt Control 0 Register (PRT1IC0, Address = Bank 1, 06h)
Port 2 Interrupt Control 0 Register (PRT2IC0, Address = Bank 1, 0Ah)
Port 3 Interrupt Control 0 Register (PRT3IC0, Address = Bank 1, 0Eh)
Port 4 Interrupt Control 0 Register (PRT4IC0, Address = Bank 1, 12h)
Port 5 Interrupt Control 0 Register (PRT5IC0, Address = Bank 1, 16h) **Note**: Port 5 is 4-bits wide

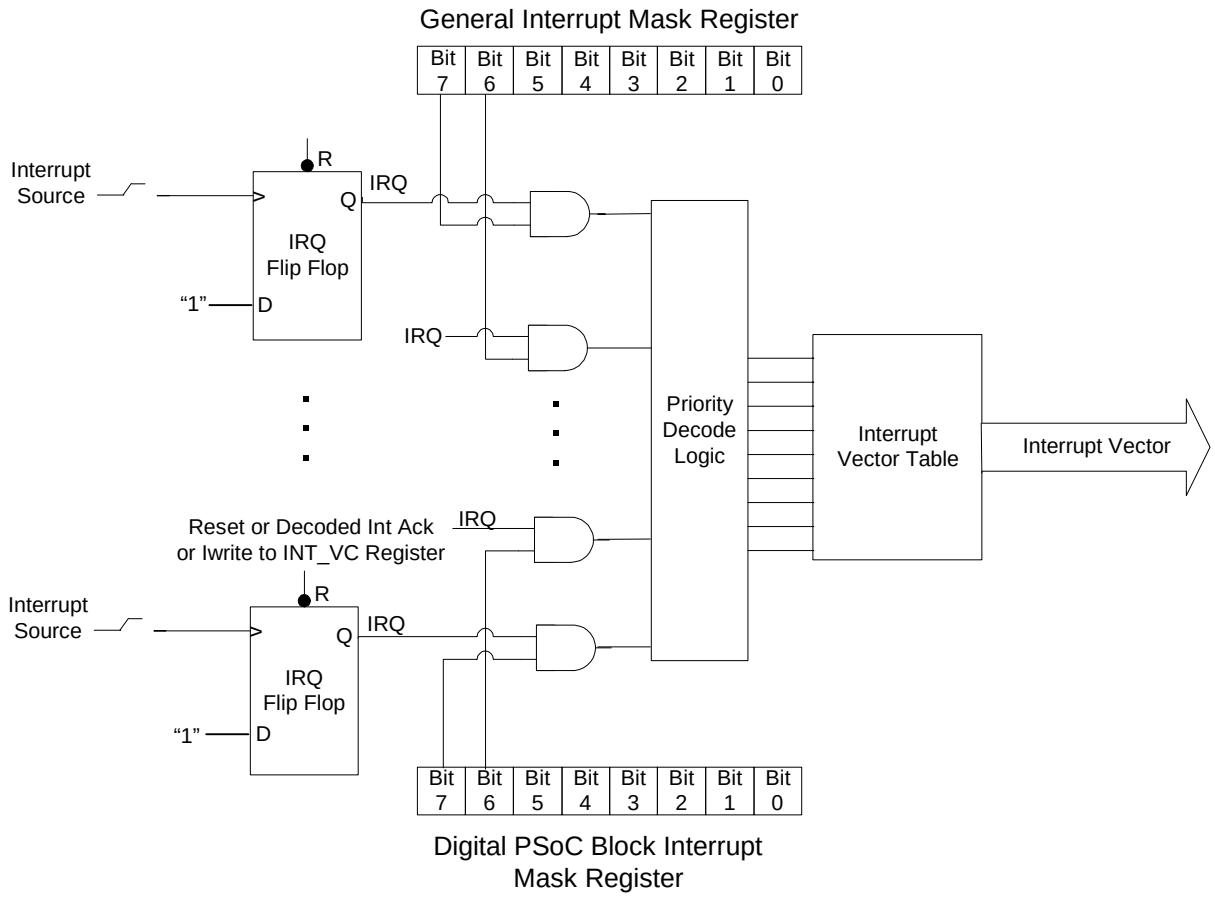

Figure 10: Interrupts Overview

8.6 GPIO Interrupt

GPIO Interrupts are polarity configurable and pin-wise maskable (within each Port's pin configuration registers). They all share the same interrupt priority and vector.

Any general purpose I/O can be used as an interrupt source. The GPIO bit in the General Interrupt Mask Register (INT_MSK0) must be set to enable pin interrupts, as well as the enable bits for each pin, which are located in the Port x Interrupt Enable Registers (PRTxIE). There are user selectable options to generate an interrupt on 1) any change from the last read state, 2) rising edge, and 3) falling edge.

When Interrupt on Change is selected, the state of the GPIO pin is stored when the port is read. Changes from this state will then assert the interrupt, if enabled.

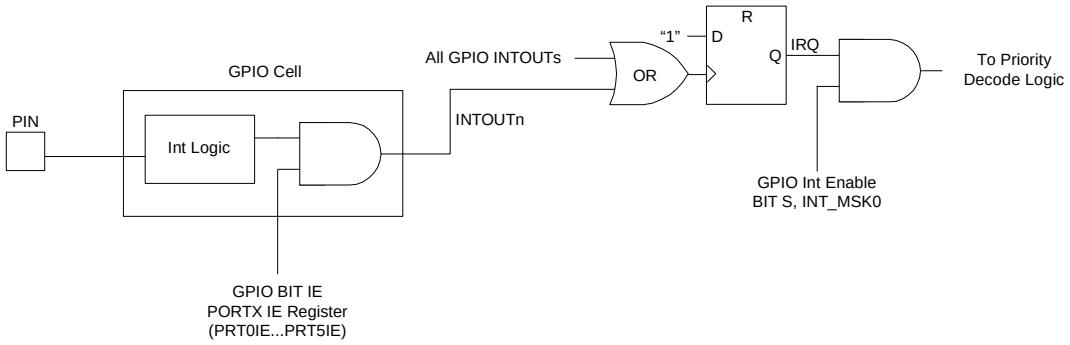

Figure 11: GPIO Interrupt Enable Diagram

For a GPIO interrupt to occur, the following steps must be taken:

1. The pin Drive Mode must be set so the pin can be an input.
2. The pin must be enabled to generate an interrupt by setting the appropriate bit in the Port interrupt Enable Register (PRTxIE).
3. The edge type for the interrupt must be set in the Port Interrupt Control 0 and Control 1 Registers (PRTxIC0 and PRTxIC1). Edge type must be set to a value other than 00.
4. The GPIO bit must be set in the General Interrupt Mask Register (INT_MSK0).
5. The Global Interrupt Enable bit must be set.
6. Because the GPIO interrupts all share the same interrupt vector, the source for the GPIO interrupt must be cleared before any other GPIO interrupt will occur (i.e., the OR gate in Figure 11: "ors" all of the INTOUTn signals together). If any of the INTOUTn signals are high, the flip-flop in Figure 11: will not see a rising edge and no IRQ will occur.

9.0 Digital PSoC Blocks

9.1 Introduction

PSoC blocks are user configurable system resources. On-chip digital PSoC blocks reduce the need for many MCU part types and external peripheral components. Digital PSoC blocks can be configured to provide a wide variety of peripheral functions. PSoC Designer Software Integrated Development Environment provides automated configuration of PSoC blocks by simply selecting the desired functions. PSoC Designer then generates the proper configuration information and can print a device data sheet unique to that configuration.

Digital PSoC blocks provide up to eight, 8-bit multipurpose timers/counters supporting multiple event timers, real-time clocks, Pulse Width Modulators (PWM), and CRCs. In addition to all PSoC block functions, communication PSoC blocks support full-duplex UARTs and SPI master or slave functions.

As shown in Figure 12:, there are a total of eight 8-bit digital PSoC blocks in this device family configured as a linear array. Four of these are the Digital Basic Type A blocks and four are the Digital Communications Type A blocks. Each of these digital PSoC blocks can be configured independently, or used in combination.

Each digital PSoC block has a unique Interrupt Vector and Interrupt Enable bit. Functions can be stopped or started with a user-accessible Enable bit.

The Timer/Counter/CRC/PRS/Deadband functions are available on the Digital Basic Type A blocks and also the Digital Communications Type A blocks. The UART and SPI communications functions are only available on the Digital Communications Type A blocks.

There are three configuration registers: the Function Register (DBA00FN-DCA07FN) to select the block function and mode, the Input Register (DBA00IN-DCA07IN) to select data input and clock selection, and the Output Register (DBA00OU-DCA07OU) to select and enable function outputs.

The three data registers are designated Data 0 (DBA00DR0-DCA07DR0), Data 1 (DBA00DR1-DCA07DR1), and Data 2 (DBA00DR2-DCA07DR2). The function of these registers and their bit mapping is dependent on the overall block function selected by the user.

The one Control Register (DBA00CR0-DCA07CR0) is designated Control 0. The function of this register and its bit mapping is dependent on the overall block function selected by the user.

If the CPU frequency is 24 MHz and a PSoC timer/counter of 24-bits or longer is operating at 48 MHz, a write to the block Control Register to enable it (for example, a call to Timer_1_Start) may not start the block properly. In the failure case, the first count will typically be indeterminate as the upper bytes fail to make the first count correctly. However, on the first terminal count, the correct period will be loaded and counted thereafter.

Digital Communications Type A Block 05 Function Register (DCA05FN, Address = Bank 1, 34h)
Digital Communications Type A Block 06 Function Register (DCA06FN, Address = Bank 1, 38h)
Digital Communications Type A Block 07 Function Register (DCA07FN, Address = Bank 1, 3Ch)

9.2.2 Digital Basic Type A / Communications Type A Block xx Input Register

The Digital Basic Type A / Communications Type A Block xx Input Register (DBA00IN-DCA07IN) consists of 4 bits [3:0] to select the block input clock and 4 bits [7:4] to select the primary data/enable input. The actual usage of the input data/enable is function dependent.

Table 48: Digital Basic Type A / Communications Type A Block xx Input Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [3]	Data [2]	Data [1]	Data [0]	Clock [3]	Clock [2]	Clock [1]	Clock [0]

Bit [7:4]: **Data [3:0] Data Enable Source Select**
0 0 0 0 = Data = 0
0 0 0 1 = Data = 1
0 0 1 0 = Digital Block 03
0 0 1 1 = Chain Function to Previous Block
0 1 0 0 = Analog Column Comparator 0
0 1 0 1 = Analog Column Comparator 1
0 1 1 0 = Analog Column Comparator 2
0 1 1 1 = Analog Column Comparator 3
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Bit [3:0]: **Clock [3:0] Clock Source Select**
0 0 0 0 = Clock Disabled
0 0 0 1 = Global Output[4] (for Digital Blocks 00 to 03) **or** Global Output[0] (for Digital Blocks 04 to 07)
0 0 1 0 = Digital Block 03 (Primary Output)
0 0 1 1 = Previous Digital PSoC block (Primary Output)
0 1 0 0 = 48M
0 1 0 1 = 24V1
0 1 1 0 = 24V2
0 1 1 1 = 32k
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Digital Basic Type A Block 00 Input Register (DBA00IN, Address = Bank 1, 21h)
Digital Basic Type A Block 01 Input Register (DBA01IN, Address = Bank 1, 25h)
Digital Basic Type A Block 02 Input Register (DBA02IN, Address = Bank 1, 29h)
Digital Basic Type A Block 03 Input Register (DBA03IN, Address = Bank 1, 2Dh)
Digital Communications Type A Block 04 Input Register (DCA04IN, Address = Bank 1, 31h)
Digital Communications Type A Block 05 Input Register (DCA05IN, Address = Bank 1, 35h)

Table 50: Digital Basic Type A / Communications Type A Block xx Output Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Reserved	AUX Out Enable	AUX IO Sel [1]	AUX IO Sel [0]	Out Enable	Out Sel [1]	Out Sel [0]

Bit 7: **Reserved**
Bit 6: **Reserved**

Bit 5: **AUX Out Enable**
0 = Disable Auxiliary Output
1 = Enable Auxiliary Output (function dependent)

Bit [4:3]: **AUX IO Sel [1:0] Function-dependent selection of auxiliary input or output**
0 0 = Drive Global Output[0] (for Digital Blocks 00 to 03) **or**
Input from Global Input[4] or Drive Global Output [4] (for Digital Blocks 04 to 07)
0 1 = Drive Global Output[1] (for Digital Blocks 00 to 03) **or**
Input from Global Input[5] or Drive Global Output[5] (for Digital Blocks 04 to 07)
1 0 = Drive Global Output[2] (for Digital Blocks 00 to 03) **or**
Input from Global Input[6] or Drive Global Output[6] (for Digital Blocks 04 to 07)
1 1 = Drive Global Output[3] (for Digital Blocks 00 to 03) **or**
Input from Global Input[7] or Drive Global Output[7] (for Digital Blocks 04 to 07)

Bit 2: **Out Enable**
0 = Disable Primary Output
1 = Enable Primary Output (function dependant)

Bit [1:0]: **Out Sel [1:0]** Primary Output
0 0 = Drive Global Output[0] (for Digital Blocks 00 to 03) **or** Drive Global Output[4] (for Digital Blocks 04 to 07)
0 1 = Drive Global Output[1] (for Digital Blocks 00 to 03) **or** Drive Global Output[5] (for Digital Blocks 04 to 07)
1 0 = Drive Global Output[2] (for Digital Blocks 00 to 03) **or** Drive Global Output[6] (for Digital Blocks 04 to 07)
1 1 = Drive Global Output[3] (for Digital Blocks 00 to 03) **or** Drive Global Output[7] (for Digital Blocks 04 to 07)

Digital Basic Type A Block 00 Output Register (DBA00OU, Address = Bank 1, 22h)
Digital Basic Type A Block 01 Output Register (DBA01OU, Address = Bank 1, 26h)
Digital Basic Type A Block 02 Output Register (DBA02OU, Address = Bank 1, 2Ah)
Digital Basic Type A Block 03 Output Register (DBA03OU, Address = Bank 1, 2Eh)
Digital Communications Type A Block 04 Output Register (DCA04OU, Address = Bank 1, 32h)
Digital Communications Type A Block 05 Output Register (DCA05OU, Address = Bank 1, 36h)
Digital Communications Type A Block 06 Output Register (DCA06OU, Address = Bank 1, 3Ah)
Digital Communications Type A Block 07 Output Register (DCA07OU, Address = Bank 1, 3Eh)

The Primary Output is the source for “Previous Digital PSoC Block” or “Digital Block 03,” selections for the “Clock Source Select” in the Digital Basic Type A/Communications Type A Block xx Input Register (Table 48 on page 51).

A digital PSoC block may have 0, 1, or 2 outputs depending on its function, as shown in the following table:

9.5.4.6 Determining the Polynomial

A simple linear-feedback shift register, or LFSR, uses an XOR gate to “add” the values of one or more bits and feed the result back into the least-significant bit. One possible realization of a 6-bit LFSR providing a maximal sequence of 63 six-bit values is shown here:

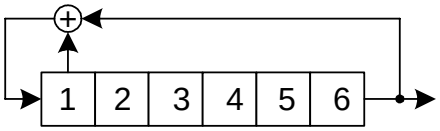

Figure 13: Polynomial LFSR

The PRS function utilizes a different “modular” architecture with one XOR gate between each bit of the shift register. A maximal sequence equivalent to that produced by the previous realization is generated by the following modular LFSR

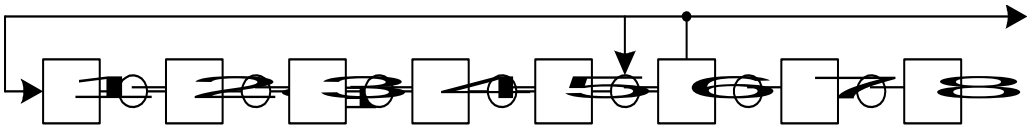

Figure 14: Polynomial PRS

Denote the first implementation as a (6, 1) LFSR, where 6 gives the length of the output codes and 1 indicates the tap which feeds the XOR gate along with the final bit. Then the modular form just shown is denoted as a [6, 5] LFSR. In general, the equivalent modular form of a simple N bit LFSR with M taps denoted by (N, t_1, t_2, …, t_M) is given by the notation [N, N-t_1, N-t_2, …, N-t_M]. Once the form (and thus the notation) is determined, the value of Data Register 1 is easily determined. The bit corresponding to the length and all tap bits are turned on; the others are zero. Thus, the polynomial specification for Data Register 1 to implement a [6, 5] LFSR is 00110000b, or 30h. A maximal sequence PRS for 8-bits giving 255 codes is [8, 4, 3, 2] with polynomial 10001110b or 8Eh.

9.5.4.7 Usage Notes

1. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 2 (Seed) is loaded directly into Data Register 0 (LFSR) to initialize or reset the seed value. All outputs are low and the block interrupt is held low.

2. Reading the LFSR

   The current LFSR value can only be read when the block is disabled by setting the Control Register bit 0 to low. Each byte of the current LFSR value (in the case of a multi-byte block) must be read individually. The Data Register 0 byte (LFSR), which returns 0, then the Data Register 1 byte, which returns the actual value.

9.5.5 CRC - Cyclic Redundancy Check

9.5.5.1 Summary

The CRC uses a shift register and XOR gates like the PRS function. However, instead of an output bit stream, the CRC function expects an input bit stream. Functionally the CRC block is identical to the PRS with the exception of the selected input data. Input data must be presented synchronously to the clock. A polynomial specification permits the length of the input sequence over which the cyclic redundancy check computes a result to be varied. CRC-configured PSoC blocks can be chained to form longer results.

9.5.5.2 Registers

Data Register 0 implements a linear-feedback shift register. Data Register 2 holds the “seed” value and when the block is disabled, a write to Data Register 2 is loaded

10.8.3.3 Analog Switch Cap Type A Block xx Control 2 Register

AnalogBus gates the output to the analog column bus. The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASA10CR0, ASA12CR0, ASA21CR0, ASA23CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the signal that is output to the analog column bus is selected by the ClockPhase bit. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus.

CompBus controls the output to the column comparator bus. Note that if the comparator bus is not driven by anything in the column, it is pulled low. The comparator output is evaluated on the rising edge of internal PHI1 and is latched so it is available during internal PHI2.

AutoZero controls the shorting of the output to the inverting input of the op-amp. When shorted, the op-amp is basically a follower. The output is the op-amp offset. By using the feedback capacitor of the integrator, the block can memorize the offset and create an offset cancellation scheme. AutoZero also controls a pair of switches between the A and B branches and the summing node of the op-amp. If AutoZero is enabled, then the pair of switches is active. AutoZero also affects the function of the FSW1 bit in Control 3 Register.

The CCap bits set the value of the capacitor in the C path.

10.9.2.2 Analog Switch Cap Type B Block xx Control 1 Register

AMux controls the input muxing for the A capacitor branch.

The BCap bits set the value of the capacitor in the B path.

Table 74: Analog Switch Cap Type B Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AMux[2]	AMux[1]	AMux[0]	BCap[4]	BCap[3]	BCap[2]	BCap[1]	BCap[0]

Bit [7:5]: **AMux [2:0]** Input muxing select for A capacitor branch. (Note that available mux inputs vary by individual PSoC block.)

ASB11	ASB13	ASB20	ASB22
0 0 0 = ACA01	ACA03	ASA10	ASA12
0 0 1 = ASA12	P2.2	P2.1	ASA21
0 1 0 = ASA10	ASA12	ASA21	ASA23
0 1 1 = ASA21	ASA23	ABUS0	ABUS2
1 0 0 = REFHI	REFHI	REFHI	REFHI
1 0 1 = ACA00	ACA02	ASB11	ASB13
1 1 0 = Reserved	Reserved	Reserved	Reserved
1 1 1 = Reserved	Reserved	Reserved	Reserved

Bit [4:0]: BCap [4:0] Binary encoding for 32 possible capacitor sizes for B Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 1 Register (ASB11CR1, Address = Bank 0/1, 85h)
Analog Switch Cap Type B Block 13 Control 1 Register (ASB13CR1, Address = Bank 0/1, 8Dh)
Analog Switch Cap Type B Block 20 Control 1 Register (ASB20CR1, Address = Bank 0/1, 91h)
Analog Switch Cap Type B Block 22 Control 1 Register (ASB22CR1, Address = Bank 0/1, 99h)

10.9.2.4 Analog Switch Cap Type B Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASB11CR2, ASB13CR2, ASB20CR2, ASB22CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BSW is used to control switching in the B branch. If disabled, the B capacitor branch is a continuous time branch like the C branch of the SC A Block. If enabled, then on internal PHI1, both ends of the cap are switched to analog ground. On internal PHI2, one end is switched to the B input and the other end is switched to the summing node.

BMuxSCB controls muxing to the input of the B capacitor branch. The B branch can be switched or unswitched.

Table 76: Analog Switch Cap Type B Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BSW	BMuxSCB	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
FSW1 bit is set to 1; the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit 3: **BSW** Enable switching in branch
0 = B branch is a continuous time path
1 = B branch is switched with internal PHI2 sampling

Bit 2: **BMuxSCB** Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block)
ASB11 ASB13 ASB20 ASB22
0 = ACA00 ACA02 ASB11 ASB13
1 = ACA01 ACA03 ASA10 ASA12

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type B Block 11 Control 3 Register (ASB11CR3, Address = Bank 0/1, 87h)
Analog Switch Cap Type B Block 13 Control 3 Register (ASB13CR3, Address = Bank 0/1, 8Fh)
Analog Switch Cap Type B Block 20 Control 3 Register (ASB20CR3, Address = Bank 0/1, 93h)
Analog Switch Cap Type B Block 22 Control 3 Register (ASB22CR3, Address = Bank 0/1, 9Bh)

The SAR hardware accelerator is a block of specialized hardware designed to sequence the SAR algorithm for efficient A/D conversion. A SAR ADC is implemented conceptually with a DAC of the desired precision, and a comparator. This functionality can be configured from one or more PSoC blocks. For each conversion, the firmware should initialize the ASY_CR register as defined below, and set the sign bit of the DAC as the first guess in the algorithm. A sequence of OR instructions (Read, Modify, Write) to the DAC (CR0) register is then executed. Each of these OR instructions causes the SAR hardware to read the current state of the comparator, checking the validity of the previous guess. It either clears it or leaves it set, accordingly. The next LSB in the DAC register is also set as the next guess. Six OR instructions will complete the conversion of a 6-bit DAC. The resulting DAC code, which matches the input voltage to within 1 LSB, is then read back from the DAC CR0 register.

10.11.1 Analog Stall and Analog Stall Lockup

Stall lockup affects the operation of stalled IO writes, such as DAC writes and the stalled IOR of the SAR hardware accelerator. The DAC and SAR User Modules operate in this mode. The analog column clock frequency must not be a power of two multiple (2, 4, 8...) higher than the CPU clock frequency. Under this condition, the CPU will never recover from a stall.

See the list of relationships (in MHz) that will fail:

Table 78: Analog Frequency Relationships

Analog Column Clock	CPU Clock
3.	1.5, 0.75, .018, 0.093
1.5	0.75, 0.18, 0.093
0.75	0.18, 0.093
0.37	0.18, 0.093
0.18	0.093

You can still run the CPU clock slower than the column clock if the relationship is not a power of two multiple. For example, you can run at 0.6 MHz, which is not a power of two multiple of any CPU frequency and therefore any CPU frequency can be selected. If the CPU frequency is greater than or equal to the analog column clock, there is not a problem.

Table 79: Analog Synchronization Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	--	W	W	W	RW	RW	RW	RW
Bit Name	Reserved	SARCOUNT [2]	SARCOUNT [1]	SARCOUNT [0]	SAR-SIGN	SARCOL [1]	SARCOL [0]	SYN-CEN

Bit 7: **Reserved**

Bit [6:4]: **SARCOUNT [2:0]** Initial SAR count. Load this field with the number of bits to process. In a typical 6-bit SAR, the value would be 6

Bit 3: **SARSIGN** Adjust the SAR comparator based on the type of block addressed. In a DAC configuration with more than one PSoC block (more than 6-bits), this bit would be 0 when processing the most significant block and 1 when processing the least significant block. This is because the least significant block of a DAC is an inverting input to the most significant block

Bit [2:1]: **SARCOL [1:0]** Column select for SAR comparator input. The DAC portion of the SAR can reside in any of the appropriate positions in the analog PSOC block array. However, once the comparator block is positioned (and it is possible to have the DAC and comparator in the same block), this should be the column selected

Bit 0: **SYNCEN** Set to 1, will stall the CPU until the rising edge of PHI1, if a write to a register within an analog Switch Cap block takes place

Analog Synchronization Control Register (ASY_CR, Address = Bank 0, 65h)

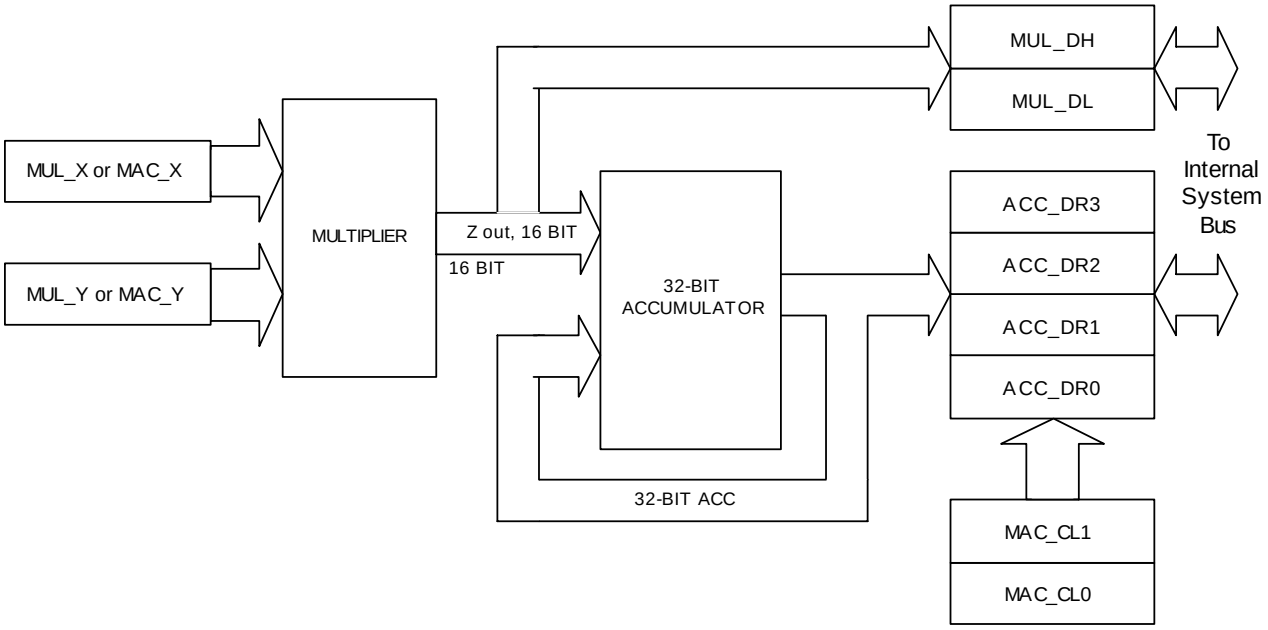

Figure 29: Multiply/Accumulate Block Diagram

Table 83: Multiply Input X Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]** 8-bit data is the input value for X multiplier								

Multiply Input X Register (MUL_X, Address = Bank 0, E8h)

Table 84: Multiply Input Y Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]** 8-bit data is the input value for Y multiplier								

Multiply Input Y Register (MUL_Y, Address = Bank 0, E9h)

This filter is implemented using a combination of hardware and software resources. Hardware is used to accumulate the high-speed in-coming data while the software is used to process the lower speed, enhanced resolution data for output.

Table 91: Decimator/Incremental Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	IGEN [3]	IGEN [2]	IGEN [1]	IGEN [0]	ICCKSEL	DCol [1]	DCol [0]	DCLKSEL

Bit [7:4]: **IGEN [3:0]** Individual enables for each analog column that gates the Analog Comparator based on the ICCKSEL input (Bit 3)

Bit 3: **ICCKSEL** Clock select for Incremental gate function
0 = Digital Basic Type A Block 02
1 = Digital Communications Type A Block 06

Bit [2:1]: **DCol [1:0]** Selects Analog Column Comparator source
0 0 = Analog Column Comparator 0
0 1 = Analog Column Comparator 1
1 0 = Analog Column Comparator 2
1 1 = Analog Column Comparator 3

Bit 0: **DCLKSEL** Clock select for Decimator latch
0 = Digital Basic Type A Block 02
1 = Digital Communications Type A Block 06

Decimator Incremental Register (DEC_CR, Address = Bank 0, E6h)

Table 92: Decimator Data High Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the high order byte within the 16-bit decimator data registers
Any 8-bit data value when written will cause both the Decimator Data High (DEC_DH) and Decimator Data Low (DEC_DL) registers to be cleared

Decimator High Register (DEC_DH / DEC_CL, Address = Bank 0, E4h)

Table 93: Decimator Data Low Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the low order byte within the 16 bit decimator data registers

Decimator Data Low Register (DEC_DL, Address = Bank 0, E5h)

11.6 Switch Mode Pump

This feature is available on the CY8C26xxx versions within this family. During the time Vcc is ramping from 0 Volts to POR V_{trip} (2.2V +/- 12%), IC operation is held off by the POR circuit and the Switch Mode Pump is enabled. The pump is realized by connecting an external inductor between the battery voltage and SMP, with an external diode pointing from SMP to the V_{cc} pin (which must have a bypass capacitance of at least 0.1uF connected to V_{cc}). This circuitry will pump Vcc to the Switch Mode Pump value specified in the Voltage Monitor Control Register (VLT_CR), shown above. Battery voltage values down to 0.9 V during operation are supported, but this circuitry is not guaranteed to start for battery voltages below 1.2 V. Once the IC is enabled after its power up and boot sequence, firmware can disable the SMP function by writing Voltage Monitor Control Register (VLT_CR) bit 7 to a 1.

When the IC is put into sleep mode, the power supply pump will remain running to maintain voltage. This may result in higher than specification sleep current depending upon application. If the user desires, the pump may be disabled during precision measurements (such as A/D conversions) and then re-enabled (writing B7 to 1 and then back to 0 again). The user, however, is responsible for making the operation happen quickly enough to guarantee supply holdup (by the bypass capacitor) sufficient for continued operation.

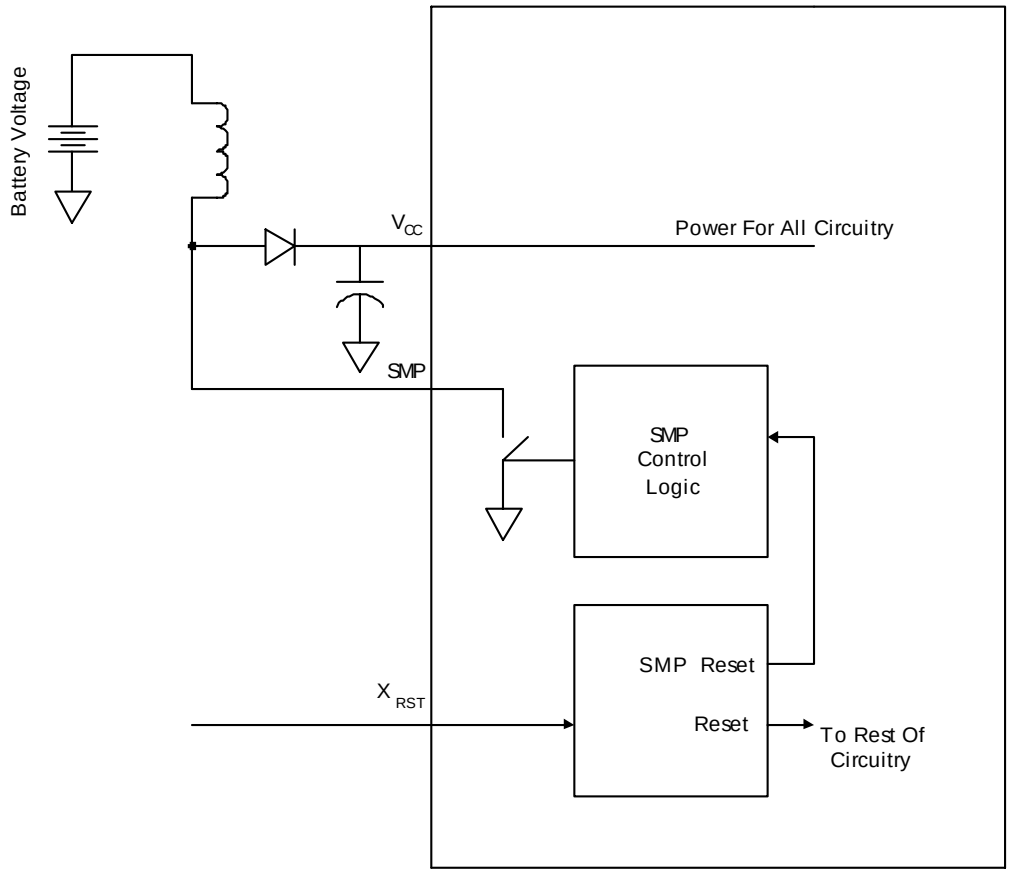

Figure 33: Switch Mode Pump

13.2.1 DC Operational Amplifier Specifications

13.2.1.1 5V Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and -40°C <= T_A <= 85°C. The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switch Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only. For 3.3V operation, see Table 106 on page 131.

Table 105: 5V DC Operational Amplifier Specifications

Symbol	5V DC Operational Amplifier Specifications	Minimum	Typical	Maximum	Unit
	Input Offset Voltage (Absolute Value)	-	7	30	mV
	Average Input Offset Voltage Drift	-	+24	-	µV/°C
	Input Leakage Current[1]	-	3	1000	nA
	Input Capacitance[2]	.30	.34	.40	pF
	Common Mode Voltage Range[3]	.5	-	V_{cc} - 1.0	VDC
	Common Mode Rejection Ratio	80	-	-	dB
	Open Loop Gain	80	-	-	dB
	High Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 V_{cc} - .4 V_{cc} - .4 V_{cc} - .4	 - - -	 - - -	 V V V
	Low Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 - - -	 - - -	 0.1 0.1 0.1	 V V V
	Supply Current (Including Associated AGND Buffer) Bias = Low Bias = Medium Bias = High	 - - -	 125 280 760	 300 600 1500	 µA µA µA
	Supply Voltage Rejection Ratio	60	-	-	dB

1. The leakage current includes the Analog Continuous Time PSoC block mux and the analog input mux. The leakage related to the General Purpose I/O pins is not included here.
2. The Input Capacitance includes the Analog Continuous Time PSoC block mux and the analog input mux. The capacitance of the General Purpose I/O pins is not included here.
3. The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.

15.0 Ordering Guide

Table 123: Ordering Guide (Leaded)[1]

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVI	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVI	16	256	Yes	Ind. -40C to +85C
48 Pin (600 Mil) Molded DIP	CY8C26643-24PI[2]	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AI	16	256	Yes	Ind. -40C to +85C

1. Orders for leaded devices will not be accepted after July 2005.
2. 48-PDIP package not offered Pb-Free.

Table 124: Ordering Guide (Pb-Free Denoted with an “X” in Ordering Code)

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PXI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26233-24SXIT	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVXI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP Tape and Reel	CY8C26233-24PVXIT	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26443-24SXIT	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVXI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP Tape and Reel	CY8C26443-24PVXIT	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVXI	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP Tape and Reel	CY8C26643-24PVXIT	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AXI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack Tape and Reel	CY8C26643-24AXIT	16	256	Yes	Ind. -40C to +85C

16.0 Document Revision History

Table 125: Document Revision History

Document Title: CY8C25122, CY8C26233, CY8C26443, CY8C26643 Device Data Sheet for Silicon Revision D **Document Number**: 38-12010				
Revision	**ECN #**	**Issue Date**	**Origin of Change**	**Description of Change**
**	116628	6/17/2002	CMS Cypress Management. New Silicon Revision.	New document to CY Document Control (Revision **). Revision 3.20 for CMS customers.
*A	127231	5/22/2003	HMT.	Implementing new error tracking and document release procedure. Changes in red for Document #: 38-12010 CY Rev. *A CMS Rev. 3.20a. Changes include: --Bit 6 of the VLT_CR register is RW. Should be changed from "RW" to "--." --Analog Output Buffer Control Register ABF_CR Read/Write in Bank 1 table was corrected to Write Only. --Rewrite of section 10.4 Analog Reference Control . --AC Char. Spec. table changed .080 to 80 in "Vdd Rise Rate at Power Up." On features pg. 2, changed "Up to 10 bit DAC" to "Up to 8 bit DAC." --Adding temp. spec. for 24 MHz at beginning of AC/DC Characteristics section and Absolute Maximum Value table. --In AC Operating Spec. table fixed footnote for Output Rise Time minimum. --In AC Operating Spec. table fixed value for External Reset Pulse Width. --Changed uS to us units in tables. --New intro. --In the Analog Reference Control Register, ARF_CR, state 100 for bits 2:0 should be described as "All Analog Off.“ --Rework title pgs.
*B	127231	5/22/2003	HMT.	Several updates including Thermal Impedances table, 8 PDIP diagram and company address. OSC_CR0 register name.
*C	362598	See ECN	HMT.	Add Pb-Free table. Add “Not Recommended for New Designs“ banner. Update package revisions. Fix register typo’s.
Distribution: External/Public **Posting**: None				