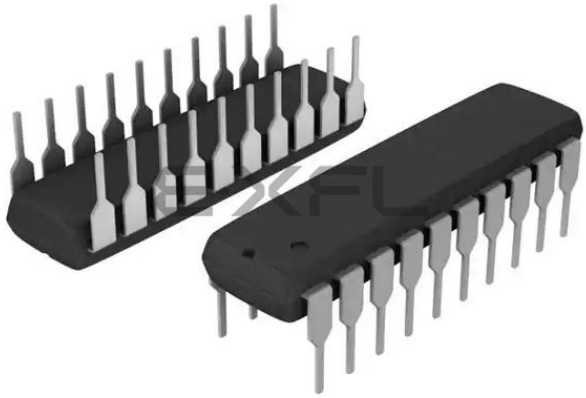

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Product Status	Obsolete
Core Processor	M8C
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Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26233-24pi

Table 6: Pin-out 48 Pin, continued

P5[0]	I/O	29	Port 5[0]
P5[2]	I/O	30	Port 5[2]
P4[0]	I/O	31	Port 4[0]
P4[2]	I/O	32	Port 4[2]
P4[4]	I/O	33	Port 4[4]
P4[6]	I/O	34	Port 4[6]
XRES	I	35	External Reset
P3[0]	I/O	36	Port 3[0]
P3[2]	I/O	37	Port 3[2]
P3[4]	I/O	38	Port 3[4]
P3[6]	I/O	39	Port 3[6]
P2[0]	I/O	40	Port 2[0] (Non-Multiplexed Analog Input)
P2[2]	I/O	41	Port 2[2] (Non-Multiplexed Analog Input)
P2[4]	I/O	42	Port 2[4] / External AGNDIn
P2[6]	I/O	43	Port 2[6] / External VREFIn
P0[0]	I/O	44	Port 0[0] (Analog Input)
P0[2]	I/O	45	Port 0[2] (Analog Input/Output)
P0[4]	I/O	46	Port 0[4] (Analog Input/Output)
P0[6]	I/O	47	Port 0[6] (Analog Input)
Vcc	Power	48	Supply Voltage

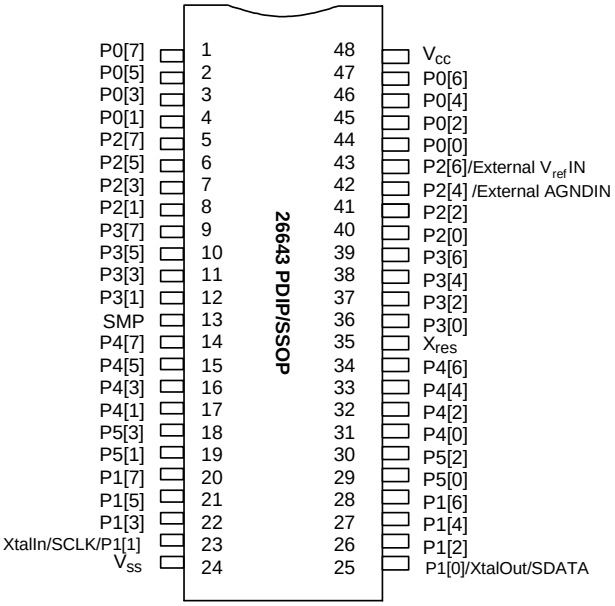

Figure 6: 26643 PDIP/SSOP

Table 45: Digital PSoC Block Interrupt Mask Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	DCA07	DCA06	DCA05	DCA04	DBA03	DBA02	DBA01	DBA00

Bit 7: **DCA07 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 6: **DCA06 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 5: **DCA05 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 4: **DCA04 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 3: **DBA03 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 2: **DBA02 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 1: **DBA01 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 0: **DBA00 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Digital PSoC Block Interrupt Mask Register (INT_MSK1, Address = Bank 0, E1h)

8.5 Interrupt Vector Register

Table 46: Interrupt Vector Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

Bit [7:0]: **Data [7:0]**
8-bit data value holds the interrupt vector for the highest priority pending interrupt. Writing to this register will clear all pending interrupts

Interrupt Vector Register (INT_VC, Address = Bank 0, E2h)

Table 47: Digital Basic Type A/ Communications Type A Block xx Function Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Reserved	End	Mode 1	Mode 0	Function [2]	Function [1]	Function [0]

Bit 7: **Reserved**
Bit 6: **Reserved**

Bit 5: **End**
0 = PSoC block is not the end of a chained function (End should not be set to 0 in block DCA07)
1 = PSoC block is the end of a chained function, or is an unchained PSoC block

Bit 4: **Mode 1** The definition of the Mode [1] bit depends on the block function selected
Timer: The Mode [1] bit signifies the Compare Type
0 = Less Than or Equal
1 = Less Than
Counter: The Mode [1] bit signifies the Compare Type
0 = Less Than or Equal
1 = Less Than
CRC/PRS: The Mode [1] bit is unused in this function
Deadband: The Mode [1] bit is unused in this function
UART: The Mode[1] bit signifies the Interrupt Type (Transmitter only)
0 = Transmit: Interrupt on TX_Reg Empty
1 = Transmit: Interrupt on TX Complete
SPI: The Mode[1] bit signifies the Interrupt Type
0 = Master: Interrupt on TX Reg Empty, Slave: Interrupt on RX Reg Full
1 = Master: Interrupt on SPI Complete, Slave: Interrupt on SPI Complete

Bit 3: **Mode 0** The definition of the Mode [0] bit depends on the block function selected
Timer: The Mode [0] bit signifies Interrupt Type
0 = Terminal Count
1 = Compare True
Counter: The Mode [0] bit signifies Interrupt Type
0 = Terminal Count
1 = Compare True
CRC/PRS: The Mode [0] bit is unused in this function
Deadband: The Mode [0] bit is unused in this function
UART: The Mode [0] bit signifies the Direction
0 = Receive
1 = Transmit
SPI: The Mode [0] bit signifies the Type
0 = Master
1 = Slave

Bit [2:0]: **Function [2:0]** The Function [2:0] bits select the block function which determines the basic hardware configuration
0 0 0 = Timer (chainable)
0 0 1 = Counter (chainable)
0 1 0 = CRC/PRS (Cyclical Redundancy Checker or Pseudo Random Sequencer) (chainable)
0 1 1 = Reserved
1 0 0 = Deadband for Pulse Width Modulator
1 0 1 = UART (function only available on DCA type blocks)
1 1 0 = SPI (function only available on DCA type blocks)
1 1 1 = Reserved

Digital Basic Type A Block 00 Function Register (DBA00FN, Address = Bank 1, 20h)
Digital Basic Type A Block 01 Function Register (DBA01FN, Address = Bank 1, 24h)
Digital Basic Type A Block 02 Function Register (DBA02FN, Address = Bank 1, 28h)
Digital Basic Type A Block 03 Function Register (DBA03FN, Address = Bank 1, 2Ch)
Digital Communications Type A Block 04 Function Register (DCA04FN, Address = Bank 1, 30h)

9.4 Global Inputs and Outputs

Global Inputs and Outputs provide additional capability to route clock and data signals to the digital PSoC blocks. Digital PSoC blocks are connected to the global input and output lines by configuring the PSoC block Input and Output registers (DBA00IN-DCA07IN, DBA00OU-DCA07OU). These global input and output lines form an 8-bit global input bus and an 8-bit global output bus. Four Digital PSoC blocks have access to the upper half of these buses, while the other four access the lower half, per the configuration register. These global input/output buses may be connected to the I/O pins on a per-pin basis using the pin configuration registers. This allows digital PSoC blocks to route their inputs and outputs to pins using the global I/O buses.

9.4.1 Input Assignments

The PSoC block Input Register defines the selection of Global Inputs to digital PSoC blocks. Only 4 of the Global Inputs bus lines are available as selections to a given digital PSoC block as shown in the table below. Once the Global Input has been selected using the PSoC block Input Register selection bits, a GPIO pin must be configured to drive the selected Global Input. This configuration may be set in the Port Global Select Register. The GPIO direction must also be set to input mode by configuring the Port Drive Mode Registers to select High Z.

Table 59: Global Input Assignments

Global Input [7]	Global Input [6]	Global Input [5]	Global Input [4]	Global Input [3]	Global Input [2]	Global Input [1]	Global Input [0]
Port x[7]	Port x[6]	Port x[5]	Port x[4]	Port x[3]	Port x[2]	Port x[1]	Port x[0]
PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03

9.4.2 Output Assignments

The PSoC block Output Register defines the selection of the Global Output bus line to be driven by the digital PSoC blocks. Only 4 of the Global Output bus lines are available as selections to a given digital PSoC block as shown in the table below. The Global Output bus has two functions. Since Global Outputs are also selectable as inputs to digital PSoC blocks, signals can be routed between blocks using this bus. In addition, Global Outputs may drive out to GPIO pins. In this case, once the Global Output has been selected using the PSoC block Output Register selection bits, a GPIO pin must be configured to select the Global Output to drive to the pin. This configuration may be set in the Port Global Select Register. The GPIO direction must also be set to output mode (which is the default) by configuring the Port Drive Mode Registers to one of the available driving strengths.

Table 60: Global Output Assignments

Global Output [7]	Global Output [6]	Global Output [5]	Global Output [4]	Global Output [3]	Global Output [2]	Global Output [1]	Global Output [0]
Port x[7]	Port x[6]	Port x[5]	Port x[4]	Port x[3]	Port x[2]	Port x[1]	Port x[0]
PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 04 PSoC Block 05 PSoC Block 06 PSoC Block 07	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03	PSoC Block 00 PSoC Block 01 PSoC Block 02 PSoC Block 03

9.5 Available Programmed Digital Functionality

9.5.1 Timer with Optional Capture

9.5.1.1 Summary

The timer function continuously measures the amount of time in “ticks” between two events, and provides a rate generator. A down counter lies at the heart of the timer functions. Rate generators divide their clock source by an integer value. Hardware or software generated events

4. Capture vs. Compare

   A capture event will overwrite Data Register 2. This is also the register that holds the compare value. Therefore, using the capture function may not be compatible with using the timer compare function.

9.5.2 Counter with Optional Compare (Pulse-Width) Output

9.5.2.1 Summary

Conceptually, a counter measures the number of events between “ticks,” however, this distinction between counter and timer blurs because both functions provide a complete range of clock selections. The counter trades the timer’s hardware capture for a clock gate or ”enable” and provides a means of adjusting the duty cycle of its output so that it can double as a pulse-width modulator. A down counter lies at the heart of the counter function. Counter-configured PSoC blocks may be chained to arbitrary lengths in 8 bit increments.

In a Counter User Module, the data input is an enable for counting. Normally, when the enable goes low, the counter will hold the current count. However, if the enable happens to go low in the same clock period as Terminal Count (count of all 0's), one additional count will occur that will reload the counter from the Period Register. Once the counter is reloaded from the Period Register, counting will stop.

9.5.2.2 Registers

Data Register 1 establishes the period of the counter. Data Register 0 holds the current state of the down counter. If the function is disabled, writing a period into Data Register 1, will automatically load Data Register 0. It is also automatically reloaded on the clock cycle after it reaches zero, the terminal count value. The value in Data Register 2 (compare value) is continually compared to Data Register 0 (count value) to establish the output pulse-width (duty cycle). Reading Data Register 0 to obtain the current value of the down counter may occur only when the function is disabled. When read, this transfers the value from Data Register 0 to Data Register 2 and returns a 0 on the data bus. The value transferred to Data Register 2 can then be directly read by the CPU. However, reading the count value in this manner will overwrite any previously written compare value in Data Register 2. Control Register 0 contains one bit to enable/disable the function.

9.5.2.3 Inputs

There are two primary inputs, the Source Clock and the Enable signal. When the Enable signal is high, the down counter is decremented on the rising-edge of the Source Clock. The multiplexers selecting these inputs are controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.2.4 Outputs

The counter function drives its primary output signal, Compare True, high on the falling edge of the Source Clock when the value in Data Register 0 is less (or less than or equal to) the value in Data Register 2. The duty cycle of the pulse-width modulator formed in this way is the ratio of Data Register 2 (or Data Register 2 minus one) to Data Register 1. The choice of compare operators is determined by the MODE[1] bit. The Compare value can be routed to additional analog or digital PSoC blocks or via Global Output lines The auxiliary output signal is the Terminal Count signal which can be routed via Global Output lines. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.2.5 Interrupts

Interrupts may be generated in either of two ways. First, the PSoC block may optionally generate an interrupt on the rising edge of Terminal Count or the rising edge of the Compare signal. The selection of interrupt source is determined by the MODE[0] bit of the PSoC block Function Register (DBA00FN-DCA07FN). The MODE[1] bit controls whether the comparison operation is “less than” or “less than or equal to.”

9.5.2.6 Usage Notes

1. Enable Input

   The enable input is synchronous and when low forces the counter into a ‘hold’ state. Outputs are unaffected by the state of the enable input. If an external source is selected as the enable input, it is synchronized to the 24 MHz clock.

except for TX Reg Empty. TX Reg Empty is automatically cleared when a byte is written to the TX Data Register (Data Register 1).

3. Using CPU Interrupts

   TX Reg Empty status or optionally TX Complete status generates the block interrupt. Executing the interrupt routine does not automatically clear status. If TX Complete is selected as the interrupt source, Control Register 0 (status) must be read in the interrupt routine to clear the status. If TX Reg Empty is selected, a byte must be written to the TX Data Register (Data Register 1) to clear the status. If the status is not cleared, further interrupts will be suppressed.

9.5.8 SPI Master - Serial Peripheral Interface (SPIM)

9.5.8.1 Summary

The SPI Master function provides a full-duplex synchronous data transceiver that also generates a bit clock for the data. This function requires a Digital Communications Type PSoC block. It cannot be chained for longer data words. This Digital Communications Type PSoC block supports SPI modes for 0, 1, 2, and 3. See Figure 15: for waveforms of the Clock Phase modes.

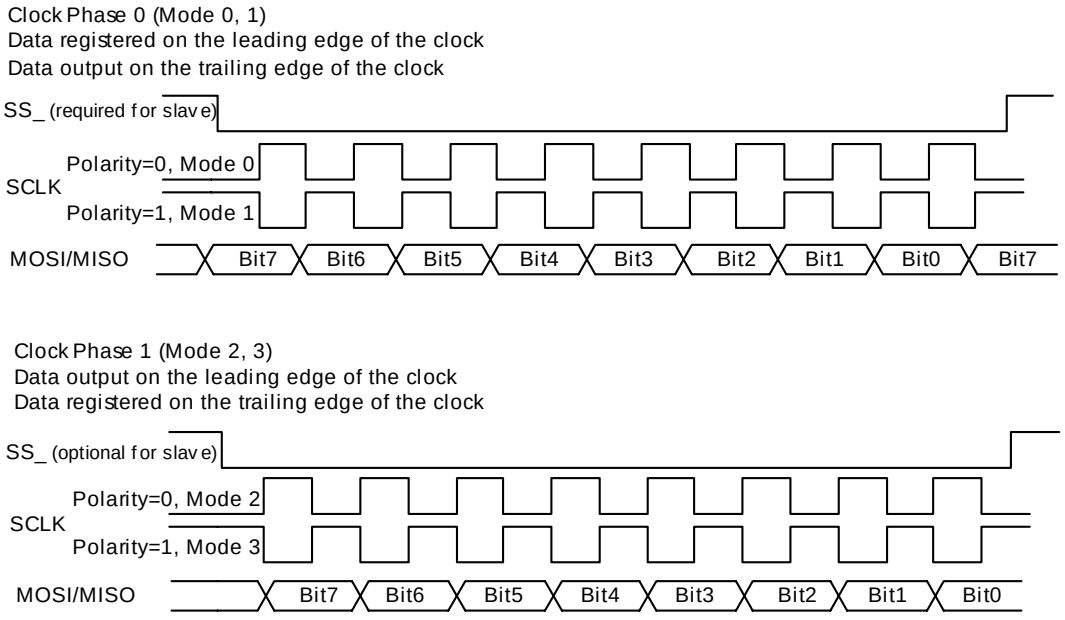

Figure 15: SPI Waveforms

9.5.8.2 Registers

Data Register 0 provides a shift register for both incoming and outgoing data. Output data is written to Data Register 1 (TX Data Register). When this block is idle, a write to the TX Data Register will initiate a transmission. Input data is read from Data Register 2 (RX Data Register). When Data Register 0 is empty, its value is updated from Data Register 1, if new data is available. As data bits are shifted in, the transmit bits are shifted out. After the 8 bits are transmitted and received by Data Register 0, the received byte is transferred into Data Register 2 from where it can be read. Simultaneously, the next byte to transmit, if available, is transferred from Data Register 1 into Data Register 0. Control Register 0 (DCA04CR0-DCA07CR0) provides status information and configures the function for one of the four standard modes, which configure the interface based on clock polarity and phase with respect to data.

divided into distinct bit fields. Some bit fields set the PSoC block's resistor ratios or capacitor values. Others configure switches and multiplexers that form connections between internal block nodes. Additionally, a block may be connected via local interconnection resources to neighboring analog PSoC blocks, reference voltage sources, input multiplexers and output busses. Specific advantages and applications of each type are treated separately below.

10.6.1 Local Interconnect

Analog continuous-time PSoC blocks occupy the top row, (row 0) of the analog array. Designated ACA for analog continuous-time subtype "A," each connects to its neighbors by means of three multiplexers. (Note that unlike the switched capacitor blocks, the continuous time blocks in the current family of parts only have one subtype.) The three are the non-inverting input multiplexer, "PMux," the inverting input multiplexer, "NMux," and the "RBotMux" which controls the node at the bottom of the resistor string. The bit fields, which control these multiplexers, are named PMux, NMux, and RBotMux, respectively. The following diagrams show how each multiplexer connects its ACA block connect to its neighbors. Each arrow points from an input source, either a PSoC block, bus or reference voltage to the block where it is used. Each arrow is labeled with the value to which the bit-field must be set to select that input source.

10.6.1.1 NMux

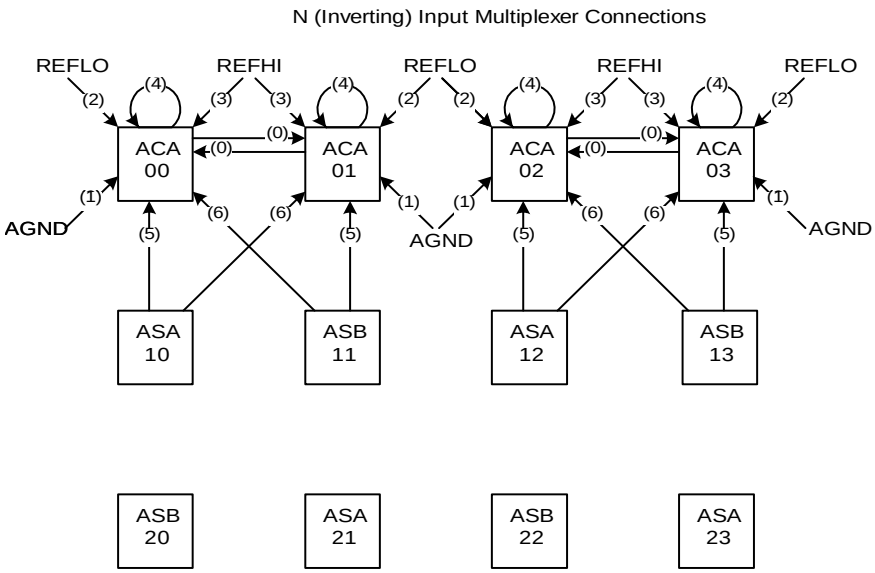

Figure 18: NMux Connections

10.6.1.2 PMux

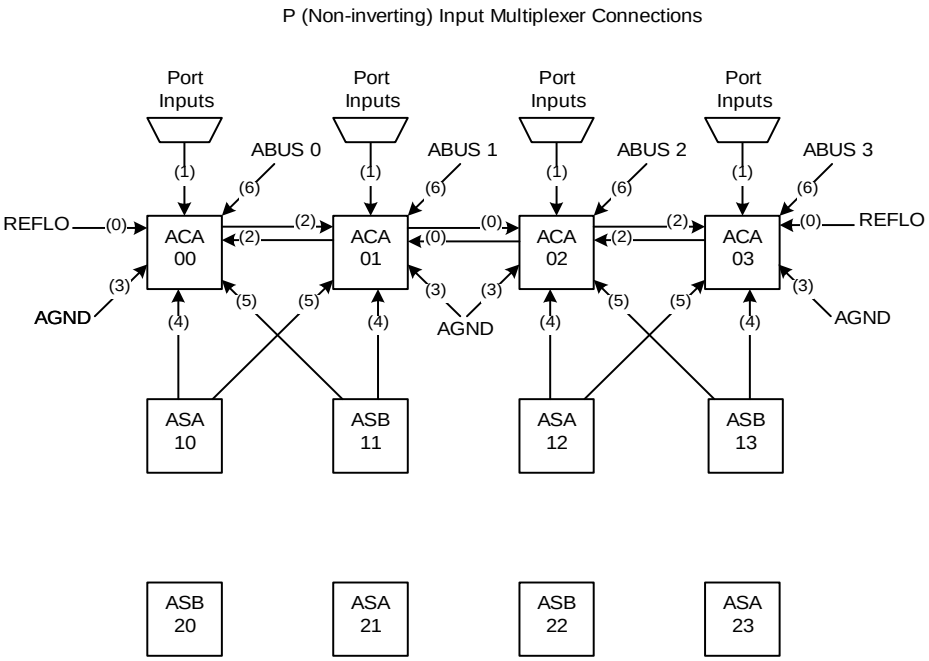

Figure 19: PMux Connections

10.6.1.3 RBotMux

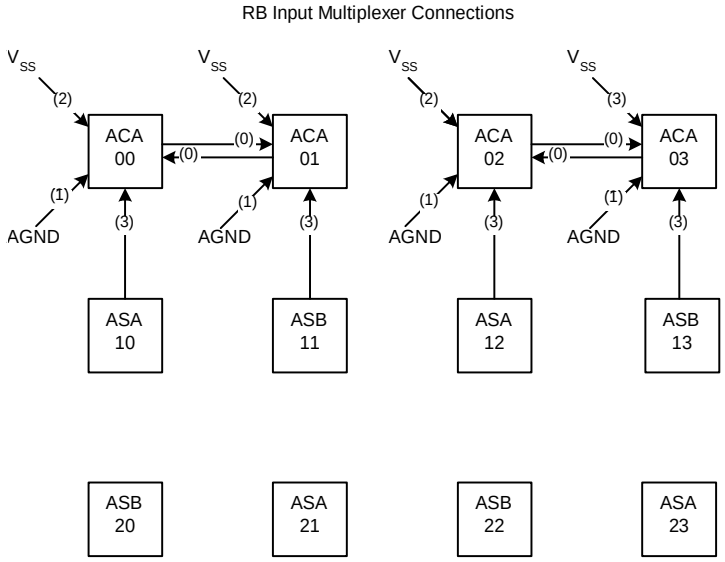

Figure 20: RBotMux Connections

Table 69: Analog Switch Cap Type A Block xx Control 0 Register, continued

Bit 7: **FCap** F Capacitor value selection bit
0 = 16 capacitor units
1 = 32 capacitor units

Bit 6: **ClockPhase** Clock phase select, will invert clocks internal to the blocks. During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2)

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Select Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s

0 = Internal PHI1 = External PHI1
1 = Internal PHI1 = External PHI2

This bit also affects the latching of the comparator output (CBUS). Both clock phases, PHI1 and PHI2, are involved in the output latching mechanism. The capture of the next value to be output from the latch (capture point event) happens during the falling edge of one clock phase, and the rising edge of the other clock phase will cause the value to come out (output point event). This bit determines which clock phase triggers the capture point event, and the other clock will trigger the output point event. The value output to the comparator bus will remain stable between output point events.

0 = Capture Point Event triggered by Falling PHI2, Output Point Event triggered by Rising PHI1
1 = Capture Point Event triggered by Falling PHI1, Output Point Event triggered by Rising PHI2

Bit 5: **ASign**
0 = Input sampled on Internal PHI1, Reference Input sampled on internal PHI2
1 = Input sampled on Internal PHI2, Reference Input sampled on internal PHI1

Bit [4:0]: **ACap [4:0]** Binary encoding for 32 possible capacitor sizes for A Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type A Block 10 Control 0 Register (ASA10CR0, Address = Bank 0/1, 80h)
Analog Switch Cap Type A Block 12 Control 0 Register (ASA12CR0, Address = Bank 0/1, 88h)
Analog Switch Cap Type A Block 21 Control 0 Register (ASA21CR0, Address = Bank 0/1, 94h)
Analog Switch Cap Type A Block 23 Control 0 Register (ASA23CR0, Address = Bank 0/1, 9Ch)

10.8.3.4 Analog Switch Cap Type A Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASA10CR2, ASA12CR2, ASA21CR2, ASA23CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BMuxSCA controls the muxing to the input of the B capacitor branch.

Power – encoding for selecting 1 of 4 power levels. The block always powers up in the off state.

Table 72: Analog Switch Cap Type A Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BMuxSCA[1]	BMuxSCA[0]	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
1 = If the FSW1 bit is set to 1, the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit [3:2] BMuxSCA [1:0] Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block.)

ASA10	ASA21	ASA12	ASA23
0 0 = ACA00	ASB11	ACA02	ASB13
0 1 = ASB11	ASB20	ASB13	ASB22
1 0 = P2.3	ASB22	ASB11	P2.0
1 1 = ASB20	T_{ref}GND	ASB22	ABUS3

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type A Block 10 Control 3 Register (ASA10CR3, Address = Bank 0/1, 83h)
Analog Switch Cap Type A Block 12 Control 3 Register (ASA12CR3, Address = Bank 0/1, 8Bh)
Analog Switch Cap Type A Block 21 Control 3 Register (ASA21CR3, Address = Bank 0/1, 97h)
Analog Switch Cap Type A Block 23 Control 3 Register (ASA23CR3, Address = Bank 0/1, 9Fh)

The SAR hardware accelerator is a block of specialized hardware designed to sequence the SAR algorithm for efficient A/D conversion. A SAR ADC is implemented conceptually with a DAC of the desired precision, and a comparator. This functionality can be configured from one or more PSoC blocks. For each conversion, the firmware should initialize the ASY_CR register as defined below, and set the sign bit of the DAC as the first guess in the algorithm. A sequence of OR instructions (Read, Modify, Write) to the DAC (CR0) register is then executed. Each of these OR instructions causes the SAR hardware to read the current state of the comparator, checking the validity of the previous guess. It either clears it or leaves it set, accordingly. The next LSB in the DAC register is also set as the next guess. Six OR instructions will complete the conversion of a 6-bit DAC. The resulting DAC code, which matches the input voltage to within 1 LSB, is then read back from the DAC CR0 register.

10.11.1 Analog Stall and Analog Stall Lockup

Stall lockup affects the operation of stalled IO writes, such as DAC writes and the stalled IOR of the SAR hardware accelerator. The DAC and SAR User Modules operate in this mode. The analog column clock frequency must not be a power of two multiple (2, 4, 8...) higher than the CPU clock frequency. Under this condition, the CPU will never recover from a stall.

See the list of relationships (in MHz) that will fail:

Table 78: Analog Frequency Relationships

Analog Column Clock	CPU Clock
3.	1.5, 0.75, .018, 0.093
1.5	0.75, 0.18, 0.093
0.75	0.18, 0.093
0.37	0.18, 0.093
0.18	0.093

You can still run the CPU clock slower than the column clock if the relationship is not a power of two multiple. For example, you can run at 0.6 MHz, which is not a power of two multiple of any CPU frequency and therefore any CPU frequency can be selected. If the CPU frequency is greater than or equal to the analog column clock, there is not a problem.

Table 79: Analog Synchronization Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	--	W	W	W	RW	RW	RW	RW
Bit Name	Reserved	SARCOUNT [2]	SARCOUNT [1]	SARCOUNT [0]	SAR-SIGN	SARCOL [1]	SARCOL [0]	SYN-CEN

Bit 7: **Reserved**

Bit [6:4]: **SARCOUNT [2:0]** Initial SAR count. Load this field with the number of bits to process. In a typical 6-bit SAR, the value would be 6

Bit 3: **SARSIGN** Adjust the SAR comparator based on the type of block addressed. In a DAC configuration with more than one PSoC block (more than 6-bits), this bit would be 0 when processing the most significant block and 1 when processing the least significant block. This is because the least significant block of a DAC is an inverting input to the most significant block

Bit [2:1]: **SARCOL [1:0]** Column select for SAR comparator input. The DAC portion of the SAR can reside in any of the appropriate positions in the analog PSOC block array. However, once the comparator block is positioned (and it is possible to have the DAC and comparator in the same block), this should be the column selected

Bit 0: **SYNCEN** Set to 1, will stall the CPU until the rising edge of PHI1, if a write to a register within an analog Switch Cap block takes place

Analog Synchronization Control Register (ASY_CR, Address = Bank 0, 65h)

Table 85: Multiply Result High Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value is the high order result of the multiply function

Multiply Result High Register (MUL_DH, Address = Bank 0, EAh)

Table 86: Multiply Result Low Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value is the low order result of the multiply function

Multiply Result Low Register (MUL_DL, Address = Bank 0, EBh)

Table 87: Accumulator Result 1 / Multiply/Accumulator Input X Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the next to lowest order result of the multiply/accumulate function
8-bit data value when written is the X multiplier input to the multiply/accumulate function

Accumulator Result 1 / Multiply/Accumulator Input X Register (ACC_DR1 / MAC_X, Address = Bank 0, ECh)

Table 88: Accumulator Result 0 / Multiply/Accumulator Input Y Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the lowest order result of the multiply/accumulate function
8-bit data value when written is the Y multiplier input to the multiply/accumulate function

Accumulator Result 0 / Multiply/Accumulator Input Y Register (ACC_DR0 / MAC_Y, Address = Bank 0, EDh)

11.8.1 Additional Function for Table Read Supervisory Call

The Table Read supervisory operation will return the Version ID in the Accumulator. The value in the Accumulator is divided into a high and low nibble, indicating major and minor revisions, respectively. **Note**: The value in the X register is modified during the Table Read Supervisory Call, and must be saved and restored if needed after the call completes.

- A[7:4]: Major silicon revisions.
- A[3:0]: Minor silicon revisions.

Table 99: Table Read for Supervisory Call Functions

Table ID	Function	TV(0)	TV(1)	TV(2)	TV(3)	TV(4)	TV(5)	TV(6)	TV(7)
00[1]	Production Silicon ID	Silicon ID 1	Silicon ID 0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01	Provides trim value for Internal Main Oscillator and Internal Voltage Reference	Internal Voltage Reference trim value for 3.3V	Internal Main Oscillator trim value for 3.3V	Reserved	Reserved	Internal Voltage Reference trim value for 5.0V	Internal Main Oscillator trim value for 5.0V	Reserved	Reserved

1. Determines silicon revision values in Accumulator and X registers.

11.9 Flash Program Memory Protection

The user has the option to define the access to the Flash memory. A flexible system allows the user to select one of four protection modes for each 64-byte block within the Flash, based on the particular application. The protection mechanism is implemented by a device programmer using the System Supervisor Call. When this command is executed, two bits within the data programmed into the Flash will select the protection mode. It is not intended that the protection byte will be modified by the user's code. The following table lists the available protection options:

Table 100: Flash Program Memory Protection

Mode Bits	Mode Name	External Read	External Write	Internal Write
00	Unprotected	Enabled	Enabled	Enabled
01	Factory Upgrade	Disabled	Enabled	Enabled
10	Field Upgrade	Disabled	Disabled	Enabled
11	Full Protection	Disabled	Disabled	Disabled

Note: Mode 10 is the default.

11.10 Programming Requirements and Step Descriptions

The pins in the following table are critical for the programmer:

Table 101: Programmer Requirements

Pin Name	Function	Programmer HW Pin Requirements
SDATA	Serial Data In/Out	Drive TTL Levels, Read TTL, High Z
SCLK	Serial Clock	Drive TTL levEl Clock Signal
V_{ss}	Power Supply Ground Connection	Low Resistance Ground Connection
V_{cc}	Power Supply Positive Voltage	0V, 3.0V, 5V, & 5.4V. 0.1V Accuracy. 20mA Current Capability

11.10.2.6 Device Checksum (at Low Vcc and High Vcc)

The device checksum is retrieved from the device and compared to the “Device Checksum” from the user’s file (Note that this is NOT the same thing as the “Record Checksum.”) The checksum is retrieved from the device with the following sequence:

```
CHECKSUM-SETUP(max_data_block)
WAIT-AND-POLL
READ-CHECKSUM(data)
```

Note: This should be done 2 times; once at Vcc=Vcchv and once at Vcc=Vcclv.

11.10.2.7 Power Down

The last step is to power down the device. This is accomplished by the following sequence:

```
Set SDATA=HighZ (float pin P1[0])
Set SCLK=0V (Vin on pin P1[1]=Vilp)
Set Vcc = 0V
```

11.11 Programming Wave Forms

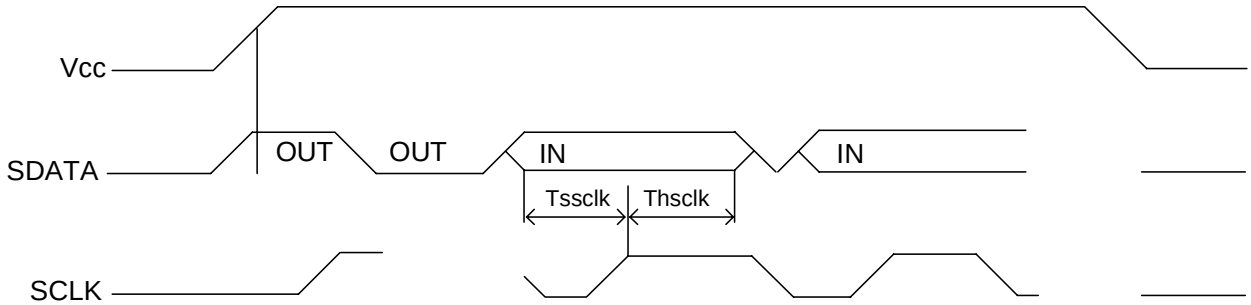

Figure 34: Programming Wave Forms

Notes:

1. Vcc is only turned off (0V) at the very beginning and the very end of the flow - not within the programming flow.
2. When the programmer puts the driver on SDATA in a High Z (floating) state, the SDATA pin will float to a low due to an internal device pull down circuit.
3. SCLK is set to VILP during the power up and power down; at other times the SCLK is “free running.” The frequency of the hardware’s SCLK signal must be known by the software because the value (entered in the number of MegaHertz multiplied by the number 5) must be passed into the device with the SET-CLK-FREQ() mnemonic.

11.12 Programming File Format

The programming file is created by PSoC Designer, the Cypress MicroSystems development tool. This tool generates the programming file in an Intel Hex format.

The programmer should assume the data is 30h/HALT if it is not specified in the user’s data file.

13.2.1.2 3.3V Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 3.3V +/- 10% and -40°C <= T_A <= 85°C. The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switch Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only. For 5V operation, see Table 105 on page 130.

Table 106: 3.3V DC Operational Amplifier Specifications

Symbol	3.3V DC Operational Amplifier Specifications	Minimum	Typical	Maximum	Unit
	Input Offset Voltage (Absolute Value)	-	7	30	mV
	Average Input Offset Voltage Drift	-	+24	-	µV/°C
	Input Leakage Current[1]	-	2	700	nA
	Input Capacitance[2]	.32	.36	.42	pF
	Common Mode Voltage Range[3]	.5	-	V_{cc} - 1.0	VDC
	Common Mode Rejection Ratio	80	-	-	dB
	Open Loop Gain	80	-	-	dB
	High Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 V_{cc} - .4 V_{cc} - .4 V_{cc} - .4	 - - -	 - - -	 V V V
	Low Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 - - -	 - - -	 0.1 0.1 0.1	 V V V
	Supply Current (Including Associated AGND Buffer) Bias = Low Bias = Medium Bias = High	 - - -	 80 112 320	 200 300 800	 µA µA µA
	Supply Voltage Rejection Ratio	60	-	-	dB

1. The leakage current includes the Analog Continuous Time PSoC block mux and the analog input mux. The leakage related to the General Purpose I/O pins is not included here.
2. The Input Capacitance includes the Analog Continuous Time PSoC block mux and the analog input mux. The capacitance of the General Purpose I/O pins is not included here.
3. The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer

Table 113: 3.3V DC Analog Reference Specifications

Symbol	3.3V DC Analog Reference Specifications	Minimum	Typical	Maximum	Unit
	AGND = Vcc/2 [1] CT Block Bias = High	Vcc/2 - 0.007	Vcc/2 - 0.003	Vcc/2 + 0.002	V
	AGND = 2*BandGap[1] CT Block Bias = High	Not Allowed			
	AGND = P2[4] (P2[4] = Vcc/2) CT Block Bias = High	P24 - 0.008	P24 + 0.001	P24 + 0.009	V
	AGND Column to Column Variation (AGND=Vcc/2)[1] CT Block Bias = High	-0.034	0.000	0.034	mV
	REFHI = Vcc/2 + BandGap Ref Control Bias = High	Not Allowed			
	REFHI = 3*BandGap Ref Control Bias = High	Not Allowed			
	REFHI = 2*BandGap + P2[6] (P2[6] = 0.5V) Ref Control Bias = High	Not Allowed			
	REFHI = P2[4] + BandGap (P2[4] = Vcc/2) Ref Control Bias = High	Not Allowed			
	REFHI = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V) Ref Control Bias = High	P2[4]+P2[6] - 0.075	P2[4]+P2[6] - 0.009	P2[4]+P2[6]+ 0.057	V
	REFLO = Vcc/2 - BandGap Ref Control Bias = High	Not Allowed			
	REFLO = BandGap Ref Control Bias = High	Not Allowed			
	REFLO = 2*BandGap - P2[6] (P2[6] = 0.5V) Ref Control Bias = High	Not Allowed			
	REFLO = P2[4] – BandGap (P2[4] = Vcc/2) Ref Control Bias = High	Not Allowed			
	REFLO = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V) Ref Control Bias = High	P2[4]-P2[6] - 0.048	P24-P26 + 0.022	P2[4]-P2[6] + 0.092	V

1. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

13.2.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications include both voltage ranges, 5V +/- 5% and 3.3V +/- 10% and the temperature range -40°C <= T_A <= 85°C. Typical parameters apply to 3.3V and 5V at 25°C and are for design guidance only.

Table 114: DC Analog PSoC Block Specifications

Symbol	DC Analog PSoC Block Specifications	Minimum	Typical	Maximum	Unit
	Resistor Unit Value (Continuous Time)	-	45	-	kΩ
	Capacitor Unit Value (Switch Cap)	-	70	-	fF

13.3.2 AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and –40°C <= T_A <= 85°C. Typical parameters are provided for design guidance only. Typical parameters apply to 5V and 25°C. For 3.3V operation, see Table 120 on page 142.

Table 119: 5V AC Analog Output Buffer Specifications

Symbol	5V AC Analog Output Buffer Specifications	Minimum	Typical	Maximum	Unit
	Rising Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.5	µs
	Bias = High	-	-	2.5	µs
	Falling Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.2	µs
	Bias = High	-	-	2.2	µs
	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load				
	Bias = Low	.9	-	-	V/µs
	Bias = High	.9	-	-	V/µs
	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load				
	Bias = Low	.9	-	-	V/µs
	Bias = High	.9	-	-	V/µs
	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load				
	Bias = Low	1.5	-	-	MHz
	Bias = High	1.5	-	-	MHz
	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load				
	Bias = Low	600	-	-	kHz
	Bias = High	600	-	-	kHz

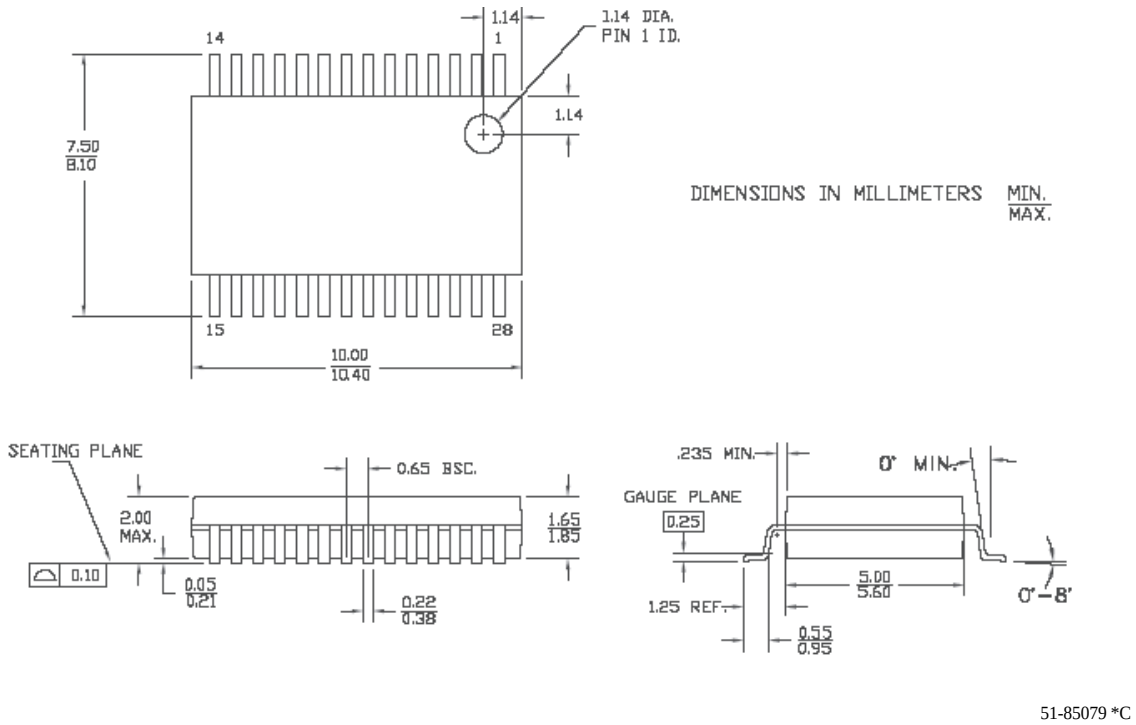

Figure 39: 28-Lead (210-Mil) Shrunk Small Outline Package O28

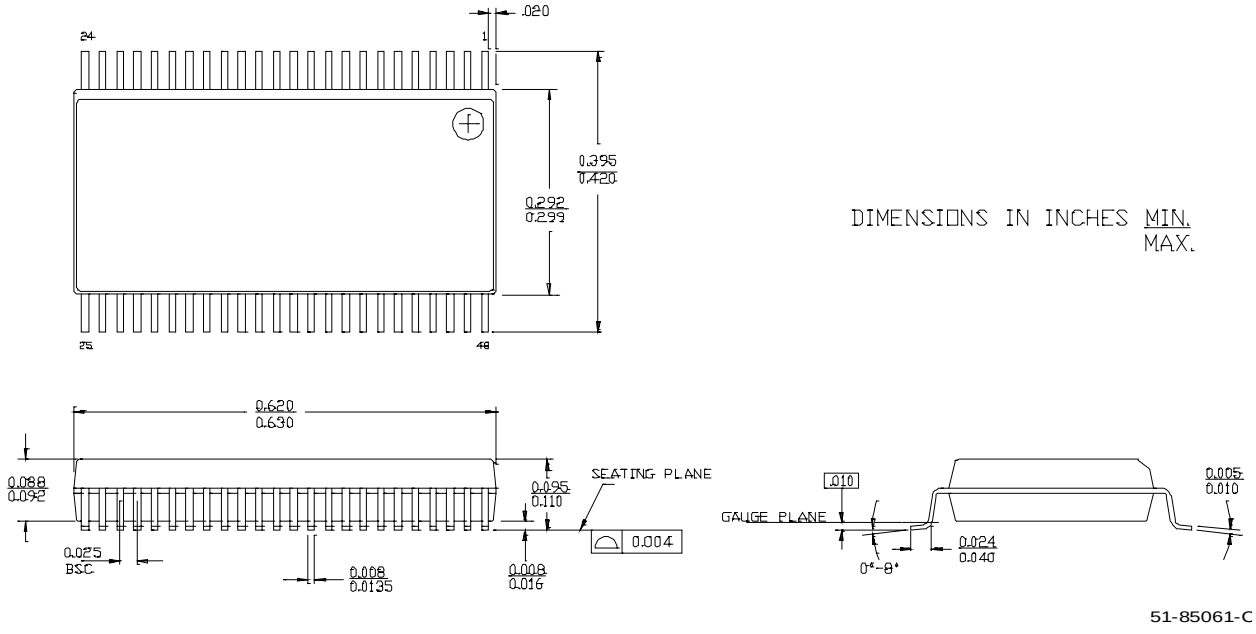

Figure 40: 48-Lead Shrunk Small Outline Package O48

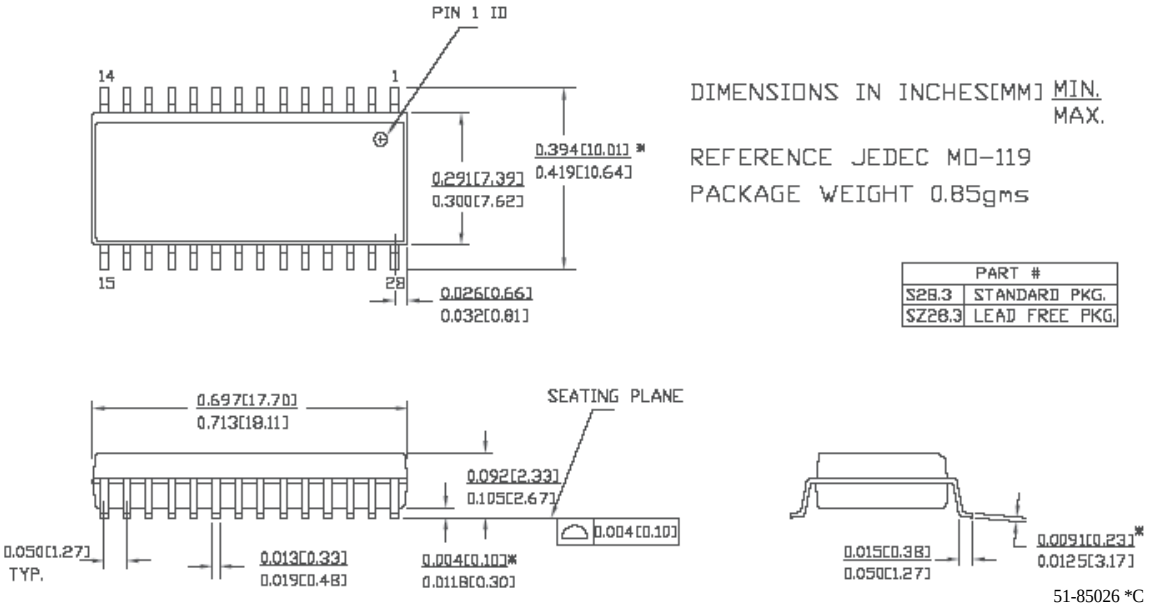

Figure 45: 28-Lead (300-Mil) Molded SOIC S21

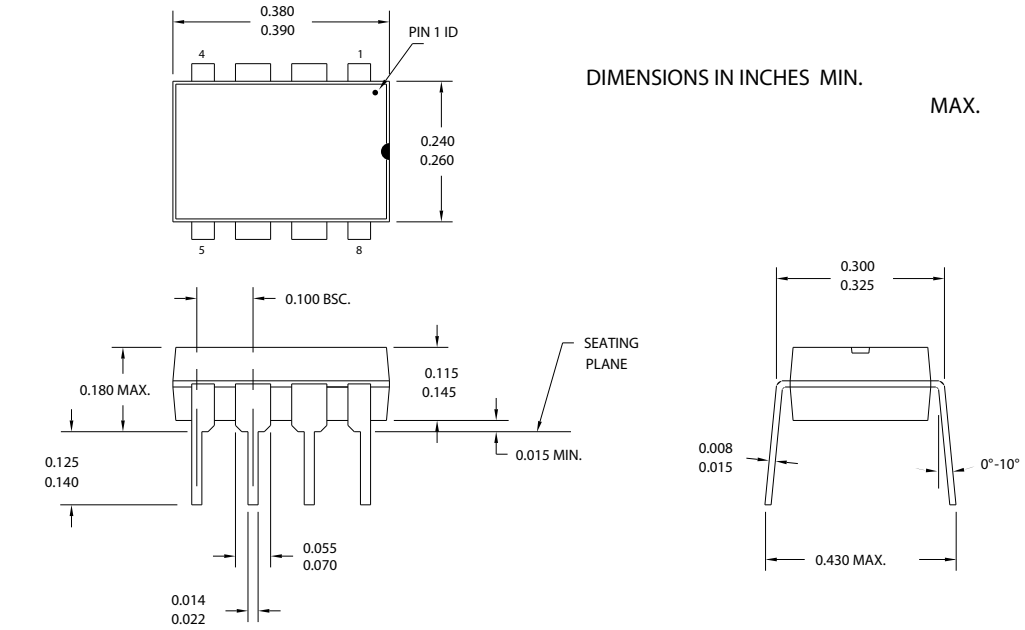

Figure 46: 8-Lead (300-Mil) Molded DIP