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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26233-24pvit

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1.2 Pin-out Descriptions

Table 2: Pin-out 8 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P1[1]	I/O	3	Port 1[1] / XtalIn / SCLK
Vss	Power	4	Ground
P1[0]	I/O	5	Port 1[0] / XtalOut / SDATA
P0[2]	I/O	6	Port 0[2] (Analog Input/Output)
P0[4]	I/O	7	Port 0[4] (Analog Input/Output)
Vcc	Power	8	Supply Voltage

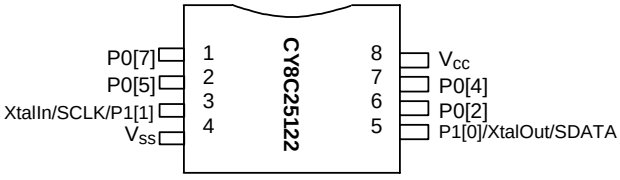

Figure 2: CY8C25122

Table 3: Pin-out 20 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
SMP	O	5	Switch Mode Pump
P1[7]	I/O	6	Port 1[7]
P1[5]	I/O	7	Port 1[5]
P1[3]	I/O	8	Port 1[3]
P1[1]	I/O	9	Port 1[1] / XtalIn / SCLK
Vss	Power	10	Ground
P1[0]	I/O	11	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	12	Port 1[2]
P1[4]	I/O	13	Port 1[4]
P1[6]	I/O	14	Port 1[6]
XRES	I	15	External Reset
P0[0]	I/O	16	Port 0[0] (Analog Input)
P0[2]	I/O	17	Port 0[2] (Analog Input/Output)
P0[4]	I/O	18	Port 0[4] (Analog Input/Output)
P0[6]	I/O	19	Port 0[6] (Analog Input)
Vcc	Power	20	Supply Voltage

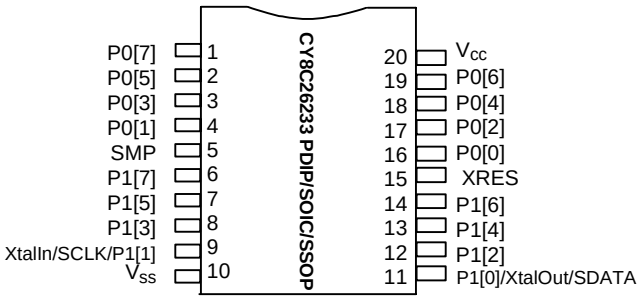

Figure 3: CY8C26233

Table 5: Pin-out 44 Pin, continued

P4[6]	I/O	25	Port 4[6]
XRES	I	26	External Reset
P3[0]	I/O	27	Port 3[0]
P3[2]	I/O	28	Port 3[2]
P3[4]	I/O	29	Port 3[4]
P3[6]	I/O	30	Port 3[6]
P2[0]	I/O	31	Port 2[0] (Non-Multiplexed Analog Input)
P2[2]	I/O	32	Port 2[2] (Non-Multiplexed Analog Input)
P2[4]	I/O	33	Port 2[4] / External AGNDIn
P2[6]	I/O	34	Port 2[6] / External VREFIn
P0[0]	I/O	35	Port 0[0] (Analog Input)
P0[2]	I/O	36	Port 0[2] (Analog Input/Output)
P0[4]	I/O	37	Port 0[4] (Analog Input/Output)
P0[6]	I/O	38	Port 0[6] (Analog Input)
Vcc	Power	39	Supply Voltage
P0[7]	I/O	40	Port 0[7] (Analog Input)
P0[5]	I/O	41	Port 0[5] (Analog Input/Output)
P0[3]	I/O	42	Port 0[3] (Analog Input/Output)
P0[1]	I/O	43	Port 0[1] (Analog Input)
P2[7]	I/O	44	Port 2[7]

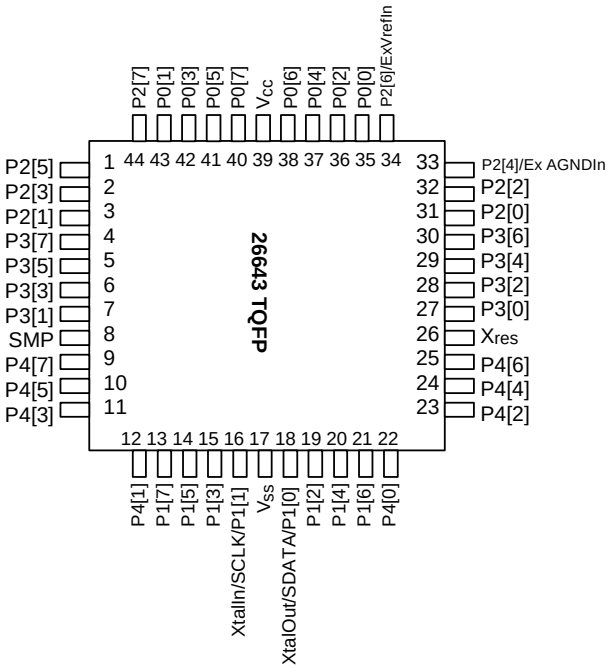

Figure 5: 26643 TQFP

Table 6: Pin-out 48 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
P2[7]	I/O	5	Port 2[7]
P2[5]	I/O	6	Port 2[5]
P2[3]	I/O	7	Port 2[3] (Non-Multiplexed Analog Input)
P2[1]	I/O	8	Port 2[1] (Non-Multiplexed Analog Input)
P3[7]	I/O	9	Port 3[7]
P3[5]	I/O	10	Port 3[5]
P3[3]	I/O	11	Port 3[3]
P3[1]	I/O	12	Port 3[1]
SMP	O	13	Switch Mode Pump
P4[7]	I/O	14	Port 4[7]
P4[5]	I/O	15	Port 4[5]
P4[3]	I/O	16	Port 4[3]
P4[1]	I/O	17	Port 4[1]
P5[3]	I/O	18	Port 5[3]
P5[1]	I/O	19	Port 5[1]
P1[7]	I/O	20	Port 1[7]
P1[5]	I/O	21	Port 1[5]
P1[3]	I/O	22	Port 1[3]
P1[1]	I/O	23	Port 1[1] / XtalIn / SCLK
Vss	Power	24	Ground
P1[0]	I/O	25	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	26	Port 1[2]
P1[4]	I/O	27	Port 1[4]
P1[6]	I/O	28	Port 1[6]

8.2 Interrupt Control Architecture

The interrupt controller contains a separate flip-flop for each interrupt. When an interrupt is generated, it is registered as a pending interrupt. It will stay pending until it is serviced, a reset occurs, or there is a write to the INT_VC Register. A pending interrupt will only generate an interrupt request when enabled by the appropriate mask bit in the Digital PSoC Block Interrupt Mask Register (INT_MSK1) or General Interrupt Mask Register (INT_MSK0), and the Global IE bit in the CPU_F register is set.

Additionally, for GPIO Interrupts, the appropriate enable and interrupt-type bits for each I/O pin must be set (see section 6.0, Table 29 on page 31, Table 33 on page 33, and Table 34 on page 34). For Analog Column Interrupts, the interrupt source must be set (see section 10.10 and Table 77 on page 101).

During the servicing of any interrupt, the MSB and LSB of Program Counter and Flag registers (CPU_PC and CPU_F) are stored onto the program stack by an automatic `CALL` instruction (13 cycles) generated during the interrupt acknowledge process. The user firmware may preserve and restore processor state during an interrupt using the `PUSH` and `POP` instructions. The memory oriented CPU architecture requires minimal state saving during interrupts, providing very fast interrupt context switching. The Program Counter and Flag registers (CPU_PC and CPU_F) are restored when the `RETI` instruction is executed. If two or more interrupts are pending at the same time, the higher priority interrupt (lower priority number) will be serviced first.

After a copy of the Flag Register is stored on the stack, the Flag Register is automatically cleared. This disables all interrupts, since the Global IE flag bit is now cleared. Executing a `RETI` instruction restores the Flag register, and re-enables the Global Interrupt bit.

Nested interrupts can be accomplished by re-enabling interrupts inside an interrupt service routine. To do this, set the IE bit in the Flag Register. The user must store sufficient information to maintain machine state if this is done.

Each digital PSoC block has its own unique Interrupt Vector and Interrupt Enable bit. There are also individual interrupt vectors for each of the Analog columns, Supply Voltage Monitor, Sleep Timer and General Purpose I/Os.

8.3 Interrupt Vectors

Table 43: Interrupt Vector Table

Address	Interrupt Priority Number	Description
0x0004	1	Supply Monitor Interrupt Vector
0x0008	2	DBA00 PSoC Block Interrupt Vector
0x000C	3	DBA01 PSoC Block Interrupt Vector
0x0010	4	DBA02 PSoC Block Interrupt Vector
0x0014	5	DBA03 PSoC Block Interrupt Vector
0x0018	6	DCA04 PSoC Block Interrupt Vector
0x001C	7	DCA05 PSoC Block Interrupt Vector
0x0020	8	DCA06 PSoC Block Interrupt Vector
0x0024	9	DCA07 PSoC Block Interrupt Vector
0x0028	10	Acolumn 0 Interrupt Vector
0x002C	11	Acolumn 1 Interrupt Vector
0x0030	12	Acolumn 2 Interrupt Vector
0x0034	13	Acolumn 3 Interrupt Vector
0x0038	14	GPIO Interrupt Vector
0x003C	15	Sleep Timer Interrupt Vector
0x0040		On-Chip Program Memory Starts

The interrupt process vectors the Program Counter to the appropriate address in the Interrupt Vector Table. Typically, these addresses contain `JMP` instructions to the start of the interrupt handling routine for the interrupt.

9.3.5 Digital Communications Type A Block xx Control Register 0 When Used as UART Receiver

Table 57: Digital Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bit Name	Parity Error	Overrun	Framing Error	RX Active	RX Reg Full	Parity Type	Parity Enable	Enable

Bit 7: **Parity Error**
0 = Indicates no parity error detected in the last byte received
1 = Indicates a parity error detected in the last byte received
Reset when this register is read

Bit 6: **Overrun**
0 = Indicates that no overrun has taken place
1 = Indicates the RX Data register was overwritten with a new byte before the previous one had been read
Reset when this register is read

Bit 5: **Framing Error**
0 = Indicates correct stop bit
1 = Indicates a missing STOP bit
Reset when this register is read

Bit 4: **RX Active**
0 = Indicates no communication currently in progress
1 = Indicates a start bit has been received and a byte is currently being received

Bit 3: **RX Reg Full**
0 = Indicates the RX Data register is empty
1 = Indicates a byte has been loaded into the RX Data register
Interrupt source for RXUART. Reset when the RX Data register is read (Data Register 2)

Bit 2: **Parity Type**
0 = Even
1 = Odd

Bit 1: **Parity Enable**
0 = Parity Disabled
1 = Parity Enabled

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

10.5 Analog PSoC Block Clocking Options

All analog PSoC blocks in a particular Analog Column share the same clock signal. Choosing the clocking for an analog PSoC block is a two-step process.

1. First, if the user wants to use the **ACLK0** and **ACLK1** system-clocking signals, the digital PSoC blocks that serve as the source for these signals must be selected. This selection is made in the Analog Clock Select Register (CLK_CR1).
2. Next, the user must select the source for the **Acolumn0**, **Acolumn1**, **Acolumn2**, and **Acolumn3** system-clocking signals. The user will choose the clock for Acolumnx[1:0] bits in the Analog Column Clock Select Register (CLK_CR0). Each analog PSoC block in a particular Analog Column is clocked from the **Acolumn[x]** system-clocking signal for that column. (Note that the Acolumn[x] signals have a 1:4 divider on them.)

10.5.1 Analog Column Clock Select Register

Table 64: Analog Column Clock Select Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Acolumn3 [1]	Acolumn3 [0]	Acolumn2 [1]	Acolumn2 [0]	Acolumn1 [1]	Acolumn1 [0]	Acolumn0 [1]	Acolumn0 [0]

Bit [7:6]: **Acolumn3 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [5:4]: **Acolumn2 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [3:2]: **Acolumn1 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [1:0]: **Acolumn0 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Analog Column Clock Select Register (CLK_CR0, Address = Bank 1, 60h)

10.6 Analog Clock Select Register

Table 65: Analog Clock Select Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	SHDIS	ACLK1 [2]	ACLK1 [1]	ACLK1 [0]	ACLK0 [2]	ACLK0 [1]	ACLK0 [0]

Bit 7: **Reserved**

Bit 6: **SHDIS** During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2)

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Select Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s

0 = Sample and hold function enabled
1 = Sample and hold function disabled

Bit [5:3]: **ACLK1 [2:0]**
0 0 0 = Digital Basic Type A Block 00
0 0 1 = Digital Basic Type A Block 01
0 1 0 = Digital Basic Type A Block 02
0 1 1 = Digital Basic Type A Block 03
1 0 0 = Digital Communications Type A Block 04
1 0 1 = Digital Communications Type A Block 05
1 1 0 = Digital Communications Type A Block 06
1 1 1 = Digital Communications Type A Block 07

Bit [2:0]: **ACLK0 [2:0]** Same configurations as ACLK1 [2:0]
0 0 0 = Digital Basic Type A Block 00
0 0 1 = Digital Basic Type A Block 01
0 1 0 = Digital Basic Type A Block 02
0 1 1 = Digital Basic Type A Block 03
1 0 0 = Digital Communications Type A Block 04
1 0 1 = Digital Communications Type A Block 05
1 1 0 = Digital Communications Type A Block 06
1 1 1 = Digital Communications Type A Block 07

Analog Clock Select Register (CLK_CR1, Address = Bank 1, 61h)

There are a total of twelve analog PSoC blocks implemented for each of the following types; Analog Continuous Time Type A (ACAxx), Analog Switch Cap Type A (ASAxx), and Analog Switch Cap Type B (ASBxx). These blocks are arranged in an array of three rows by four columns. Each column has one of each type of PSoC block, and the individual PSoC blocks are identified by the row and column in which they reside.

There are two primary types of analog PSoC blocks. Both types contain one op-amp but their principles of operation are quite different. Continuous-time PSoC blocks employ three configuration registers and use resistors to condition amplifier response. Switched capacitor blocks have one comparator and four configuration registers and operate as discrete-time sampling operators. In both types, the configuration registers are

inverting op-amp input) or for loss (center tap to output of the block). Note that setting Gain alone does not guarantee a gain or loss block. Routing of the other ends of the resistor determine this.

Note that connections between GIN and GOUT, and LIN and LOUT are automatically resolved by PSoC Designer when they are set in a differential configuration with an adjacent CT block.

Table 66: Analog Continuous Time Block xx Control 0 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	RTap-Mux[3]	RTap-Mux[2]	RTap-Mux[1]	RTap-Mux[0]	Gain	RTopMux	RBotMux[1]	RBotMux[0]

Bit [7:4]: **RTapMux [3:0]** Encoding for selecting 1 of 16 resistor taps
0 0 0 0 = Rf 15 = Ri 01 = Loss .0625 / Gain 16.00
0 0 0 1 = Rf 14 = Ri 02 = Loss .1250 / Gain 8.000
0 0 1 0 = Rf 13 = Ri 03 = Loss .1875 / Gain 5.333
0 0 1 1 = Rf 12 = Ri 04 = Loss .2500 / Gain 4.000
0 1 0 0 = Rf 11 = Ri 05 = Loss .3125 / Gain 3.200
0 1 0 1 = Rf 10 = Ri 06 = Loss .3750 / Gain 2.667
0 1 1 0 = Rf 09 = Ri 07 = Loss .4375 / Gain 2.286
0 1 1 1 = Rf 08 = Ri 08 = Loss .5000 / Gain 2.000
1 0 0 0 = Rf 07 = Ri 09 = Loss .5625 / Gain 1.778
1 0 0 1 = Rf 06 = Ri 10 = Loss .6250 / Gain 1.600
1 0 1 0 = Rf 05 = Ri 11 = Loss .6875 / Gain 1.455
1 0 1 1 = Rf 04 = Ri 12 = Loss .7500 / Gain 1.333
1 1 0 0 = Rf 03 = Ri 13 = Loss .8125 / Gain 1.231
1 1 0 1 = Rf 02 = Ri 14 = Loss .8750 / Gain 1.143
1 1 1 0 = Rf 01 = Ri 15 = Loss .9375 / Gain 1.067
1 1 1 1 = Rf 00 = Ri 16 = Loss 1.000 / Gain 1.000

Bit 3: **Gain** Select gain or loss configuration for output tap
0 = Loss
1 = Gain

Bit 2: **RTopMux** Encoding for feedback resistor select
0 = Rtop to Vcc
1 = Rtop to op-amp's output

Bit [1:0]: **RBotMux [1:0]** Encoding for feedback resistor select

	ACA00	ACA01	ACA02	ACA03
0 0 =	ACA01	ACA00	ACA03	ACA02
0 1 =	AGND	AGND	AGND	AGND
1 0 =	Vss	Vss	Vss	Vss
1 1 =	ASA10	ASB11	ASA12	ASB13

Analog Continuous Time Block 00 Control 0 Register (ACA00CR0, Address = Bank 0/1, 71h)
Analog Continuous Time Block 01 Control 0 Register (ACA01CR0, Address = Bank 0/1, 75h)
Analog Continuous Time Block 02 Control 0 Register (ACA02CR0, Address = Bank 0/1, 79h)
Analog Continuous Time Block 03 Control 0 Register (ACA03CR0, Address = Bank 0/1, 7Dh)

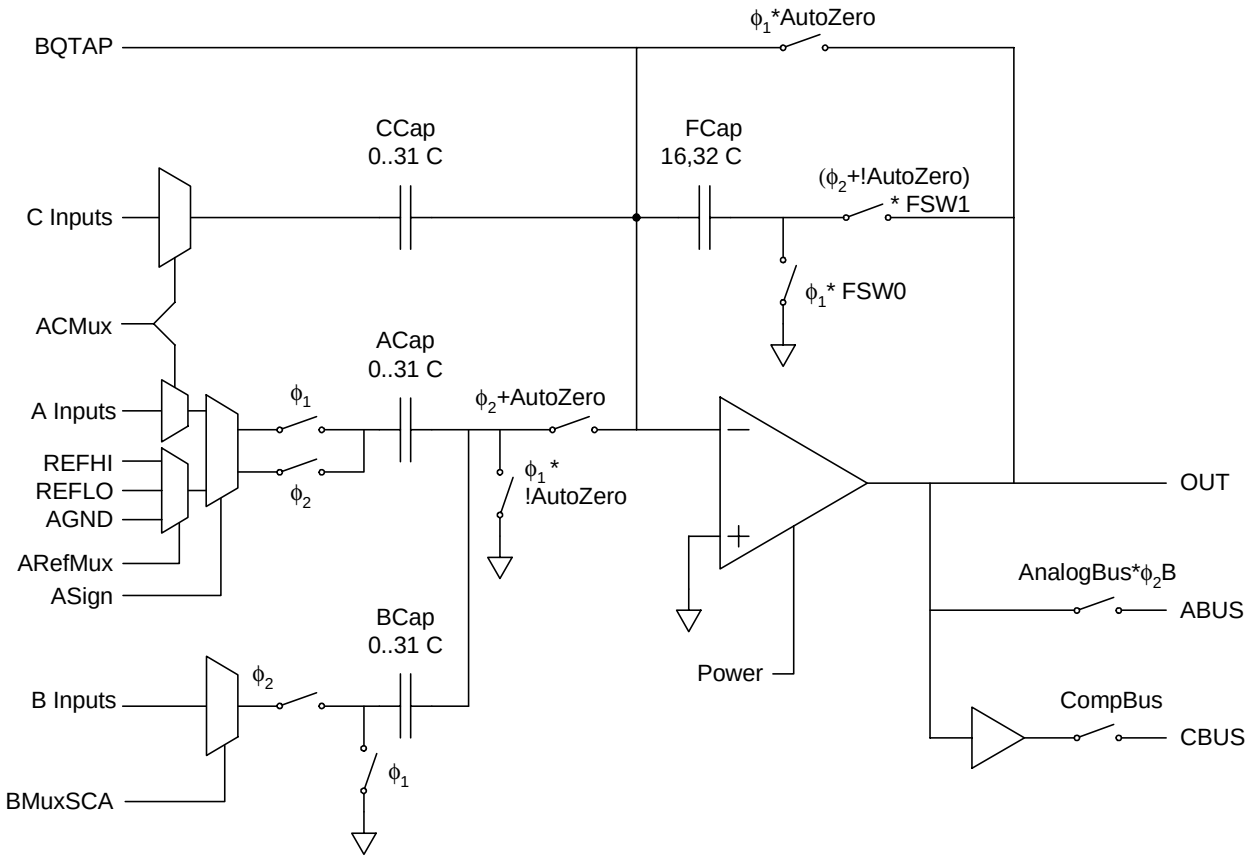

Figure 22: Analog Switch Cap Type A PSoC Blocks

Table 71: Analog Switch Cap Type A Block xx Control 2 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	AutoZero	CCap[4]	CCap[3]	CCap[2]	CCap[1]	CCap[0]

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable output to analog column bus
1 = Enable output to analog column bus
(The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASA10CR0, ASA12CR0, ASA21CR0, ASA23CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the signal that is output to the analog column bus is selected by the ClockPhase bit. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus.)

Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable output to comparator bus
1 = Enable output to comparator bus

Bit 5: **AutoZero** Bit for controlling gated switches
0 = Shorting switch is not active. Input cap branches shorted to op-amp input
1 = Shorting switch is enabled during internal PHI1. Input cap branches shorted to analog ground during internal PHI1 and to op-amp input during internal PHI2.

Bit [4:0]: **CCap [4:0]** Binary encoding for 32 possible capacitor sizes for C Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type A Block 10 Control 2 Register (ASA10CR2, Address = Bank 0/1, 82h)
Analog Switch Cap Type A Block 12 Control 2 Register (ASA12CR2, Address = Bank 0/1, 8Ah)
Analog Switch Cap Type A Block 21 Control 2 Register (ASA21CR2, Address = Bank 0/1, 96h)
Analog Switch Cap Type A Block 23 Control 2 Register (ASA23CR2, Address = Bank 0/1, 9Eh)

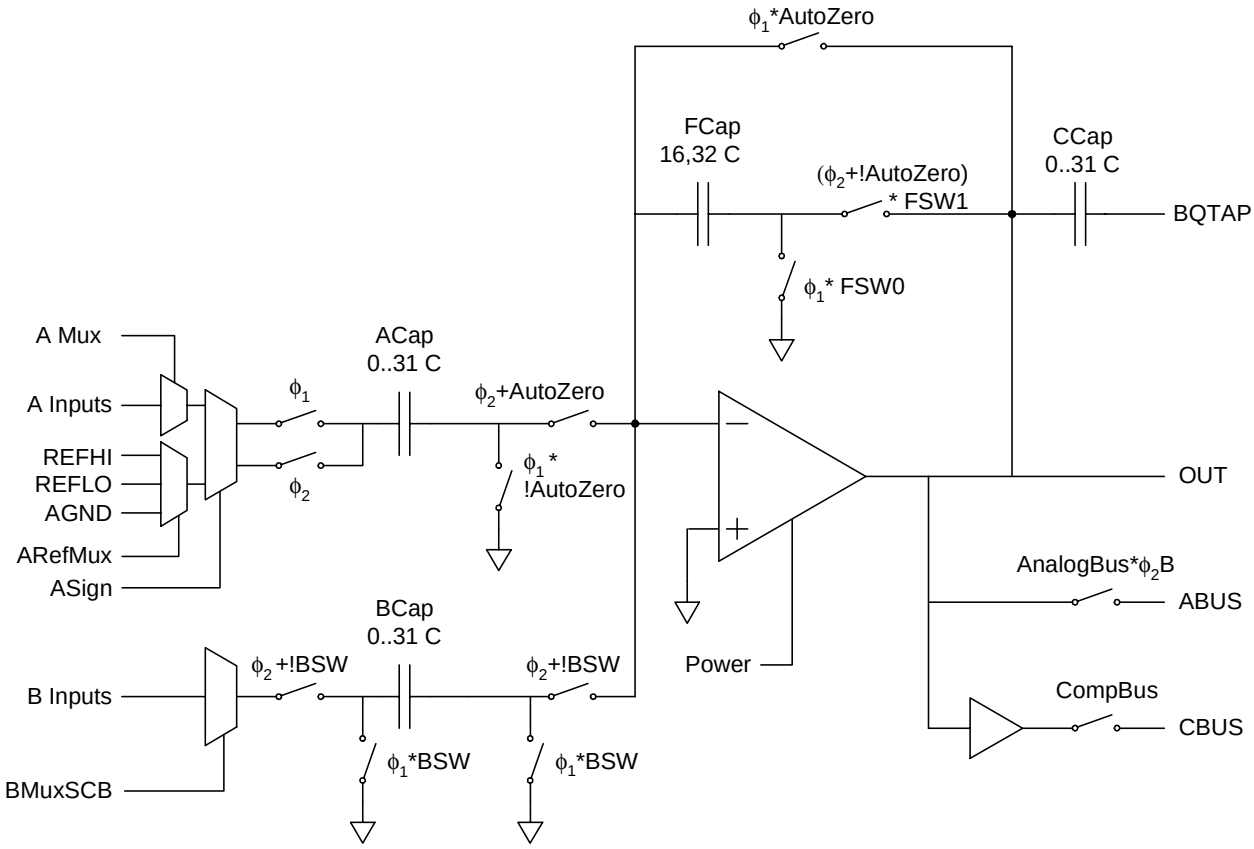

Figure 26: Analog Switch Cap Type B PSoC Blocks

10.9.2 Registers

10.9.2.1 Analog Switch Cap Type B Block xx Control 0 Register

FCap controls the size of the switched feedback capacitor in the integrator.

ClockPhase controls the internal clock phasing relative to the input clock phasing. ClockPhase affects the output of the analog column bus which is controlled by the AnalogBus bit in Control 2 Register (ASB11CR2, ASB13CR2, ASB20CR2, ASB22CR2).

ASign controls the switch phasing of the switches on the bottom plate of the A capacitor. The bottom plate samples the input or the reference.

The ACap bits set the value of the capacitor in the A path.

Table 73: Analog Switch Cap Type B Block xx Control 0 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	FCap	ClockPhase	ASign	ACap[4]	ACap[3]	ACap[2]	ACap[1]	ACap[0]

10.9.2.2 Analog Switch Cap Type B Block xx Control 1 Register

AMux controls the input muxing for the A capacitor branch.

The BCap bits set the value of the capacitor in the B path.

Table 74: Analog Switch Cap Type B Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AMux[2]	AMux[1]	AMux[0]	BCap[4]	BCap[3]	BCap[2]	BCap[1]	BCap[0]

Bit [7:5]: **AMux [2:0]** Input muxing select for A capacitor branch. (Note that available mux inputs vary by individual PSoC block.)

ASB11	ASB13	ASB20	ASB22
0 0 0 = ACA01	ACA03	ASA10	ASA12
0 0 1 = ASA12	P2.2	P2.1	ASA21
0 1 0 = ASA10	ASA12	ASA21	ASA23
0 1 1 = ASA21	ASA23	ABUS0	ABUS2
1 0 0 = REFHI	REFHI	REFHI	REFHI
1 0 1 = ACA00	ACA02	ASB11	ASB13
1 1 0 = Reserved	Reserved	Reserved	Reserved
1 1 1 = Reserved	Reserved	Reserved	Reserved

Bit [4:0]: BCap [4:0] Binary encoding for 32 possible capacitor sizes for B Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 1 Register (ASB11CR1, Address = Bank 0/1, 85h)
Analog Switch Cap Type B Block 13 Control 1 Register (ASB13CR1, Address = Bank 0/1, 8Dh)
Analog Switch Cap Type B Block 20 Control 1 Register (ASB20CR1, Address = Bank 0/1, 91h)
Analog Switch Cap Type B Block 22 Control 1 Register (ASB22CR1, Address = Bank 0/1, 99h)

10.12.4 Analog Output Buffer Control Register

Table 81: Analog Output Buffer Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	--	W
Bit Name	ACol1Mux	ACol2Mux	ABUF1EN	ABUF2EN	ABUF0EN	ABUF3EN	Reserved	PWR

Bit 7: **ACol1Mux**
0 = Set column 1 input to column 1 input mux output
1 = Set column 1 input to column 0 input mux output

Bit 6: **ACol2Mux**
0 = Set column 2 input to column 2 input mux output
1 = Set column 2 input to column 3 input mux output

Bit 5: **ABUF1EN** Enables the analog output buffer for Analog Column 1 (Pin P0[5])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 4: **ABUF2EN** Enables the analog output buffer for Analog Column 2 (Pin P0[4])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 3: **ABUF0EN** Enables the analog output buffer for Analog Column 0 (Pin P0[3])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 2: **ABUF3EN** Enables the analog output buffer for Analog Column 3 (Pin P0[2])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit [1]: **Reserved** Must be left as 0

Bit [0]: **PWR** Determines power level of all output buffers
0 = Low output power
1 = High output power

Analog Output Buffer Control Register (ABF_CR, Address = Bank 1, 62h)

10.13 Analog Modulator

The user has the capability to use the Analog Switch Cap Type A PSoC Blocks in Columns 0 and 2 as amplitude modulators. The Analog Modulator Control Register (AMD_CR) allows the user to select the appropriate modulating signal. When the modulating signal is low, the polarity follows the setting of the ASign bit set in the Analog Switch Cap Type A Control 0 Register (ASAxxCR0). When this signal is high, the normal gain polarity of the PSoC block is inverted.

10.15 Temperature Sensing Capability

A temperature-sensitive voltage derived from the Band Gap sensing on the die is buffered and available as an analog input into the Analog Switch Cap Type A Block ASA21. Temperature sensing allows protection of device operating ranges for fail-safe applications. Temperature sensing combined with a long sleep timer interval (to allow the die to approximate ambient temperature) can give an approximate ambient temperature for data acquisition and battery charging applications. The user may also calibrate the internal temperature rise based on a known current consumption.

The temperature sensor input to the ASA21 block is labeled VTemp, and its associated ground reference is labeled TRefGND (see Figure 22:, Figure 24:).

Table 85: Multiply Result High Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value is the high order result of the multiply function

Multiply Result High Register (MUL_DH, Address = Bank 0, EAh)

Table 86: Multiply Result Low Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value is the low order result of the multiply function

Multiply Result Low Register (MUL_DL, Address = Bank 0, EBh)

Table 87: Accumulator Result 1 / Multiply/Accumulator Input X Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the next to lowest order result of the multiply/accumulate function
8-bit data value when written is the X multiplier input to the multiply/accumulate function

Accumulator Result 1 / Multiply/Accumulator Input X Register (ACC_DR1 / MAC_X, Address = Bank 0, ECh)

Table 88: Accumulator Result 0 / Multiply/Accumulator Input Y Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the lowest order result of the multiply/accumulate function
8-bit data value when written is the Y multiplier input to the multiply/accumulate function

Accumulator Result 0 / Multiply/Accumulator Input Y Register (ACC_DR0 / MAC_Y, Address = Bank 0, EDh)

13.2 DC Characteristics

Table 104: DC Operating Specifications

Symbol	DC Operating Specifications	Minimum	Typical	Maximum	Unit
V_{cc}	Supply Voltage	3.00	-	5.25	V
I_{cc}	Supply Current	-	5	8[1]	mA
I_{sb}	Sleep (Mode) Current	-	-	5[2]	µA
I_{sbxtl}	Sleep (Mode) Current with Crystal Oscillator	-	3	5[3]	µA
V_{ref}	Reference Voltage (Bandgap)	1.275	1.3	1.325[4]	V
V_{il}	Input Low Voltage	-	-	0.8	V
V_{ih}	Input High Voltage	2.2	-	-	V
V_h	Hysterisis Voltage	-	60	-	mV
V_{ol}	Output Low Voltage	-	-	Vss+0.75[5]	V
V_{oh}	Output High Voltage	V_{cc}-1.0[6]	-	-	V
R_{pu}	Pull Up Resistor Value	4000	5600	8000	Ω
R_{pd}	Pull Down Resistor Value	4000	5600	8000	Ω
I_{il}	Input Leakage (Absolute Value)	-	0.1	5	µA
C_{in}	Capacitive Load on Pins as Input	0.5	1.7	10[7]	pF
C_{out}	Capacitive Load on Pins as Output	0.5	1.7	10[7]	pF
V_{LVD}	LVD and SMP Tolerance[8]	0.95 x Ideal[8]	Ideal	1.05 x Ideal[8]	V

1. Conditions are 5.0V, 25 ^{o}C, 3 MHz.
2. Without Crystal Oscillator, V_{cc} = 3.3 V, TA <= 85 ^{o}C.
3. Conditions are 3.0V <= V_{cc} <= 3.6V, -40 ^{o}C <= TA <= 85 ^{o}C. Correct operation assumes a properly loaded, 1 uW maximum drive level, 32.768 kHz crystal.
4. Trimmed for appropriate V_{cc}.
5. Isink = 25 mA, V_{cc} = 4.5 V (maximum of 8 IO sinking, 4 on each side of the IC).
6. Isource =10 mA, V_{cc} = 4.5 V (maximum of 8 IO sourcing, 4 on each side of the IC).
7. Package dependent.
8. Ideal values are +/- 5% absolute tolerance and +/- 1% tolerance relative to each other (for adjacent levels).

13.2.6 DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and -40°C <= TA <= 85°C. The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The bias levels for AGND refer to the bias of the Analog Continuous Time PSoC block. The bias levels for RefHi and RefLo refer to the Analog Reference Control Register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25C and are for design guidance only. (3.3V replaces 5V for the 3.3V DC Analog Reference Specifications.)

Table 112: 5V DC Analog Reference Specifications

Symbol	5V DC Analog Reference Specifications	Minimum	Typical	Maximum	Unit
	AGND = Vcc/2[1] CT Block Bias = High	V_{cc}/2 - 0.010	V_{cc}/2 - 0.004	V_{cc}/2 + 0.003	V
	AGND = 2*BandGap[1] CT Block Bias = High	2*BG - 0.043	2*BG - 0.010	2*BG + 0.024	V
	AGND = P2[4] (P2[4] = Vcc/2)[1] CT Block Bias = High	P24 - 0.013	P24 0.001	P24 + 0.014	V
	AGND Column to Column Variation (AGND=Vcc/2)[1] CT Block Bias = High	-0.034	0.000	0.034	mV
	REFHI = Vcc/2 + BandGap Ref Control Bias = High	V_{cc}/2+BG - 0.140	V_{cc}/2+BG - 0.018	V_{cc}/2+BG + 0.103	V
	REFHI = 3*BandGap Ref Control Bias = High	3*BG - 0.112	3*BG - 0.018	3*BG + 0.076	V
	REFHI = 2*BandGap + P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG+P2[6] - 0.113	2*BG+P2[6] - 0.018	2*BG+P2[6]+ 0.077	V
	REFHI = P2[4] + BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]+BG - 0.130	P2[4]+BG - 0.016	P2[4]+BG + 0.098	V
	REFHI = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]+P2[6] - 0.133	P2[4]+P2[6] - 0.016	P2[4]+P2[6]+ 0.100	V
	REFLO = Vcc/2 – BandGap Ref Control Bias = High	V_{cc}/2-BG - 0.051	V_{cc}/2-BG + 0.024	V_{cc}/2-BG + 0.098	V
	REFLO = BandGap Ref Control Bias = High	BG - 0.082	BG + 0.023	BG + 0.129	V
	REFLO = 2*BandGap - P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG-P2[6] - 0.084	2*BG-P2[6] + 0.025	2*BG-P2[6] + 0.134	V
	REFLO = P2[4] – BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]-BG - 0.056	P2[4]-BG + 0.026	P2[4]-BG + 0.107	V
	REFLO = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]-P2[6] - 0.057	P24-P26 + 0.026	P2[4]-P2[6] + 0.110	V

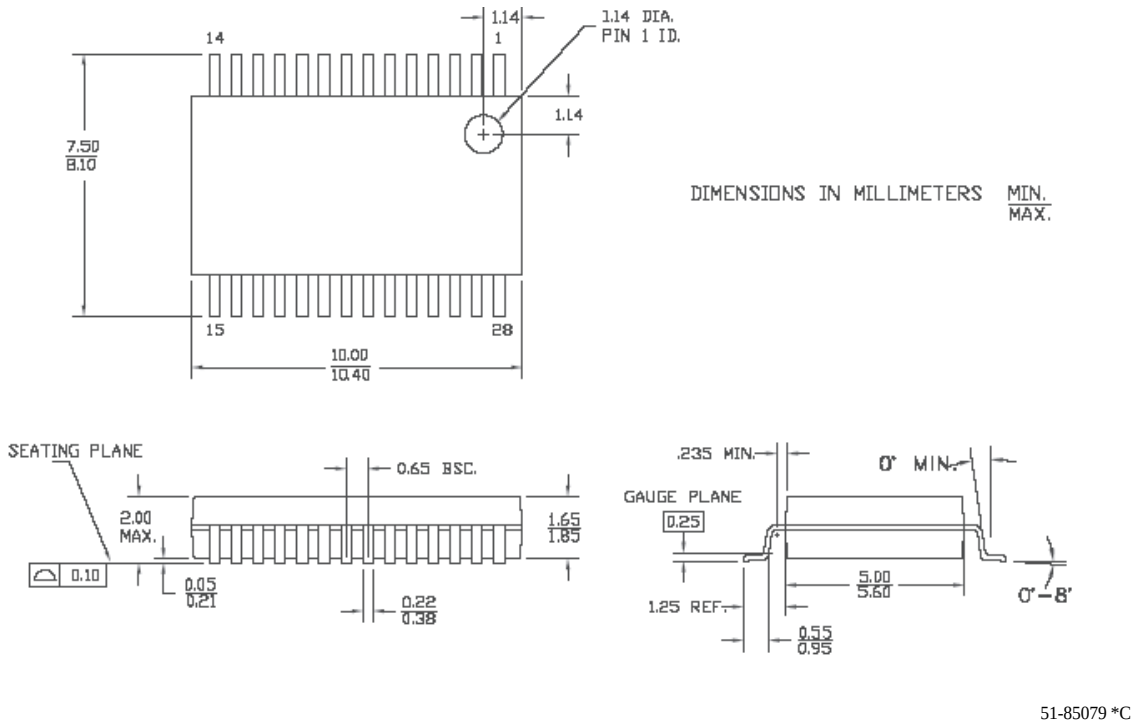

Figure 39: 28-Lead (210-Mil) Shrunk Small Outline Package O28

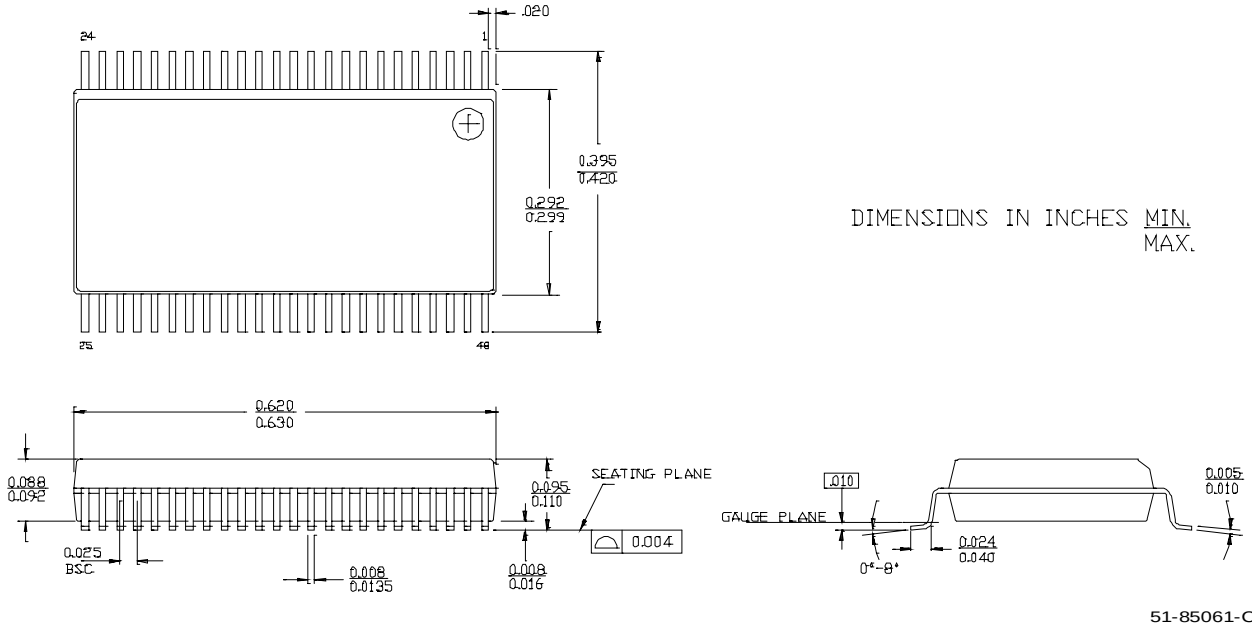

Figure 40: 48-Lead Shrunk Small Outline Package O48

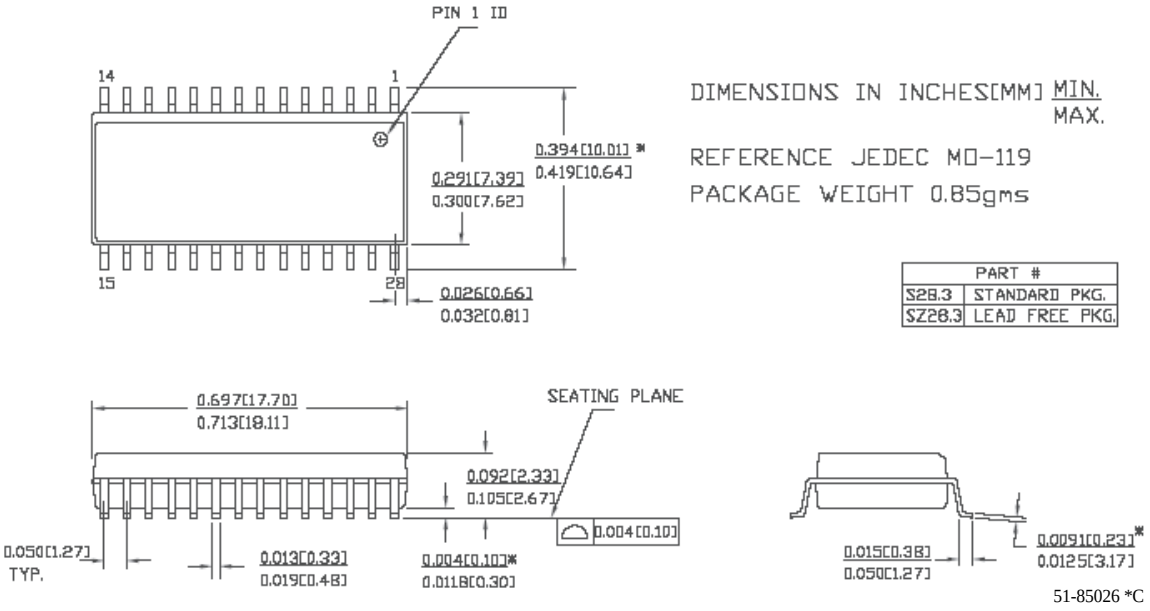

Figure 45: 28-Lead (300-Mil) Molded SOIC S21

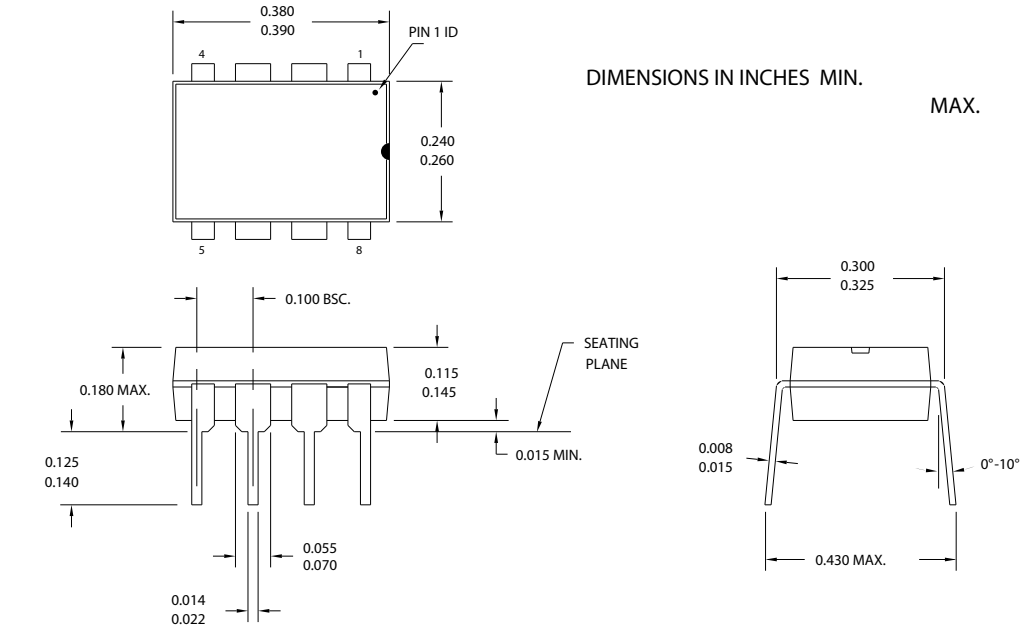

Figure 46: 8-Lead (300-Mil) Molded DIP