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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26233-24pvxi

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List of Figures

6.0 I/O Registers

6.1 Port Data Registers

Table 28: Port Data Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]** When written is the bits for output on port pins. When read is the state of the port pins								

Port 0 Data Register (PRT0DR, Address = Bank 0, 00h)
Port 1 Data Register (PRT1DR, Address = Bank 0, 04h)
Port 2 Data Register (PRT2DR, Address = Bank 0, 08h)
Port 3 Data Register (PRT3DR, Address = Bank 0, 0Ch)
Port 4 Data Register (PRT4DR, Address = Bank 0, 10h)
Port 5 Data Register (PRT5DR, Address = Bank 0, 14h) **Note**: Port 5 is 4-bits wide, Bit [3:0]

6.2 Port Interrupt Enable Registers

Table 29: Port Interrupt Enable Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	Int En [7]	Int En [6]	Int En [5]	Int En [4]	Int En [3]	Int En [2]	Int En [1]	Int En [0]
Bit [7:0]: **Int En [7:0]** When written sets the pin interrupt state 0 = Interrupt disabled for pin 1 = Interrupt enabled for pin								

Port 0 Interrupt Enable Register (PRT0IE, Address = Bank 0, 01h)
Port 1 Interrupt Enable Register (PRT1IE, Address = Bank 0, 05h)
Port 2 Interrupt Enable Register (PRT2IE, Address = Bank 0, 09h)
Port 3 Interrupt Enable Register (PRT3IE, Address = Bank 0, 0Dh)
Port 4 Interrupt Enable Register (PRT4IE, Address = Bank 0, 11h)
Port 5 Interrupt Enable Register (PRT5IE, Address = Bank 0, 15h) **Note**: Port 5 is 4-bits wide

6.3.4 Port Interrupt Control 1 Registers

Table 34: Port Interrupt Control 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	W	W
Bit Name	IC1 [7]	IC1 [6]	IC1 [5]	IC1 [4]	IC1 [3]	IC1 [2]	IC1 [1]	IC1 [0]
Bit [7:0]: **IC1 [7:0]** See truth table for Port Interrupt Control 0 Registers, above								

Port 0 Interrupt Control 1 Register (PRT0IC1, Address = Bank 1, 03h)
Port 1 Interrupt Control 1 Register (PRT1IC1, Address = Bank 1, 07h)
Port 2 Interrupt Control 1 Register (PRT2IC1, Address = Bank 1, 0Bh)
Port 3 Interrupt Control 1 Register (PRT3IC1, Address = Bank 1, 0Fh)
Port 4 Interrupt Control 1 Register (PRT4IC1, Address = Bank 1, 13h)
Port 5 Interrupt Control 1 Register (PRT5IC1, Address = Bank 1, 17h) **Note**: Port 5 is 4-bits wide

Digital Communications Type A Block 06 Data Register 2 (DCA06DR2, Address = Bank 0, 3Ah)
Digital Communications Type A Block 07 Data Register 0 (DCA07DR0, Address = Bank 0, 3Ch)
Digital Communications Type A Block 07 Data Register 1 (DCA07DR1, Address = Bank 0, 3Dh)
Digital Communications Type A Block 07 Data Register 2 (DCA07DR2, Address = Bank 0, 3Eh)

Table 53: R/W Variations per User Module Selection

Function	DR0	R/W	DR1	R/W	DR2	R/W
Timer	Count	R[1]	Period Value	W	Capture Value	RW
Counter	Count	R[1]	Period Value	W	Compare Value	RW
CRC	Current Value/CRC Residue	R[1]	Polynomial Mask Value	W	Seed Value	RW
PRS	Current Value	R[1]	Polynomial Mask Value	W	Seed Value	RW
Deadband	Count	R[1]	Period Value	W	Not Used	RW
RX UART	Shifter	NA	Not Used	NA	Data Register	R
TX UART	Shifter	NA	Data Register	W	Not Used	NA
SPI	Shifter	NA	TX Data Register		RX Data Register	R

1. Each time the register is read, its value is written to the DR2 register.

9.3.2 Digital Basic Type A / Communications Type A Block xx Control Register 0

Table 54: Digital Basic Type A / Communications Type A Block xx Control Register 0

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]**								

1. Varies by function.

Digital Basic Type A Block 00 Control Register 0 (DBA00CR0, Address = Bank 0, 23h)
Digital Basic Type A Block 01 Control Register 0 (DBA01CR0, Address = Bank 0, 27h)
Digital Basic Type A Block 02 Control Register 0 (DBA02CR0, Address = Bank 0, 2Bh)
Digital Basic Type A Block 03 Control Register 0 (DBA03CR0, Address = Bank 0, 2Fh)
Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

9.3.3 Digital Basic Type A/Communications Type A Block xx Control Register 0 When Used as Timer, Counter, CRC, and Deadband

Note that the data in this register, as well as the following three registers, are a mapping of the functions of the variables selected in the associated Digital Basic Type A/ Communications Type A Block xx Control Register 0.

Table 55: Digital Basic Type A/Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	--	--	--	--	--	--	--	0
Read/Write	--	--	--	--	--	--	--	RW
Bit Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Enable

Bit 7: **Reserved**
Bit 6: **Reserved**
Bit 5: **Reserved**
Bit 4: **Reserved**
Bit 3: **Reserved**
Bit 2: **Reserved**
Bit 1: **Reserved**

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Basic Type A Block 00 Control Register 0 (DBA00CR0, Address = Bank 0, 23h)
Digital Basic Type A Block 01 Control Register 0 (DBA01CR0, Address = Bank 0, 27h)
Digital Basic Type A Block 02 Control Register 0 (DBA02CR0, Address = Bank 0, 2Bh)
Digital Basic Type A Block 03 Control Register 0 (DBA03CR0, Address = Bank 0, 2Fh)
Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

9.3.4 Digital Communications Type A Block xx Control Register 0 When Used as UART Transmitter

Table 56: Digital Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	--	--	R	R	--	RW	RW	RW
Bit Name	Reserved	Reserved	TX Complete	TX Reg Empty	Reserved	Parity Type	Parity Enable	Enable

Bit 7: **Reserved**
Bit 6: **Reserved**

Bit 5: **TX Complete**
0 = Indicates that if a transmission has been initiated, it is still in progress
1 = Indicates that the current transmission is complete (including framing bits)
Optional interrupt source for TX UART. Reset when this register is read.

Bit 4: **TX Reg Empty**
0 = Indicates TX Data register is not available to accept another byte (writing to register will cause data to be lost)
1 = Indicates TX Data register is available to accept another byte
Note that the interrupt does not occur until at least 1 byte has been previously written to the TX Data Register
Default interrupt source for TX UART. Reset when the TX Data Register (Data Register 1) is written.

Bit 3: **Reserved**

Bit 2: **Parity Type**
0 = Even
1 = Odd

Bit 1: **Parity Enable**
0 = Parity Disabled
1 = Parity Enabled

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

10.4 Analog Reference Control

The reference generator establishes a set of three internally fixed reference voltages for the whole chip, AGND, RefHi and RefLo. The 8C26xxx is a single supply part, with no negative voltage available or applicable. Analog ground (AGND) is constructed near mid-supply. This ground is routed to all analog blocks and separately buffered within each block. There may be a small offset voltage between buffered analog grounds, as indicated in the AC/DC Characteristics section. RefHi and RefLo signals are generated, buffered and routed to the analog blocks. RefHi is used to set the conversion range (i.e., span) of analog to digital (ADC) and digital to analog (DAC) converters. RefHi and RefLo can be used to set thresholds in comparators.

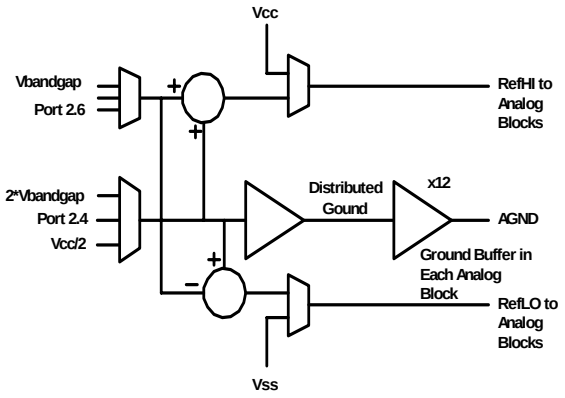

Figure 17: Analog Reference Control Schematic

10.4.1 Bandgap Test

BGT Bandgap Test is used for factory testing of the internal reference voltage testing.

10.4.2 Bias Level

HBE Controls the bias level for all analog functions. It operates with the power setting in each block to set the parameters of that block. Most applications will benefit most from the low bias level. At high bias, the analog block op-amps have faster slew rate but slightly less voltage swing and higher noise.

10.4.3 AGND, RefHI, RefLO

REF Sets Analog Array Reference Control, selecting specific combinations of voltage for analog ground and references. Many of these reference voltages are based on the precision internal reference, a Silicon band gap operating at 1.300 Volts. This reference has good thermal stability and power supply rejection.

Alternatively, the power supply can be scaled to provide analog ground and references; this is particularly useful for signals, which are ratiometric to the power supply voltage.

User supplied external precision references can be connected to Port 2 inputs (available on 28 pin and larger parts). This is useful in setting reference for specific customer applications such as a +/-1.000 V (from AGND) ADC scale. References derived from Port 2 inputs are limited to the same output voltage range as the op-amps in the analog blocks.

10.8 Analog Switch Cap Type A PSoC Blocks

10.8.1 Introduction

The Analog Switch Cap Type A PSoC blocks are built around an operational amplifier. There are several analog muxes that are controlled by register-bit settings in the control registers that determine the signal topology inside the block. There are also four arrays of unit value capacitors that are located in the feedback path for the op-amp, and are switched by two phase clocks, PHI1 and PHI2. These four capacitor arrays are labeled A Cap Array, B Cap Array, C Cap Array, and F Cap Array. There is also an analog comparator connected to the output OUT, which converts analog comparisons into digital signals.

There are three discrete outputs from this block. These outputs are:

1. The analog output bus (ABUS), which is an analog bus resource that is shared by all of the analog blocks in the analog column for that block.

2. The comparator bus (CBUS), which is a digital bus that is a resource that is shared by all of the analog blocks in a column for that block.

3. The output bus (OUT), which is an analog bus resource that is shared by all of the analog blocks in a column and connects to one of the analog output buffers, to send a signal externally to the device.

SC Integrator Block A supports Delta-Sigma, Successive Approximation and Incremental A/D Conversion, Capacitor DACs, and SC filters. It has three input arrays of binarily-weighted switched capacitors, allowing user programmability of the capacitor weights. This provides summing capability of two (CDAC) scaled inputs, and a non-switched capacitor input. Since the input of SC Block A has this additional switched capacitor, it is configured for the input stage of such a switched capacitor biquad filter. When followed by an SC Block B Integrator, this combination of blocks can be used to provide a full Switched Capacitor Biquad.

10.12.4 Analog Output Buffer Control Register

Table 81: Analog Output Buffer Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	--	W
Bit Name	ACol1Mux	ACol2Mux	ABUF1EN	ABUF2EN	ABUF0EN	ABUF3EN	Reserved	PWR

Bit 7: **ACol1Mux**
0 = Set column 1 input to column 1 input mux output
1 = Set column 1 input to column 0 input mux output

Bit 6: **ACol2Mux**
0 = Set column 2 input to column 2 input mux output
1 = Set column 2 input to column 3 input mux output

Bit 5: **ABUF1EN** Enables the analog output buffer for Analog Column 1 (Pin P0[5])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 4: **ABUF2EN** Enables the analog output buffer for Analog Column 2 (Pin P0[4])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 3: **ABUF0EN** Enables the analog output buffer for Analog Column 0 (Pin P0[3])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 2: **ABUF3EN** Enables the analog output buffer for Analog Column 3 (Pin P0[2])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit [1]: **Reserved** Must be left as 0

Bit [0]: **PWR** Determines power level of all output buffers
0 = Low output power
1 = High output power

Analog Output Buffer Control Register (ABF_CR, Address = Bank 1, 62h)

10.13 Analog Modulator

The user has the capability to use the Analog Switch Cap Type A PSoC Blocks in Columns 0 and 2 as amplitude modulators. The Analog Modulator Control Register (AMD_CR) allows the user to select the appropriate modulating signal. When the modulating signal is low, the polarity follows the setting of the ASign bit set in the Analog Switch Cap Type A Control 0 Register (ASAxxCR0). When this signal is high, the normal gain polarity of the PSoC block is inverted.

Table 89: Accumulator Result 3 / Multiply/Accumulator Clear 0 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the highest order result of the multiply/accumulate function
Any 8-bit data value when written will cause all four Accumulator result registers to clear

Accumulator Result 3 / Multiply/Accumulator Clear 0 Register (ACC_DR3 / MAC_CL0, Address = Bank 0, EEh)

Table 90: Accumulator Result 2 / Multiply/Accumulator Clear 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is next to highest order result of the multiply/accumulate function
Any 8-bit data value when written will cause all four Accumulator result registers to clear

Accumulator Result 2 / Multiply/Accumulator Clear 1 Register (ACC_DR2 / MAC_CL1, Address = Bank 0, EFh)

11.2 Decimator

The output of a ΔΣ modulator is a high-speed, single bit A/D converter. A single bit A/D converter is of little use to anyone and must be converted to a lower speed multiple bit output. Converting this high-speed single bit data stream to a lower speed multiple bit data stream requires a data decimator.

A “divide by n” decimator is a digital filter that takes the single bit data at a fast rate and outputs multiple bits at one n^{th} the speed. For a single stage ΔΣ converter, the optimal filter has a $sinc^2$ response. This filter can be implemented as a finite impulse response (FIR) filter and for a “divide by n” implementation should have the following coefficients:

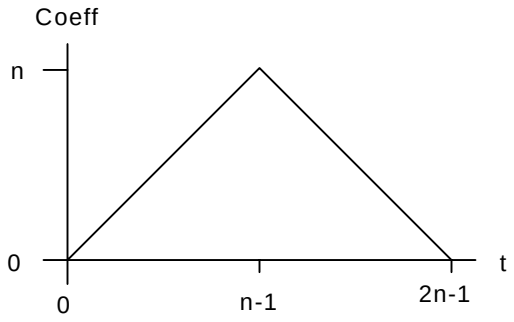

Figure 30: Decimator Coefficients

11.8.1 Additional Function for Table Read Supervisory Call

The Table Read supervisory operation will return the Version ID in the Accumulator. The value in the Accumulator is divided into a high and low nibble, indicating major and minor revisions, respectively. **Note**: The value in the X register is modified during the Table Read Supervisory Call, and must be saved and restored if needed after the call completes.

- A[7:4]: Major silicon revisions.
- A[3:0]: Minor silicon revisions.

Table 99: Table Read for Supervisory Call Functions

Table ID	Function	TV(0)	TV(1)	TV(2)	TV(3)	TV(4)	TV(5)	TV(6)	TV(7)
00[1]	Production Silicon ID	Silicon ID 1	Silicon ID 0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01	Provides trim value for Internal Main Oscillator and Internal Voltage Reference	Internal Voltage Reference trim value for 3.3V	Internal Main Oscillator trim value for 3.3V	Reserved	Reserved	Internal Voltage Reference trim value for 5.0V	Internal Main Oscillator trim value for 5.0V	Reserved	Reserved

1. Determines silicon revision values in Accumulator and X registers.

11.9 Flash Program Memory Protection

The user has the option to define the access to the Flash memory. A flexible system allows the user to select one of four protection modes for each 64-byte block within the Flash, based on the particular application. The protection mechanism is implemented by a device programmer using the System Supervisor Call. When this command is executed, two bits within the data programmed into the Flash will select the protection mode. It is not intended that the protection byte will be modified by the user's code. The following table lists the available protection options:

Table 100: Flash Program Memory Protection

Mode Bits	Mode Name	External Read	External Write	Internal Write
00	Unprotected	Enabled	Enabled	Enabled
01	Factory Upgrade	Disabled	Enabled	Enabled
10	Field Upgrade	Disabled	Disabled	Enabled
11	Full Protection	Disabled	Disabled	Disabled

Note: Mode 10 is the default.

11.10 Programming Requirements and Step Descriptions

The pins in the following table are critical for the programmer:

Table 101: Programmer Requirements

Pin Name	Function	Programmer HW Pin Requirements
SDATA	Serial Data In/Out	Drive TTL Levels, Read TTL, High Z
SCLK	Serial Clock	Drive TTL levEl Clock Signal
V_{ss}	Power Supply Ground Connection	Low Resistance Ground Connection
V_{cc}	Power Supply Positive Voltage	0V, 3.0V, 5V, & 5.4V. 0.1V Accuracy. 20mA Current Capability

11.10.1 Data File Read

The user's data file should be read into the programmer. The checksum should be calculated by the programmer for each record and compared to the record checksum stored in the file for each record. If there is an error, a message should be sent to the user explaining that the file has a checksum error and the programming should not be allowed to continue.

11.10.2 Programmer Flow

The following sequence (with descriptions) is the main flow used to program the devices: (Note that failure at any step will result in termination of the flow and an error message to the device programmer's operator.)

11.10.2.1 Verify Silicon ID

The silicon ID is read and verified against the expected value. If it is not the expected value, then the device is failed and an error message is sent to the device programmer's operator.

This test will detect a bad connection to the programmer or an incorrect device selection on the programmer.

The silicon ID test is required to be first in the flow and cannot be bypassed. The sequence is as follows:

```
Set Vcc=0V
Set SDATA=HighZ
Set SCLK=VILP
Set Vcc=Vccp
Start the programmer's SCLK driver
"free running"
WAIT-AND-POLL
ID-SETUP
WAIT-AND-POLL
READ-ID-WORD
```

Notes: See "DC Specifications" table in section 13 for value of Vccp and VILP. See "AC Specifications" table in section 13 for value of frequency for the SCLK driver (Fsclk).

11.10.2.2 Erase

The Flash memory is erased. This is accomplished by the following sequence:

```
SET-CLK-FREQ(num_MHz_times_5)
Erase All
WAIT-AND-POLL
```

11.10.2.3 Program

The Flash is programmed with the contents of the user's programming file. This is accomplished by the following sequence:

```
For num_block = 0 to max_data_block
For address =0 to 63
WRITE-BYTE(address,data):
End for address loop
SET-CLK-FREQ(num_MHz_times_5)
SET-BLOCK-NUM(num_block)
PROGRAM-BLOCK
WAIT-AND-POLL
End for num_block loop
```

11.10.2.4 Verify (at Low Vcc and High Vcc)

The device data is read out to compare to the data in the user's programming file. This is accomplished by the following sequence:

```
For num_block = 0 to max_data_block
SET-BLOCK-NUM (num_block)
VERIFY-SETUP
Wait & POLL the SDATA for a high to
low transition
For address =0 to max_byte_per_block
READ-BYTE(address,data)
End for address loop
End for num_block loop
```

Note: This should be done 2 times; once at Vcc=Vcclv and once at Vcc=Vcchv.

11.10.2.5 Set Security

The security operation protects certain blocks from being read or changed. This is done at the end of the flow so that the security does not interfere with the verify step. Security is set with the following sequence:

```
For address =0 to 63
WRITE-SECURITY-BYTE(address,data):
End for address loop
SET-CLK-FREQ(num_MHz_times_5)
SECURE
WAIT-AND-POLL
```

Note: This sequence is done at Vcc=Vccp.

13.0 DC and AC Characteristics

Specifications are valid for -40 °C </= T_A </= 85 °C and T_J </= 100 °C as specified, except where noted. Specifications for devices running at 24 MHz are valid at -40 °C </= T_A </= 70°C and T_J </= 82 °C.

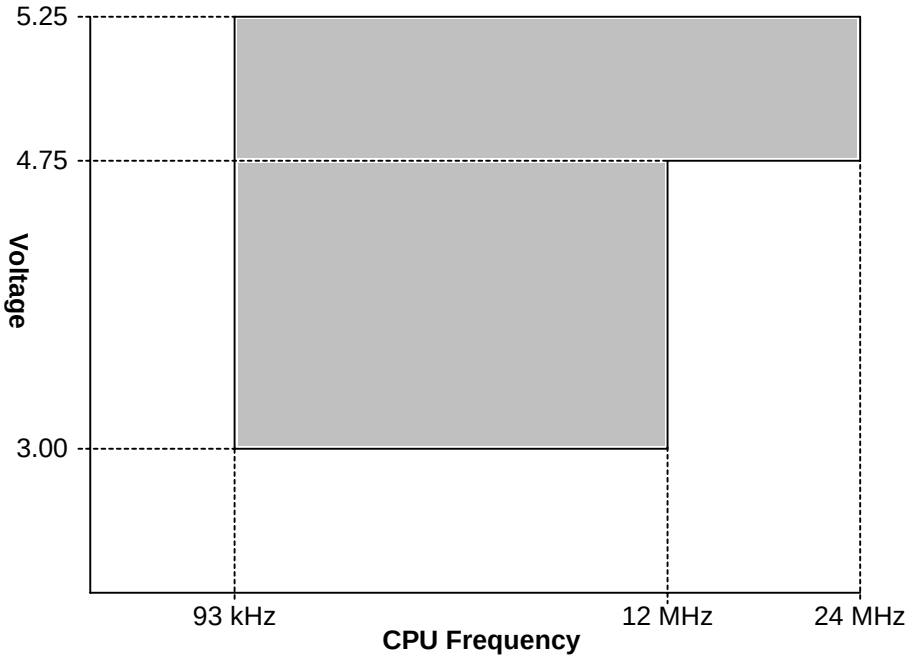

Figure 36: CY8C25xxx/CY8C26xxx Voltage Frequency Graph

13.1 Absolute Maximum Ratings

Table 102: Absolute Maximum Ratings

Symbol	Absolute Maximum Ratings	Minimum	Typical	Maximum	Unit
	Storage Temperature	-65	-	+100 [1]	°C
	Ambient Temperature with Power Applied	-40	-	+85	°C
	Supply Voltage on V_{cc} Relative to V_{ss}	-0.5	-	+6.0	V
	DC Input Voltage	-0.5	-	V_{cc}+0.5	V
	DC Voltage Applied to Tri-state	V_{ss}-0.5	-	V_{cc}+0.5	V
	Maximum Current into any Port Pin	-25	-	+50	mA
	Maximum Current into any Port Pin Configured as Analog Driver	-50	-	+50	mA
	Junction Temperature up to 12 MHz	-	-	100[2]	°C
	Junction Temperature at 24 MHz	-	-	82	°C
	Static Discharge Voltage	2000	-	-	V
	Latch-up Current	200	-	-	mA

1. Higher storage temperatures will reduce data retention time.

13.2.6 DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and -40°C <= TA <= 85°C. The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The bias levels for AGND refer to the bias of the Analog Continuous Time PSoC block. The bias levels for RefHi and RefLo refer to the Analog Reference Control Register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25C and are for design guidance only. (3.3V replaces 5V for the 3.3V DC Analog Reference Specifications.)

Table 112: 5V DC Analog Reference Specifications

Symbol	5V DC Analog Reference Specifications	Minimum	Typical	Maximum	Unit
	AGND = Vcc/2[1] CT Block Bias = High	V_{cc}/2 - 0.010	V_{cc}/2 - 0.004	V_{cc}/2 + 0.003	V
	AGND = 2*BandGap[1] CT Block Bias = High	2*BG - 0.043	2*BG - 0.010	2*BG + 0.024	V
	AGND = P2[4] (P2[4] = Vcc/2)[1] CT Block Bias = High	P24 - 0.013	P24 0.001	P24 + 0.014	V
	AGND Column to Column Variation (AGND=Vcc/2)[1] CT Block Bias = High	-0.034	0.000	0.034	mV
	REFHI = Vcc/2 + BandGap Ref Control Bias = High	V_{cc}/2+BG - 0.140	V_{cc}/2+BG - 0.018	V_{cc}/2+BG + 0.103	V
	REFHI = 3*BandGap Ref Control Bias = High	3*BG - 0.112	3*BG - 0.018	3*BG + 0.076	V
	REFHI = 2*BandGap + P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG+P2[6] - 0.113	2*BG+P2[6] - 0.018	2*BG+P2[6]+ 0.077	V
	REFHI = P2[4] + BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]+BG - 0.130	P2[4]+BG - 0.016	P2[4]+BG + 0.098	V
	REFHI = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]+P2[6] - 0.133	P2[4]+P2[6] - 0.016	P2[4]+P2[6]+ 0.100	V
	REFLO = Vcc/2 – BandGap Ref Control Bias = High	V_{cc}/2-BG - 0.051	V_{cc}/2-BG + 0.024	V_{cc}/2-BG + 0.098	V
	REFLO = BandGap Ref Control Bias = High	BG - 0.082	BG + 0.023	BG + 0.129	V
	REFLO = 2*BandGap - P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG-P2[6] - 0.084	2*BG-P2[6] + 0.025	2*BG-P2[6] + 0.134	V
	REFLO = P2[4] – BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]-BG - 0.056	P2[4]-BG + 0.026	P2[4]-BG + 0.107	V
	REFLO = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]-P2[6] - 0.057	P24-P26 + 0.026	P2[4]-P2[6] + 0.110	V

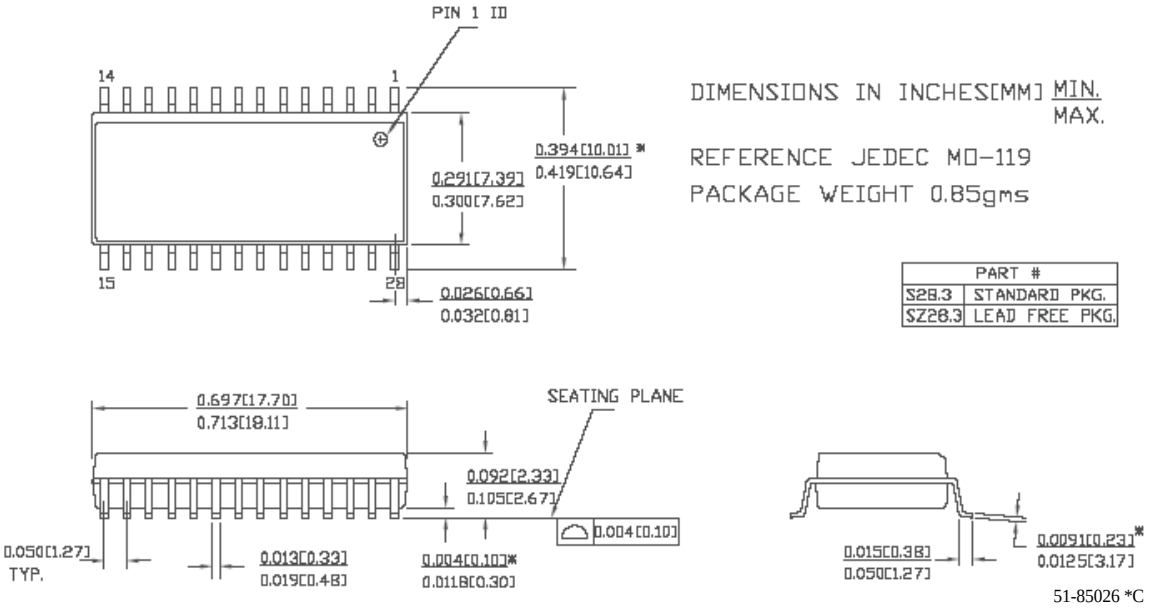

Figure 45: 28-Lead (300-Mil) Molded SOIC S21

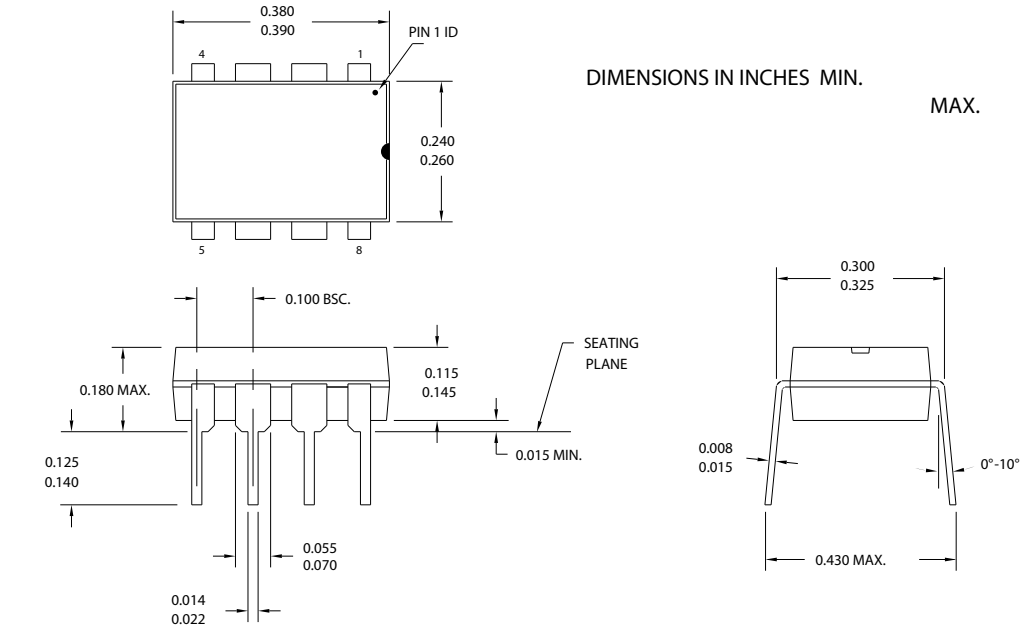

Figure 46: 8-Lead (300-Mil) Molded DIP