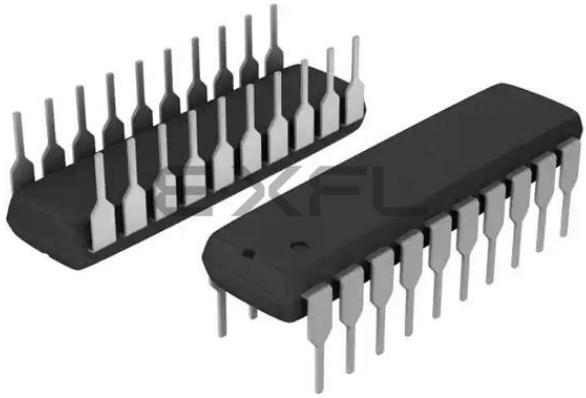

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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26233-24pxi

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1.2 Pin-out Descriptions

Table 2: Pin-out 8 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P1[1]	I/O	3	Port 1[1] / XtalIn / SCLK
Vss	Power	4	Ground
P1[0]	I/O	5	Port 1[0] / XtalOut / SDATA
P0[2]	I/O	6	Port 0[2] (Analog Input/Output)
P0[4]	I/O	7	Port 0[4] (Analog Input/Output)
Vcc	Power	8	Supply Voltage

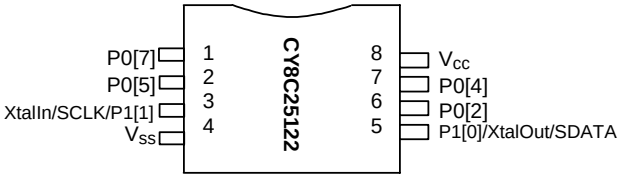

Figure 2: CY8C25122

Table 3: Pin-out 20 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
SMP	O	5	Switch Mode Pump
P1[7]	I/O	6	Port 1[7]
P1[5]	I/O	7	Port 1[5]
P1[3]	I/O	8	Port 1[3]
P1[1]	I/O	9	Port 1[1] / XtalIn / SCLK
Vss	Power	10	Ground
P1[0]	I/O	11	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	12	Port 1[2]
P1[4]	I/O	13	Port 1[4]
P1[6]	I/O	14	Port 1[6]
XRES	I	15	External Reset
P0[0]	I/O	16	Port 0[0] (Analog Input)
P0[2]	I/O	17	Port 0[2] (Analog Input/Output)
P0[4]	I/O	18	Port 0[4] (Analog Input/Output)
P0[6]	I/O	19	Port 0[6] (Analog Input)
Vcc	Power	20	Supply Voltage

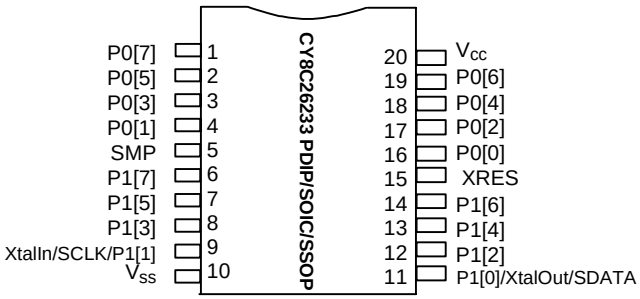

Figure 3: CY8C26233

Table 4: Pin-out 28 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/ Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/ Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
P2[7]	I/O	5	Port 2[7]
P2[5]	I/O	6	Port 2[5]
P2[3]	I/O	7	Port 2[3] (Non-Multiplexed Analog Input)
P2[1]	I/O	8	Port 2[1] (Non-Multiplexed Analog Input)
SMP	O	9	Switch Mode Pump
P1[7]	I/O	10	Port 1[7]
P1[5]	I/O	11	Port 1[5]
P1[3]	I/O	12	Port 1[3]
P1[1]	I/O	13	Port 1[1] / XtalIn / SCLK
Vss	Power	14	Ground
P1[0]	I/O	15	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	16	Port 1[2]
P1[4]	I/O	17	Port 1[4]
P1[6]	I/O	18	Port 1[6]
XRES	I	19	External Reset
P2[0]	I/O	20	Port 2[0] (Non-Multiplexed Analog Input)
P2[2]	I/O	21	Port 2[2] (Non-Multiplexed Analog Input)
P2[4]	I/O	22	Port 2[4] / External AGNDIn
P2[6]	I/O	23	Port 2[6] / External VREFIn
P0[0]	I/O	24	Port 0[0] (Analog Input)
P0[2]	I/O	25	Port 0[2] (Analog Input/Output)
P0[4]	I/O	26	Port 0[4] (Analog Input/Output)
P0[6]	I/O	27	Port 0[6] (Analog Input)
Vcc	Power	28	Supply Voltage

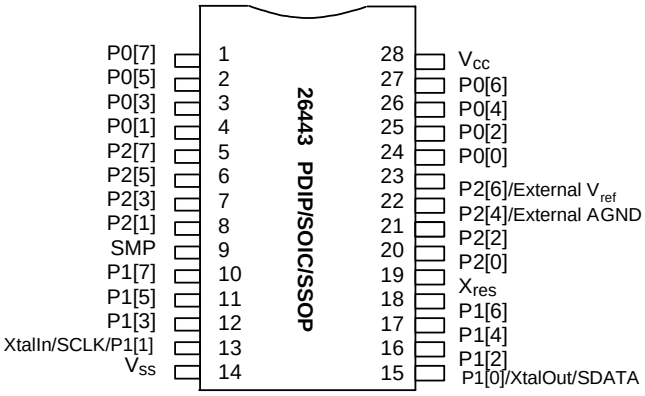

Figure 4: 26443 PDIP/SOIC/SSOP

Table 5: Pin-out 44 Pin

Name	I/O	Pin	Description
P2[5]	I/O	1	Port 2[5]
P2[3]	I/O	2	Port 2[3] (Non-Multiplexed Analog Input)
P2[1]	I/O	3	Port 2[1] (Non-Multiplexed Analog Input)
P3[7]	I/O	4	Port 3[7]
P3[5]	I/O	5	Port 3[5]
P3[3]	I/O	6	Port 3[3]
P3[1]	I/O	7	Port 3[1]
SMP	O	8	Switch Mode Pump
P4[7]	I/O	9	Port 4[7]
P4[5]	I/O	10	Port 4[5]
P4[3]	I/O	11	Port 4[3]
P4[1]	I/O	12	Port 4[1]
P1[7]	I/O	13	Port 1[7]
P1[5]	I/O	14	Port 1[5]
P1[3]	I/O	15	Port 1[3]
P1[1]	I/O	16	Port 1[1] / XtalIn / SCLK
Vss	Power	17	Ground
P1[0]	I/O	18	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	19	Port 1[2]
P1[4]	I/O	20	Port 1[4]
P1[6]	I/O	21	Port 1[6]
P4[0]	I/O	22	Port 4[0]
P4[2]	I/O	23	Port 4[2]
P4[4]	I/O	24	Port 4[4]

2.2 CPU Registers

2.2.1 Flags Register

The Flags Register can only be set or reset with logical instruction.

Table 8: Flags Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	1	0
Read/ Write	--	--	--	RW	R	RW	RW	RW
Bit Name	Reserved	Reserved	Reserved	XIO	Super	Carry	Zero	Global IE

Bit 7: **Reserved**
Bit 6: **Reserved**
Bit 5: **Reserved**

Bit 4: **XIO** Set by the user to select between the register banks
0 = Bank 0
1 = Bank 1

Bit 3: **Super** Indicates whether the CPU is executing user code or Supervisor Code. (This code cannot be accessed directly by the user and is not displayed in the ICE debugger.)
0 = User Code
1 = Supervisor Code

Bit 2: **Carry** Set by CPU to indicate whether there has been a carry in the previous logical/arithmetic operation
0 = No Carry
1 = Carry

Bit 1: **Zero** Set by CPU to indicate whether there has been a zero result in the previous logical/arithmetic operation
0 = Not Equal to Zero
1 = Equal to Zero

Bit 0: **Global IE** Determines whether all interrupts are enabled or disabled
0 = Disabled
1 = Enabled

2.2.2 Accumulator Register

Table 9: Accumulator Register (CPU_A)

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value holds the result of any logical/arithmetic instruction that uses a source addressing mode

1. System - not directly accessible by the user

4.3 Register Bank 1 Map

Table 27: Bank 1

Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access
PRT0DM0	00h	32	W	Reserved	40h			ASA10CR0	80h	88	RW	Reserved	C0h		
PRT0DM1	01h	33	W		41h			ASA10CR1	81h	90	RW		C1h		
PRT0IC0	02h	33	W		42h			ASA10CR2	82h	92	RW		C2h		
PRT0IC1	03h	34	W		43h			ASA10CR3	83h	93	RW		C3h		
PRT1DM0	04h	32	W		44h			ASB11CR0	84h	95	RW		C4h		
PRT1DM1	05h	33	W		45h			ASB11CR1	85h	97	RW		C5h		
PRT1IC0	06h	33	W		46h			ASB11CR2	86h	99	RW		C6h		
PRT1IC1	07h	34	W		47h			ASB11CR3	87h	100	RW		C7h		
PRT2DM0	08h	32	W		48h			ASA12CR0	88h	88	RW		C8h		
PRT2DM1	09h	33	W		49h			ASA12CR1	89h	90	RW		C9h		
PRT2IC0	0Ah	33	W		4Ah			ASA12CR2	8Ah	92	RW		CAh		
PRT2IC1	0Bh	34	W		4Bh			ASA12CR3	8Bh	93	RW		CBh		
PRT3DM0	0Ch	32	W		4Ch			ASB13CR0	8Ch	95	RW		CCh		
PRT3DM1	0Dh	33	W		4Dh			ASB13CR1	8Dh	97	RW		CDh		
PRT3IC0	0Eh	33	W		4Eh			ASB13CR2	8Eh	99	RW		CEh		
PRT3IC1	0Fh	34	W		4Fh			ASB13CR3	8Fh	100	RW		CFh		
PRT4DM0	10h	32	W		50h			ASB20CR0	90h	95	RW		D0h		
PRT4DM1	11h	33	W		51h			ASB20CR1	91h	97	RW		D1h		
PRT4IC0	12h	33	W		52h			ASB20CR2	92h	99	RW		D2h		
PRT4IC1	13h	34	W		53h			ASB20CR3	93h	100	RW		D3h		
PRT5DM0	14h	32	W		54h			ASA21CR0	94h	88	RW		D4h		
PRT5DM1	15h	33	W		55h			ASA21CR1	95h	90	RW		D5h		
PRT5IC0	16h	33	W		56h			ASA21CR2	96h	92	RW		D6h		
PRT5IC1	17h	34	W		57h			ASA21CR3	97h	93	RW		D7h		
Reserved	18h				58h			ASB22CR0	98h	95	RW		D8h		
	19h				59h			ASB22CR1	99h	97	RW		D9h		
	1Ah				5Ah			ASB22CR2	9Ah	99	RW		DAh		
	1Bh				5Bh			ASB22CR3	9Bh	100	RW		DBh		
	1Ch				5Ch			ASA23CR0	9Ch	88	RW		DCh		
	1Dh				5Dh			ASA23CR1	9Dh	90	RW		DDh		
	1Eh				5Eh			ASA23CR2	9Eh	92	RW		DEh		
	1Fh				5Fh			ASA23CR3	9Fh	93	RW		DFh		
DBA00FN	20h	50	RW	CLK_CR0	60h	76	RW	Reserved	A0h			OSC_CR0	E0h	40	RW
DBA00IN	21h	51	RW	CLK_CR1	61h	77	RW		A1h			OSC_CR1	E1h	40	RW
DBA00OU	22h	53	RW	ABF_CR	62h	106	W		A2h			Reserved	E2h		
Reserved	23h			AMD_CR	63h	107	RW		A3h			VLT_CR	E3h	118	RW
DBA01FN	24h	50	RW	Reserved	64h				A4h			Reserved	E4h		
DBA01IN	25h	51	RW		65h				A5h			Reserved	E5h		
DBA01OU	26h	53	RW		66h				A6h			Reserved	E6h		
Reserved	27h				67h				A7h			Reserved	E7h		
DBA02FN	28h	50	RW		68h				A8h			IMO_TR	E8h	35	W
DBA02IN	29h	51	RW		69h				A9h			ILO_TR	E9h	36	W
DBA02OU	2Ah	53	RW		6Ah				AAh			BDG_TR	EAh	120	W
Reserved	2Bh				6Bh				ABh			ECO_TR	EBh	37	W
DBA03FN	2Ch	50	RW		6Ch				ACh			Reserved	ECh		
DBA03IN	2Dh	51	RW		6Dh				ADh				EDh		
DBA03OU	2Eh	53	RW		6Eh				AEh				EEh		
Reserved	2Fh				6Fh				AFh				EFh		
DCA04FN	30h	50	RW		70h				B0h				F0h		
DCA04IN	31h	51	RW	ACA00CR0	71h	82	RW		B1h				F1h		
DCA04OU	32h	53	RW	ACA00CR1	72h	83	RW		B2h				F2h		
Reserved	33h			ACA00CR2	73h	84	RW		B3h				F3h		
DCA05FN	34h	50	RW	Reserved	74h				B4h				F4h		
DCA05IN	35h	51	RW	ACA01CR0	75h	82	RW		B5h				F5h		
DCA05OU	36h	53	RW	ACA01CR1	76h	83	RW		B6h				F6h		
Reserved	37h			ACA01CR2	77h	84	RW		B7h				F7h		
DCA06FN	38h	50	RW	Reserved	78h				B8h				F8h		
DCA06IN	39h	51	RW	ACA02CR0	79h	82	RW		B9h				F9h		
DCA06OU	3Ah	53	RW	ACA02CR1	7Ah	83	RW		BAh				FAh		
Reserved	3Bh			ACA02CR2	7Bh	84	RW		BBh				FBh		
DCA07FN	3Ch	50	RW	Reserved	7Ch				BCh				FCh		
DCA07IN	3Dh	51	RW	ACA03CR0	7Dh	82	RW		BDh				FDh		
DCA07OU	3Eh	53	RW	ACA03CR1	7Eh	83	RW		BEh				FEh		
Reserved	3Fh			ACA03CR2	7Fh	84	RW		BFh			CPU_SCR	FFh	114	[1]

1. Read/Write access is bit-specific or varies by function. See register.

6.3.4 Port Interrupt Control 1 Registers

Table 34: Port Interrupt Control 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	W	W
Bit Name	IC1 [7]	IC1 [6]	IC1 [5]	IC1 [4]	IC1 [3]	IC1 [2]	IC1 [1]	IC1 [0]
Bit [7:0]: **IC1 [7:0]** See truth table for Port Interrupt Control 0 Registers, above								

Port 0 Interrupt Control 1 Register (PRT0IC1, Address = Bank 1, 03h)
Port 1 Interrupt Control 1 Register (PRT1IC1, Address = Bank 1, 07h)
Port 2 Interrupt Control 1 Register (PRT2IC1, Address = Bank 1, 0Bh)
Port 3 Interrupt Control 1 Register (PRT3IC1, Address = Bank 1, 0Fh)
Port 4 Interrupt Control 1 Register (PRT4IC1, Address = Bank 1, 13h)
Port 5 Interrupt Control 1 Register (PRT5IC1, Address = Bank 1, 17h) **Note**: Port 5 is 4-bits wide

The following diagram shows the PSoC MCU Clock Tree of signals 48M through SLP:

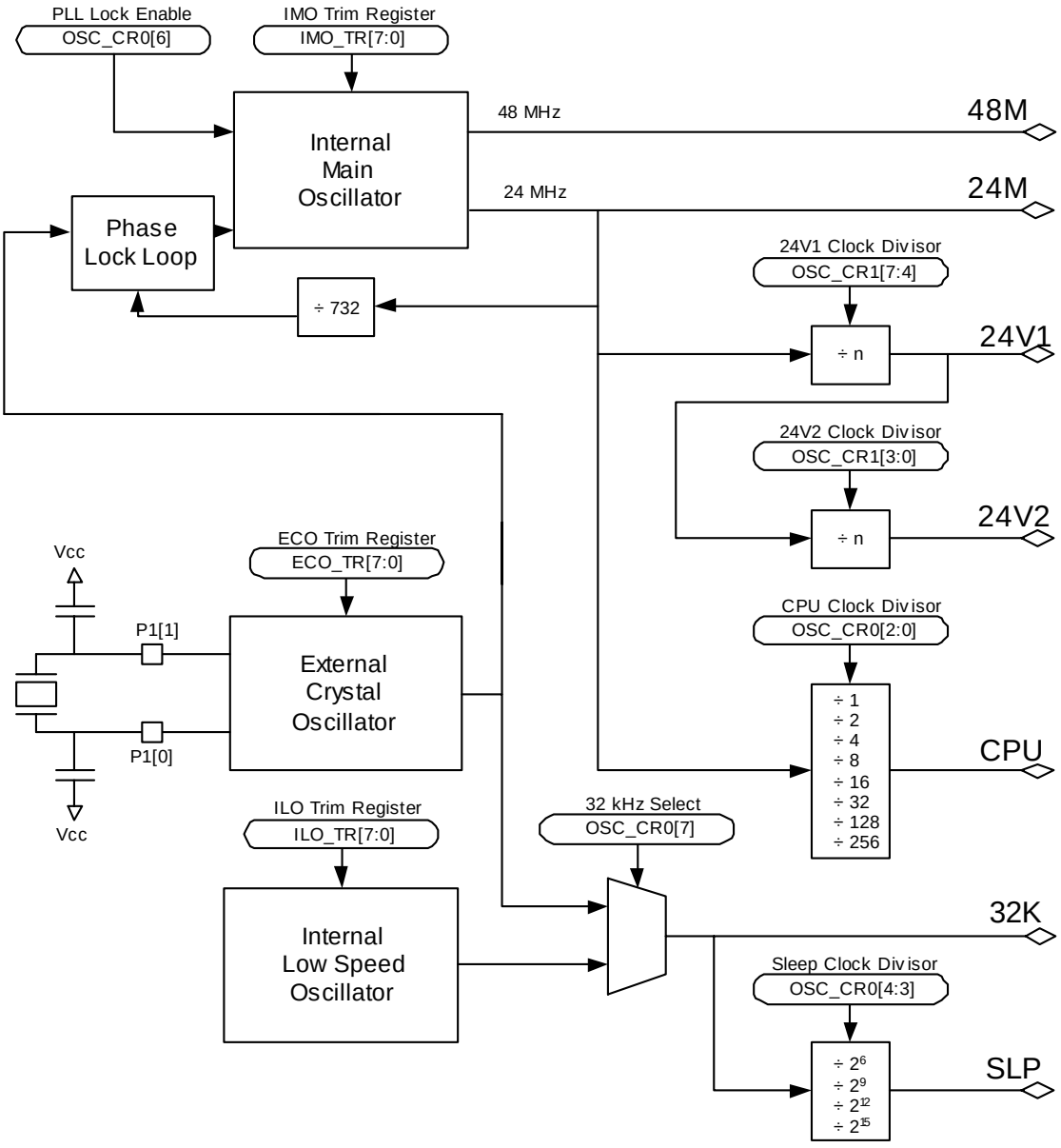

Figure 9: PSoC MCU Clock Tree of Signals

7.2.1 CPU and Sleep Timer Clock Options

The CPU is clocked off the **CPU** system-clocking signal, which can be configured to run at one of eight rates. This selection is independent from all other clock selection functions. It is completely safe for the CPU to change its clock rate without a timing hazard. The CPU clock period is determined by setting the CPU[2:0] bits in the Oscillator Control 0 Register (OSC_CR0).

The sleep timer is clocked off the **SLP** system-clocking signal. The SLEEP[1] and SLEEP[0] bits in the Oscillator Control 0 Register (OSC_CR0) allow the user to select from the four available periods.

7.2.3 Digital PSoC Block Clocking Options

All digital PSoC block clocks are a user-selectable choice of **48M**, **24V1**, **24V2**, or **32K**, as well as clocking signals from other digital PSoC blocks or general purpose I/O pins. There are a total of 16 possible clock options for each digital PSoC block. See the **Digital PSoC Block** section for details.

8.0 Interrupts

8.1 Overview

Interrupts can be generated by the General Purpose I/O lines, the Power monitor, the internal Sleep Timer, the eight Digital PSoC blocks, and the four analog columns. Every interrupt has a separate enable bit, which is contained in the General Interrupt Mask Register (INT_MSK0) and the Digital PSoC Block Interrupt Mask Register (INT_MSK1). When the user writes a “1” to a particular bit position, this enables the interrupt associated with that position. There is a single Global Interrupt Enable bit in the Flags Register (CPU_F), which can disable all interrupts, or enable those interrupts that also have their individual interrupt bit enabled. During a reset, the enable bits in the General Interrupt Mask Register (INT_MASK0), the enable bits in the Digital PSoC Block Interrupt Mask Register (INT_MSK1) and the Global Interrupt Enable bit in the Flags Register (CPU_F) are all cleared. The Interrupt Vector Register (INT_VC) holds the interrupt vector for the highest priority pending interrupt when read, and when written will clear all pending interrupts.

If there is only one interrupt pending and an instruction is executed that would mask that pending interrupt (by clearing the corresponding bit in either of the interrupt mask registers at address E0h or E1h in Bank 0), the CPU will take that interrupt. Since the pending interrupt has been cleared and there are no others, the resulting interrupt vector is 0000h and the CPU will jump to the user code at the beginning of Flash. To address this issue, use the macro defined in *m8c.inc* called "M8C_DisableIntMask" in PSoC Designer. This macro brackets the register write with a disable then an enable of global interrupts.

Digital Communications Type A Block 05 Function Register (DCA05FN, Address = Bank 1, 34h)
Digital Communications Type A Block 06 Function Register (DCA06FN, Address = Bank 1, 38h)
Digital Communications Type A Block 07 Function Register (DCA07FN, Address = Bank 1, 3Ch)

9.2.2 Digital Basic Type A / Communications Type A Block xx Input Register

The Digital Basic Type A / Communications Type A Block xx Input Register (DBA00IN-DCA07IN) consists of 4 bits [3:0] to select the block input clock and 4 bits [7:4] to select the primary data/enable input. The actual usage of the input data/enable is function dependent.

Table 48: Digital Basic Type A / Communications Type A Block xx Input Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [3]	Data [2]	Data [1]	Data [0]	Clock [3]	Clock [2]	Clock [1]	Clock [0]

Bit [7:4]: **Data [3:0] Data Enable Source Select**
0 0 0 0 = Data = 0
0 0 0 1 = Data = 1
0 0 1 0 = Digital Block 03
0 0 1 1 = Chain Function to Previous Block
0 1 0 0 = Analog Column Comparator 0
0 1 0 1 = Analog Column Comparator 1
0 1 1 0 = Analog Column Comparator 2
0 1 1 1 = Analog Column Comparator 3
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Bit [3:0]: **Clock [3:0] Clock Source Select**
0 0 0 0 = Clock Disabled
0 0 0 1 = Global Output[4] (for Digital Blocks 00 to 03) **or** Global Output[0] (for Digital Blocks 04 to 07)
0 0 1 0 = Digital Block 03 (Primary Output)
0 0 1 1 = Previous Digital PSoC block (Primary Output)
0 1 0 0 = 48M
0 1 0 1 = 24V1
0 1 1 0 = 24V2
0 1 1 1 = 32k
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Digital Basic Type A Block 00 Input Register (DBA00IN, Address = Bank 1, 21h)
Digital Basic Type A Block 01 Input Register (DBA01IN, Address = Bank 1, 25h)
Digital Basic Type A Block 02 Input Register (DBA02IN, Address = Bank 1, 29h)
Digital Basic Type A Block 03 Input Register (DBA03IN, Address = Bank 1, 2Dh)
Digital Communications Type A Block 04 Input Register (DCA04IN, Address = Bank 1, 31h)
Digital Communications Type A Block 05 Input Register (DCA05IN, Address = Bank 1, 35h)

trigger capture operations that permit calculation of elapsed “ticks.” Timer-configured PSoC blocks may be chained to arbitrary lengths in 8 bit increments.

9.5.1.2 Registers

Data Register 1 establishes the period or integer clock division value. Data Register 0 holds the current state of the down counter. If the function is disabled, writing a period into Data Register 1, will automatically load Data Register 0. It is also automatically reloaded on the clock cycle after it reaches zero, the terminal count value. When a capture event occurs, the current value of Data Register 0 is transferred to Data Register 2. The captured value in Data Register 2 may then be read by the CPU. In addition to the hardware capture input, A CPU read of Data Register 0 generates a software capture event. This read will return 0 as data. A subsequent read of Data Register 2 will return the captured value. Control Register 0 contains one bit to enable/disable the function.

9.5.1.3 Inputs

There are two inputs, the Source Clock and the Hardware Capture signal. The down counter is decremented on the rising-edge of the Source Clock. A hardware capture event is signaled by a rising edge of the Hardware Capture signal. This is synchronized to the 24 MHz system clock and the data is synchronously transferred to Data Register 2. The Hardware Capture Signal is OR’ed with a software capture signal that is generated when Data Register 0 is read directly by the CPU. In order to use the software capture mechanism, the Hardware Capture signal input selection must be low. The multiplexers selecting these input sources are controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.1.4 Outputs

The Terminal Count signal is the primary output and it exhibits a duty cycle that is the reciprocal of the period value contained in Data Register 1. In other words, it is high during the source clock cycle when the value in Data Register 0 is zero and low otherwise. The Terminal Count can be routed to additional analog or digital PSoC blocks or via Global Output lines. The auxiliary output is the Compare True signal. This output is high when the current count is less than (or less than or equal to) the value in Data Register 2 (compare type controlled by Mode[1] in the PSoC block Function Register). The auxiliary output can be routed via Global Output lines. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.1.5 Interrupts

Interrupts may be generated in either of two ways. First, the PSoC block may optionally generate an interrupt on the rising edge of Terminal Count or the rising edge of the Compare True signal. The selection of interrupt source is determined by the MODE[0] bit of the PSoC block Function Register (DBA00FN-DCA07FN). The MODE[1] bit controls whether the comparison operation is “less than” or “less than or equal to.” If capture events are disabled, Data Register 2 can be used to create a periodic interrupt with a particular offset from the terminal count.

9.5.1.6 Usage Notes

1. Constraints

   Hardware/software synchronous capture is only available with a clocking rate of 24 MHz and below.

2. Software Capture

   When a capture event occurs, all bytes in a multi-byte timer transfer simultaneously from the current count (Data Register 0) to the capture register (Data Register 2). To generate a software capture event, only the least significant Data Register 0 byte needs to be read by the CPU. This causes the same simultaneous transfer as a hardware event.

3. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 1 (Period) is loaded directly into Data Register 0 (Counter) to initialize or reset the count. All outputs are low and the block interrupt is held low. Disabling a timer does not affect the current count value and it may be read by the CPU. However, since hardware/software capture is disabled in this state, two reads are required to read each byte of a multi-byte register. One to transfer each Data Register 0 count value to the associated Data Register 2 capture register, then one to read the result in Data Register 2.

2. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 1 (Period) is loaded directly into Data Register 0 (Counter) to initialize or reset the count. All outputs are low and the block interrupt is held low. Disabling a counter does not affect the current count value and it may be read by the CPU. Two reads are required to read each byte of a multi-byte register. One to transfer each Data Register 0 count value to the associated Data Register 2 capture register, then one to read the result in Data Register 2.

3. Reading the Count Value

   A CPU read of Data Register 0 (count value) will overwrite Data Register 2 (compare value). Therefore, when reading the current count, a previously written compare value will be overwritten.

4. Extra Count

   In a Counter User Module, the data input is an enable for counting. Normally, when the enable goes low, the counter will hold the current count. However, if the enable happens to go low in the same clock period as Terminal Count (count of all 0's), one additional count will occur that will reload the counter from the Period Register. Once the counter is reloaded from the Period Register, counting will stop.

9.5.3 Deadband Generator

9.5.3.1 Summary

The Deadband function produces two output waveforms, F0 and F1, with the same frequency as the input, but “under-lapped” so they are never both high at the same time. An 8-bit down counter controls the length of the “dead time” during which both output signals are low. When the deadband function detects a rising edge on the input waveform, the F1 output signal goes low and the counter decrements from its initial value to its terminal count. When the down counter reaches zero, the F0 output signal goes high. The process reverses on the falling edge of the input waveform so that after the same dead time, F1 goes high until the input signal transitions again. Dead-band generator PSoC blocks cannot be chained to increase the width of the down counter beyond 8 bits or 256 dead-time “ticks.”

9.5.3.2 Registers

Data Register 1 stores the count that controls the elapsed dead time. Data Register 0 holds the current state of the dead-time down counter. If the function is disabled, writing a period into Data Register 1, will automatically load Data Register 0 with the deadband period. This period is automatically re-loaded into the counter on each edge of the input signal. Data Register 2 is unused. Control Register 0 contains one bit to enable/disable the function.

9.5.3.3 Inputs

The input controls the period and duty cycle of the dead-band generator outputs. This input is fixed to be derived from the primary output of the previous block. If this signal is pulse-width modulated, i.e., if a PWM block is configured as the previous block, the dead-band outputs will be similarly modulated. The F0 output corresponds to the duty cycle of the input (less the dead time) and F1 to the duty cycle of the inverted input (again, less the dead time). The clock input to the dead-band generator controls the rate at which the down counter is decremented. The primary data input is the “Kill” Signal. When this signal is asserted high, both F0 and F1 outputs will go low. The multiplexers selecting these input are controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.3.4 Outputs

Both the F0 and F1 outputs can be driven onto the Global Output bus. If the next PSoC block selects “Previous PSoC block” for its clock input, it only “sees” the F0 output of the dead-band function. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.3.5 Interrupts

The rising edge of the F0 signal provides the interrupt for this block.

9.5.3.6 Usage Notes

1. Constraints

   The dead time must not exceed the minimum of the input signal’s pulse-width high and pulse-width low time, less two CPU clocks. Dead time equals the period of the input clock times one plus the value written to Data Register 1.

only be input from GPIO input pins (Global Input Bus). There is no way to enable the SS_internally. In SPI modes 2 & 3, where SS is not required between each byte, the external pin may be grounded.

Important: The AUX Out Enable bit (bit 5) of the Output Register (DCA04OU-DCA07OU) must be set to 0 to disable it.

9.5.9.4 Outputs

The function output is the MISO (master-in, slave-out) signal, which may be driven on the Global Output bus and is selected by Output Register (DCA04OU-DCA07OU).

9.5.9.5 Interrupts

When enabled, the function generates an interrupt on RX Reg Full status (Data Register 2 full). If Mode[1] of the Function Register is set, the interrupt will be generated on SPI Complete status.

9.5.9.6 Usage Notes

1. Reading the Status

   Reading Control Register 0, which contains the status bits, automatically resets the status bits to 0 with the exception of TX Reg Empty, which is cleared when a byte is written to the TX Data Register (Data Register 1), and the RX Reg Full, which is cleared when a byte is read from the RX Data Register (Data Register 2).

2. Multi-Slave Environment

   The SS_ signal does not have any affect on the output from the slave. The output of the slave at the end of a reception/transmission is always the first bit sent (the MSB, unless LSBF option is selected, then it's the LSB). To implement a multi-slave environment, a GPIO interrupt may be configured on the SS_ input, and the Slave output strength may be toggled between driving and High Z in firmware.

3. Using Interrupts

   RX Reg Full status or SPI Complete status generates an interrupt. Executing the interrupt routine does not automatically clear status. If SPI Complete is selected as the interrupt source, Control Register 0 (status) must be read in the interrupt routine to clear the status. If RX Reg Full status is selected, a byte must be read from the RX Data Register (Data Register 2) to clear the status. If the interrupting status is not cleared further interrupts will be suppressed.

4. Synchronization of CPU Interaction

   Because the SPI Slave is clocked asynchronously by the master SCLK, transfer of data between the TX Register to shifter and shifter to RX Register occurs asynchronously.

   Either polling or interrupts can be used to detect that a byte has been received and is ready to read. However, on the TX side, the user is responsible for implementing a protocol that ensures there is enough set-up time from the TX Data Register write to the first clock (mode 2, 3) or SS_ (mode 0, 1) from the master.

10.8.2.3 ACMux

The ACMux, as shown in Analog Switch Cap Type A Block xx Control 1 Register, controls the input muxing for both the A and C capacitor branches. The high order bit, ACMux[2], selects one of two inputs for the C branch. However, when the bit is high, it also overrides the two low order bits, forcing the A and C branches to the same source. The resulting condition is used to construct low pass biquad filters. See the individual AMux and CMux diagrams.

10.8.2.4 BMuxSCA/SCB

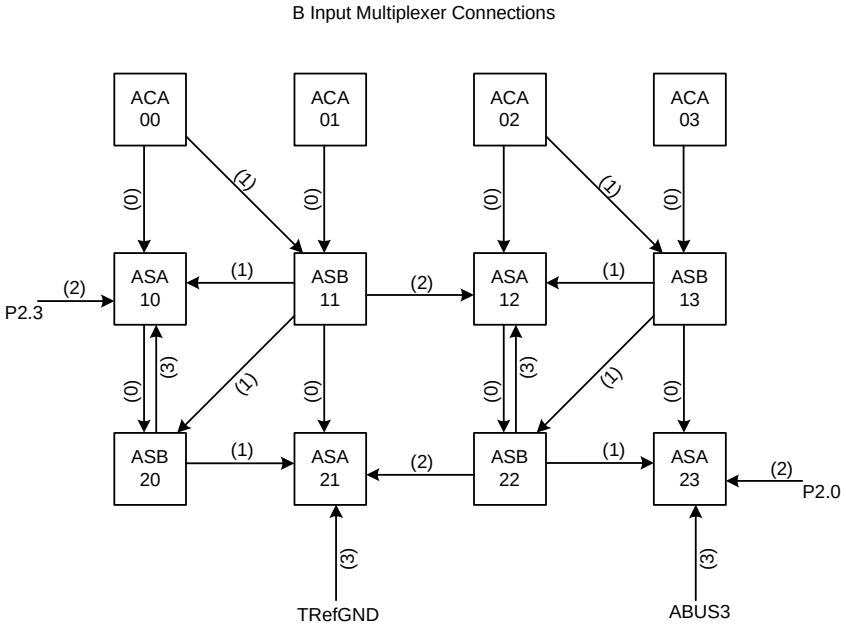

Figure 25: BMuxSCA/SCB Connections

10.8.3 Registers

10.8.3.1 Analog Switch Cap Type A Block xx Control 0 Register

FCap controls the size of the switched feedback capacitor in the integrator.

ClockPhase controls the internal clock phasing relative to the input clock phasing. ClockPhase affects the output of the analog column bus which is controlled by the AnalogBus bit in Control 2 Register (ASA10CR2, ASA12CR2, ASA21CR2, ASA23CR2).

ASign controls the switch phasing of the switches on the bottom plate of the ACap capacitor. The bottom plate samples the input or the reference.

The ACap bits set the value of the capacitor in the A path.

Table 69: Analog Switch Cap Type A Block xx Control 0 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	FCap	ClockPhase	ASign	ACap[4]	ACap[3]	ACap[2]	ACap[1]	ACap[0]

10.8.3.4 Analog Switch Cap Type A Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASA10CR2, ASA12CR2, ASA21CR2, ASA23CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BMuxSCA controls the muxing to the input of the B capacitor branch.

Power – encoding for selecting 1 of 4 power levels. The block always powers up in the off state.

Table 72: Analog Switch Cap Type A Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BMuxSCA[1]	BMuxSCA[0]	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
1 = If the FSW1 bit is set to 1, the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit [3:2] BMuxSCA [1:0] Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block.)

ASA10	ASA21	ASA12	ASA23
0 0 = ACA00	ASB11	ACA02	ASB13
0 1 = ASB11	ASB20	ASB13	ASB22
1 0 = P2.3	ASB22	ASB11	P2.0
1 1 = ASB20	T_{ref}GND	ASB22	ABUS3

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type A Block 10 Control 3 Register (ASA10CR3, Address = Bank 0/1, 83h)
Analog Switch Cap Type A Block 12 Control 3 Register (ASA12CR3, Address = Bank 0/1, 8Bh)
Analog Switch Cap Type A Block 21 Control 3 Register (ASA21CR3, Address = Bank 0/1, 97h)
Analog Switch Cap Type A Block 23 Control 3 Register (ASA23CR3, Address = Bank 0/1, 9Fh)

10.12 Analog I/O

10.12.1 Analog Input Muxing

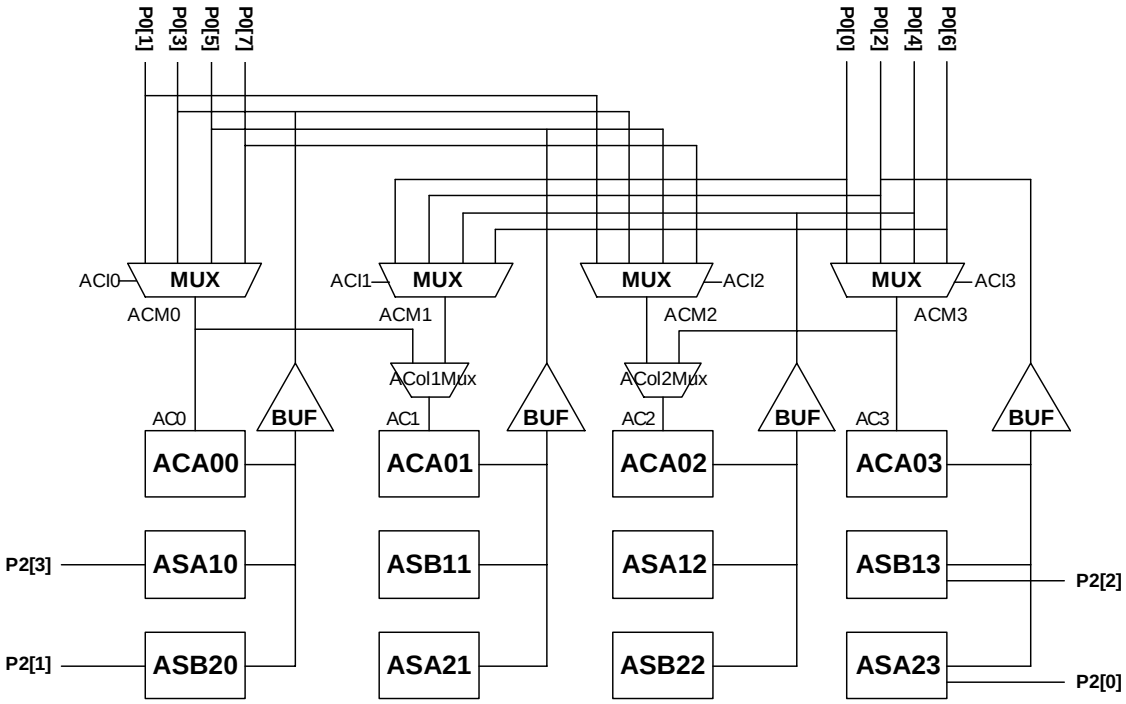

Figure 27: Analog Input Muxing

10.12.2 Analog Input Select Register

This register controls the analog muxes that feed signals in from port pins into each Analog Column. Each of the Analog Columns can have up to four port bits connected to its muxed input. Analog Columns 01 and 02 (ACI1 and ACI2) have additional muxes that allow selection between separate column multiplexers (see Analog Input Muxing diagram above). The AC1Mux and AC2Mux bit fields control the bits for those muxes and are located in the Analog Output Buffer Control Register (ABF_CR). There are four additional analog inputs that go directly into the Switch Capacitor PSoC blocks.

11.0 Special Features of the CPU

11.1 Multiplier/Accumulator

A fast, on-chip signed 2's complement MAC (Multiply/Accumulate) function is provided to assist the main CPU with digital signal processing applications. Multiply results, as well as the lower 2 bytes of the Accumulator, are available immediately after the input registers are written. The upper 2 bytes require a single instruction delay before reading. The MAC function is tied directly on the internal data bus, and is mapped into the register space. The following MAC block diagram provides data flow information. The user has the choice to either cause a multiply/accumulate function to take place, or a multiply only function. The user selects which operation is performed by the choice of input register. The multiply function occurs immediately whenever the MUL_X or the MUL_Y multiplier input registers are written, and the result is available in the MUL_DH and MUL_DL multiplier result registers. The Multiply/Accumulate function is executed whenever there is a write to the MAC_X or the MAC_Y Multiply/Accumulate input registers, and the result is available in the ACC_DR3, ACC_DR2, ACC_DR1, and ACC_DR0 accumulator result registers. A write to MUL_X or MAC_X is input as the X value to both the multiply and Multiply/Accumulate functions. A write to MUL_Y or MAC_Y is input as the Y value to both the multiply and Multiply/Accumulate functions. A write to the MAC_CL0 or MAC_CL1 registers will clear the value in the four accumulate registers.

Operation of the Multiply/Accumulate function relies on proper multiplicand input. The first value of each multiplicand must be placed into MUL_X (or MUL_Y) register to avoid causing a Multiply/Accumulate to occur. The second multiplicand must be placed into MAC_Y (or MAC_X) thereby triggering the Multiply/Accumulate function.

MUL_X, MUL_Y, MAC_X, and MAC_Y are 8-bit signed input registers. MUL_DL and MUL_DH form a 16-bit signed output. ACC_DR0, ACC_DR1, ACC_DR2 and ACC_DR3 form a 32-bit signed output.

An extra instruction must be inserted between the following sequences of MAC operations to provide extra delay. If this is not done, the Accumulator results will be inaccurate.

a. Two MAC instructions in succession:

```
mov reg[MAC_X],a
nop //add nop or any other instruction
mov reg[MAC_X],a
```

For sequence a., there is no workaround, the nop or other instruction must be inserted.

b. A MAC instruction followed by a read of the most significant Accumulator bytes:

```
mov reg[MAC_X],a
nop //add nop or any other instruction
mov a,[ACC_DR2] // or ACC_DR3
```

For sequence b., the least significant Accumulator bytes (ACC_DR0, ACC_DR1) may be reliably read directly after the MAC instruction.

Writing to the multiplier registers (MUL_X, MUL_Y), and reading the result back from the multiplier product registers (MUL_DH, MUL_DL), is not affected by this problem and does not have any restrictions.

13.2.1 DC Operational Amplifier Specifications

13.2.1.1 5V Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and -40°C <= T_A <= 85°C. The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switch Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only. For 3.3V operation, see Table 106 on page 131.

Table 105: 5V DC Operational Amplifier Specifications

Symbol	5V DC Operational Amplifier Specifications	Minimum	Typical	Maximum	Unit
	Input Offset Voltage (Absolute Value)	-	7	30	mV
	Average Input Offset Voltage Drift	-	+24	-	µV/°C
	Input Leakage Current[1]	-	3	1000	nA
	Input Capacitance[2]	.30	.34	.40	pF
	Common Mode Voltage Range[3]	.5	-	V_{cc} - 1.0	VDC
	Common Mode Rejection Ratio	80	-	-	dB
	Open Loop Gain	80	-	-	dB
	High Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 V_{cc} - .4 V_{cc} - .4 V_{cc} - .4	 - - -	 - - -	 V V V
	Low Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 - - -	 - - -	 0.1 0.1 0.1	 V V V
	Supply Current (Including Associated AGND Buffer) Bias = Low Bias = Medium Bias = High	 - - -	 125 280 760	 300 600 1500	 µA µA µA
	Supply Voltage Rejection Ratio	60	-	-	dB

1. The leakage current includes the Analog Continuous Time PSoC block mux and the analog input mux. The leakage related to the General Purpose I/O pins is not included here.
2. The Input Capacitance includes the Analog Continuous Time PSoC block mux and the analog input mux. The capacitance of the General Purpose I/O pins is not included here.
3. The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.

13.2.5 Switch Mode Pump Specifications

Table 111: DC Switch Mode Pump Specifications

Symbol	DC Switch Mode Pump Specifications	Minimum	Typical	Maximum	Unit
	Output Voltage[1]	3.07	-	5.15	V
	Available Output Current V_i = 1.5 V, V_o = 3.25 V V_i = 1.5 V, V_o = 5.0 V	 8[2] 5	 - -	 - -	 mA mA
	Short Circuit Current (V_i = 3.3 V)	-	12	-	mA
	Input Voltage Range (During sustained operation)	1.0	-	3.3	V
	Minimum Input Voltage to Start Pump	1.1	1.2	-	
	Output Voltage Tolerance (Over V_i Range)	-	5	-	%V_o
	Line Regulation (Over V_i Range)	-	5	-	%V_o
	Load Regulation	-	5	-	%V_o
	Output Voltage Ripple (Depends on capacitor and load)	-	25[3]	-	mV_{pp}
	Transient Response 50% Load Change to 5% error envelope V_o Over/Undershoot for 50% Load Change	 - -	 1 1	 - -	 µs %V_o
	Efficiency	35[4]	50	-	%
	Switching Frequency	-	1.3	-	MHz
	Switching Duty Cycle	-	50	-	%

1. Average, neglecting ripple.
2. For implementation, which includes 2 µH inductor, 1 µF capacitor, and Schottkey diode. Performance is significantly a function of external components. Specifications guaranteed for inductors with series resistance less than 0.1 W, with a current rating of > 250 mA, a capacitor with less than 1µA leakage at 5V, and Schottkey diode with less than 0.6V of drop at 50 mA.
3. Configuration of note 2. Load is 5 mA.
4. Configuration of note 2. Load is 5 mA. V_{out} is 3.25V.

Table 113: 3.3V DC Analog Reference Specifications

Symbol	3.3V DC Analog Reference Specifications	Minimum	Typical	Maximum	Unit
	AGND = Vcc/2 [1] CT Block Bias = High	Vcc/2 - 0.007	Vcc/2 - 0.003	Vcc/2 + 0.002	V
	AGND = 2*BandGap[1] CT Block Bias = High	Not Allowed			
	AGND = P2[4] (P2[4] = Vcc/2) CT Block Bias = High	P24 - 0.008	P24 + 0.001	P24 + 0.009	V
	AGND Column to Column Variation (AGND=Vcc/2)[1] CT Block Bias = High	-0.034	0.000	0.034	mV
	REFHI = Vcc/2 + BandGap Ref Control Bias = High	Not Allowed			
	REFHI = 3*BandGap Ref Control Bias = High	Not Allowed			
	REFHI = 2*BandGap + P2[6] (P2[6] = 0.5V) Ref Control Bias = High	Not Allowed			
	REFHI = P2[4] + BandGap (P2[4] = Vcc/2) Ref Control Bias = High	Not Allowed			
	REFHI = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V) Ref Control Bias = High	P2[4]+P2[6] - 0.075	P2[4]+P2[6] - 0.009	P2[4]+P2[6]+ 0.057	V
	REFLO = Vcc/2 - BandGap Ref Control Bias = High	Not Allowed			
	REFLO = BandGap Ref Control Bias = High	Not Allowed			
	REFLO = 2*BandGap - P2[6] (P2[6] = 0.5V) Ref Control Bias = High	Not Allowed			
	REFLO = P2[4] – BandGap (P2[4] = Vcc/2) Ref Control Bias = High	Not Allowed			
	REFLO = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V) Ref Control Bias = High	P2[4]-P2[6] - 0.048	P24-P26 + 0.022	P2[4]-P2[6] + 0.092	V

1. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

13.2.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications include both voltage ranges, 5V +/- 5% and 3.3V +/- 10% and the temperature range -40°C <= T_A <= 85°C. Typical parameters apply to 3.3V and 5V at 25°C and are for design guidance only.

Table 114: DC Analog PSoC Block Specifications

Symbol	DC Analog PSoC Block Specifications	Minimum	Typical	Maximum	Unit
	Resistor Unit Value (Continuous Time)	-	45	-	kΩ
	Capacitor Unit Value (Switch Cap)	-	70	-	fF

Table 120: 3.3V AC Analog Output Buffer Specifications

Symbol	3.3V AC Analog Output Buffer Specifications	Minimum	Typical	Maximum	Unit
	Rising Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	3.2	µs
	Bias = High	-	-	3.2	µs
	Falling Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.6	µs
	Bias = High	-	-	2.6	µs
	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load				
	Bias = Low	.5	-	-	V/µs
	Bias = High	.5	-	-	V/µs
	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load				
	Bias = Low	.5	-	-	V/µs
	Bias = High	.5	-	-	V/µs
	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load				
	Bias = Low	1.3	-	-	MHz
	Bias = High	1.3	-	-	MHz
	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load				
	Bias = Low	360	-	-	kHz
	Bias = High	360	-	-	kHz

13.3.3 AC Programming Specifications

Table 121: AC Programming Specifications

Symbol	AC Programming Specifications	Minimum	Typical	Maximum	Unit
T_{rsclk}	Rise Time of SCLK	1	-	20	ns
T_{fsclk}	Fall Time of SCLK	1	-	20	ns
T_{ssclk}	Data Set up Time to Rising Edge of SCLK	25	-	-	ns
T_{hsclk}	Data Hold Time from Rising Edge of SCLK	25	-	-	ns
F_{sclk}	Frequency of SCLK	2	-	20	MHz
T_{eraseb}	Flash Erase Time (Block)	-	10	-	ms
T_{erasef}	Flash Erase Time (Full)	-	40	-	ms
T_{write}	Flash Block Write Time	2	10	20	ms