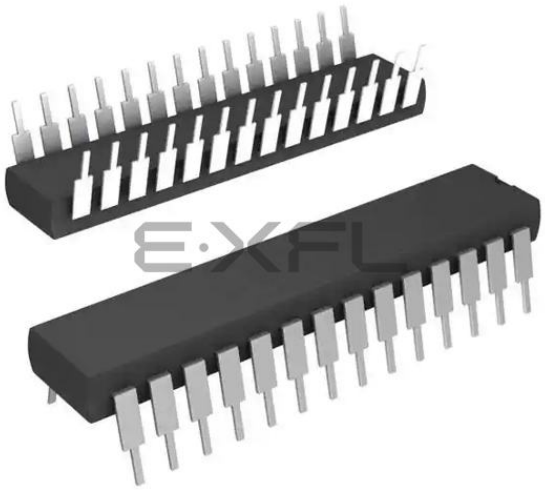

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Peripherals	LVD, POR, PWM, WDT
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Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
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Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26443-24pi

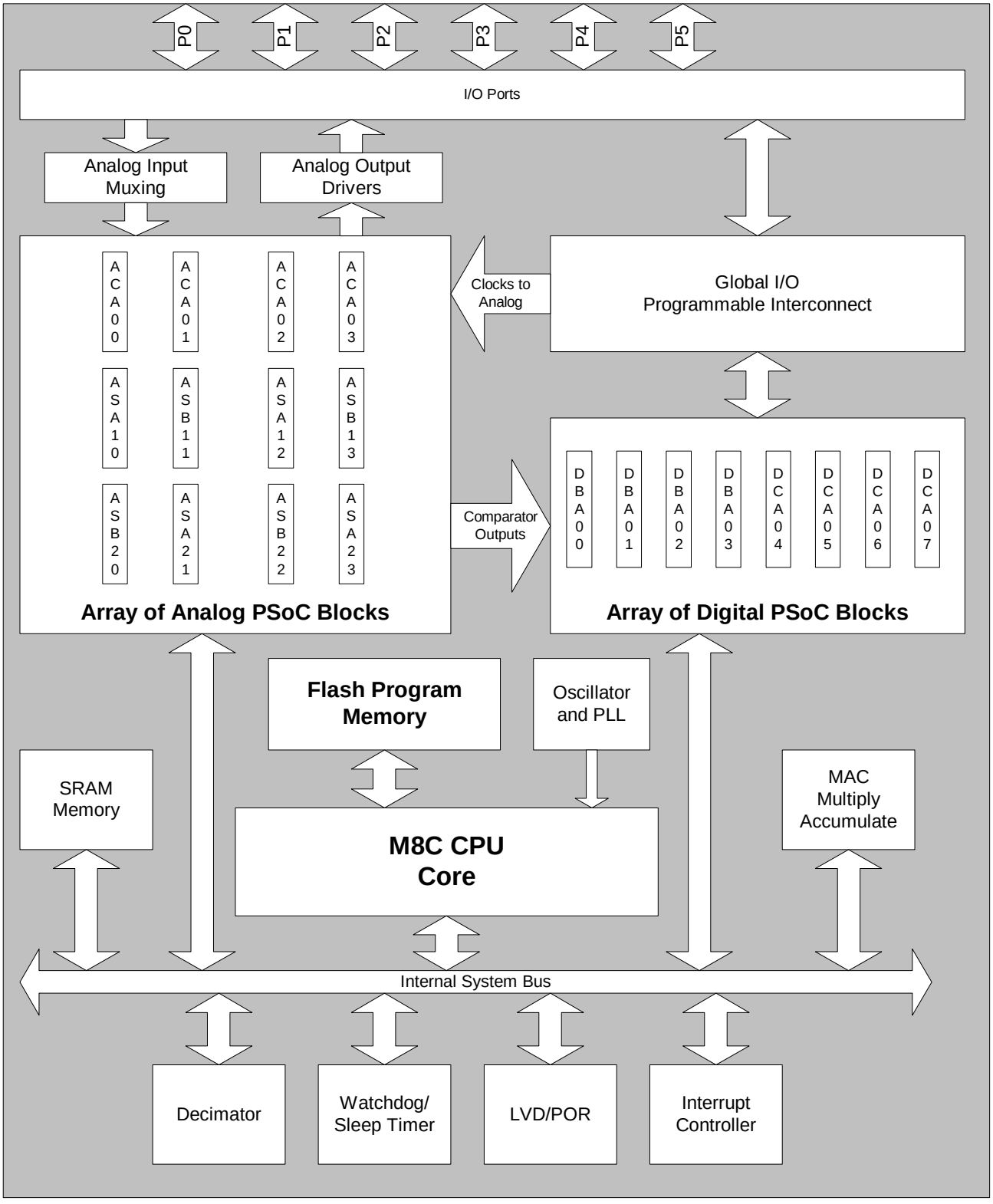

Figure 1: Block Diagram

2.2 CPU Registers

2.2.1 Flags Register

The Flags Register can only be set or reset with logical instruction.

Table 8: Flags Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	1	0
Read/ Write	--	--	--	RW	R	RW	RW	RW
Bit Name	Reserved	Reserved	Reserved	XIO	Super	Carry	Zero	Global IE

Bit 7: **Reserved**
Bit 6: **Reserved**
Bit 5: **Reserved**

Bit 4: **XIO** Set by the user to select between the register banks
0 = Bank 0
1 = Bank 1

Bit 3: **Super** Indicates whether the CPU is executing user code or Supervisor Code. (This code cannot be accessed directly by the user and is not displayed in the ICE debugger.)
0 = User Code
1 = Supervisor Code

Bit 2: **Carry** Set by CPU to indicate whether there has been a carry in the previous logical/arithmetic operation
0 = No Carry
1 = Carry

Bit 1: **Zero** Set by CPU to indicate whether there has been a zero result in the previous logical/arithmetic operation
0 = Not Equal to Zero
1 = Equal to Zero

Bit 0: **Global IE** Determines whether all interrupts are enabled or disabled
0 = Disabled
1 = Enabled

2.2.2 Accumulator Register

Table 9: Accumulator Register (CPU_A)

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]	System[1]
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]** 8-bit data value holds the result of any logical/arithmetic instruction that uses a source addressing mode

1. System - not directly accessible by the user

4.3 Register Bank 1 Map

Table 27: Bank 1

Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access	Register Name	Address	Data Sheet Page	Access
PRT0DM0	00h	32	W	Reserved	40h			ASA10CR0	80h	88	RW	Reserved	C0h		
PRT0DM1	01h	33	W		41h			ASA10CR1	81h	90	RW		C1h		
PRT0IC0	02h	33	W		42h			ASA10CR2	82h	92	RW		C2h		
PRT0IC1	03h	34	W		43h			ASA10CR3	83h	93	RW		C3h		
PRT1DM0	04h	32	W		44h			ASB11CR0	84h	95	RW		C4h		
PRT1DM1	05h	33	W		45h			ASB11CR1	85h	97	RW		C5h		
PRT1IC0	06h	33	W		46h			ASB11CR2	86h	99	RW		C6h		
PRT1IC1	07h	34	W		47h			ASB11CR3	87h	100	RW		C7h		
PRT2DM0	08h	32	W		48h			ASA12CR0	88h	88	RW		C8h		
PRT2DM1	09h	33	W		49h			ASA12CR1	89h	90	RW		C9h		
PRT2IC0	0Ah	33	W		4Ah			ASA12CR2	8Ah	92	RW		CAh		
PRT2IC1	0Bh	34	W		4Bh			ASA12CR3	8Bh	93	RW		CBh		
PRT3DM0	0Ch	32	W		4Ch			ASB13CR0	8Ch	95	RW		CCh		
PRT3DM1	0Dh	33	W		4Dh			ASB13CR1	8Dh	97	RW		CDh		
PRT3IC0	0Eh	33	W		4Eh			ASB13CR2	8Eh	99	RW		CEh		
PRT3IC1	0Fh	34	W		4Fh			ASB13CR3	8Fh	100	RW		CFh		
PRT4DM0	10h	32	W		50h			ASB20CR0	90h	95	RW		D0h		
PRT4DM1	11h	33	W		51h			ASB20CR1	91h	97	RW		D1h		
PRT4IC0	12h	33	W		52h			ASB20CR2	92h	99	RW		D2h		
PRT4IC1	13h	34	W		53h			ASB20CR3	93h	100	RW		D3h		
PRT5DM0	14h	32	W		54h			ASA21CR0	94h	88	RW		D4h		
PRT5DM1	15h	33	W		55h			ASA21CR1	95h	90	RW		D5h		
PRT5IC0	16h	33	W		56h			ASA21CR2	96h	92	RW		D6h		
PRT5IC1	17h	34	W		57h			ASA21CR3	97h	93	RW		D7h		
Reserved	18h				58h			ASB22CR0	98h	95	RW		D8h		
	19h				59h			ASB22CR1	99h	97	RW		D9h		
	1Ah				5Ah			ASB22CR2	9Ah	99	RW		DAh		
	1Bh				5Bh			ASB22CR3	9Bh	100	RW		DBh		
	1Ch				5Ch			ASA23CR0	9Ch	88	RW		DCh		
	1Dh				5Dh			ASA23CR1	9Dh	90	RW		DDh		
	1Eh				5Eh			ASA23CR2	9Eh	92	RW		DEh		
	1Fh				5Fh			ASA23CR3	9Fh	93	RW		DFh		
DBA00FN	20h	50	RW	CLK_CR0	60h	76	RW	Reserved	A0h			OSC_CR0	E0h	40	RW
DBA00IN	21h	51	RW	CLK_CR1	61h	77	RW		A1h			OSC_CR1	E1h	40	RW
DBA00OU	22h	53	RW	ABF_CR	62h	106	W		A2h			Reserved	E2h		
Reserved	23h			AMD_CR	63h	107	RW		A3h			VLT_CR	E3h	118	RW
DBA01FN	24h	50	RW	Reserved	64h				A4h			Reserved	E4h		
DBA01IN	25h	51	RW		65h				A5h			Reserved	E5h		
DBA01OU	26h	53	RW		66h				A6h			Reserved	E6h		
Reserved	27h				67h				A7h			Reserved	E7h		
DBA02FN	28h	50	RW		68h				A8h			IMO_TR	E8h	35	W
DBA02IN	29h	51	RW		69h				A9h			ILO_TR	E9h	36	W
DBA02OU	2Ah	53	RW		6Ah				AAh			BDG_TR	EAh	120	W
Reserved	2Bh				6Bh				ABh			ECO_TR	EBh	37	W
DBA03FN	2Ch	50	RW		6Ch				ACh			Reserved	ECh		
DBA03IN	2Dh	51	RW		6Dh				ADh				EDh		
DBA03OU	2Eh	53	RW		6Eh				AEh				EEh		
Reserved	2Fh				6Fh				AFh				EFh		
DCA04FN	30h	50	RW		70h				B0h				F0h		
DCA04IN	31h	51	RW	ACA00CR0	71h	82	RW		B1h				F1h		
DCA04OU	32h	53	RW	ACA00CR1	72h	83	RW		B2h				F2h		
Reserved	33h			ACA00CR2	73h	84	RW		B3h				F3h		
DCA05FN	34h	50	RW	Reserved	74h				B4h				F4h		
DCA05IN	35h	51	RW	ACA01CR0	75h	82	RW		B5h				F5h		
DCA05OU	36h	53	RW	ACA01CR1	76h	83	RW		B6h				F6h		
Reserved	37h			ACA01CR2	77h	84	RW		B7h				F7h		
DCA06FN	38h	50	RW	Reserved	78h				B8h				F8h		
DCA06IN	39h	51	RW	ACA02CR0	79h	82	RW		B9h				F9h		
DCA06OU	3Ah	53	RW	ACA02CR1	7Ah	83	RW		BAh				FAh		
Reserved	3Bh			ACA02CR2	7Bh	84	RW		BBh				FBh		
DCA07FN	3Ch	50	RW	Reserved	7Ch				BCh				FCh		
DCA07IN	3Dh	51	RW	ACA03CR0	7Dh	82	RW		BDh				FDh		
DCA07OU	3Eh	53	RW	ACA03CR1	7Eh	83	RW		BEh				FEh		
Reserved	3Fh			ACA03CR2	7Fh	84	RW		BFh			CPU_SCR	FFh	114	[1]

1. Read/Write access is bit-specific or varies by function. See register.

6.3.4 Port Interrupt Control 1 Registers

Table 34: Port Interrupt Control 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	W	W
Bit Name	IC1 [7]	IC1 [6]	IC1 [5]	IC1 [4]	IC1 [3]	IC1 [2]	IC1 [1]	IC1 [0]
Bit [7:0]: **IC1 [7:0]** See truth table for Port Interrupt Control 0 Registers, above								

Port 0 Interrupt Control 1 Register (PRT0IC1, Address = Bank 1, 03h)
Port 1 Interrupt Control 1 Register (PRT1IC1, Address = Bank 1, 07h)
Port 2 Interrupt Control 1 Register (PRT2IC1, Address = Bank 1, 0Bh)
Port 3 Interrupt Control 1 Register (PRT3IC1, Address = Bank 1, 0Fh)
Port 4 Interrupt Control 1 Register (PRT4IC1, Address = Bank 1, 13h)
Port 5 Interrupt Control 1 Register (PRT5IC1, Address = Bank 1, 17h) **Note**: Port 5 is 4-bits wide

8.2 Interrupt Control Architecture

The interrupt controller contains a separate flip-flop for each interrupt. When an interrupt is generated, it is registered as a pending interrupt. It will stay pending until it is serviced, a reset occurs, or there is a write to the INT_VC Register. A pending interrupt will only generate an interrupt request when enabled by the appropriate mask bit in the Digital PSoC Block Interrupt Mask Register (INT_MSK1) or General Interrupt Mask Register (INT_MSK0), and the Global IE bit in the CPU_F register is set.

Additionally, for GPIO Interrupts, the appropriate enable and interrupt-type bits for each I/O pin must be set (see section 6.0, Table 29 on page 31, Table 33 on page 33, and Table 34 on page 34). For Analog Column Interrupts, the interrupt source must be set (see section 10.10 and Table 77 on page 101).

During the servicing of any interrupt, the MSB and LSB of Program Counter and Flag registers (CPU_PC and CPU_F) are stored onto the program stack by an automatic `CALL` instruction (13 cycles) generated during the interrupt acknowledge process. The user firmware may preserve and restore processor state during an interrupt using the `PUSH` and `POP` instructions. The memory oriented CPU architecture requires minimal state saving during interrupts, providing very fast interrupt context switching. The Program Counter and Flag registers (CPU_PC and CPU_F) are restored when the `RETI` instruction is executed. If two or more interrupts are pending at the same time, the higher priority interrupt (lower priority number) will be serviced first.

After a copy of the Flag Register is stored on the stack, the Flag Register is automatically cleared. This disables all interrupts, since the Global IE flag bit is now cleared. Executing a `RETI` instruction restores the Flag register, and re-enables the Global Interrupt bit.

Nested interrupts can be accomplished by re-enabling interrupts inside an interrupt service routine. To do this, set the IE bit in the Flag Register. The user must store sufficient information to maintain machine state if this is done.

Each digital PSoC block has its own unique Interrupt Vector and Interrupt Enable bit. There are also individual interrupt vectors for each of the Analog columns, Supply Voltage Monitor, Sleep Timer and General Purpose I/Os.

8.3 Interrupt Vectors

Table 43: Interrupt Vector Table

Address	Interrupt Priority Number	Description
0x0004	1	Supply Monitor Interrupt Vector
0x0008	2	DBA00 PSoC Block Interrupt Vector
0x000C	3	DBA01 PSoC Block Interrupt Vector
0x0010	4	DBA02 PSoC Block Interrupt Vector
0x0014	5	DBA03 PSoC Block Interrupt Vector
0x0018	6	DCA04 PSoC Block Interrupt Vector
0x001C	7	DCA05 PSoC Block Interrupt Vector
0x0020	8	DCA06 PSoC Block Interrupt Vector
0x0024	9	DCA07 PSoC Block Interrupt Vector
0x0028	10	Acolumn 0 Interrupt Vector
0x002C	11	Acolumn 1 Interrupt Vector
0x0030	12	Acolumn 2 Interrupt Vector
0x0034	13	Acolumn 3 Interrupt Vector
0x0038	14	GPIO Interrupt Vector
0x003C	15	Sleep Timer Interrupt Vector
0x0040		On-Chip Program Memory Starts

The interrupt process vectors the Program Counter to the appropriate address in the Interrupt Vector Table. Typically, these addresses contain `JMP` instructions to the start of the interrupt handling routine for the interrupt.

8.4 Interrupt Masks

Table 44: General Interrupt Mask Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Sleep	GPIO	Acolumn3	Acolumn2	Acolumn1	Acolumn0	Voltage Monitor

Bit 7: **Reserved**

Bit 6: **Sleep Interrupt Enable Bit (see 11.4)**
0 = Disabled
1 = Enabled

Bit 5: **GPIO Interrupt Enable Bit (see 8.6)**
0 = Disabled
1 = Enabled

Bit [4]: **Acolumn 3 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [3]: **Acolumn 2 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [2]: **Acolumn 1 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [1]: **Acolumn 0 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit 0: **Voltage Monitor Interrupt Enable Bit (see 11.5)**
0 = Disabled
1 = Enabled

General Interrupt Mask Register (INT_MSK0, Address = Bank 0, E0h)

9.3.3 Digital Basic Type A/Communications Type A Block xx Control Register 0 When Used as Timer, Counter, CRC, and Deadband

Note that the data in this register, as well as the following three registers, are a mapping of the functions of the variables selected in the associated Digital Basic Type A/ Communications Type A Block xx Control Register 0.

Table 55: Digital Basic Type A/Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	--	--	--	--	--	--	--	0
Read/Write	--	--	--	--	--	--	--	RW
Bit Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Enable

Bit 7: **Reserved**
Bit 6: **Reserved**
Bit 5: **Reserved**
Bit 4: **Reserved**
Bit 3: **Reserved**
Bit 2: **Reserved**
Bit 1: **Reserved**

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Basic Type A Block 00 Control Register 0 (DBA00CR0, Address = Bank 0, 23h)
Digital Basic Type A Block 01 Control Register 0 (DBA01CR0, Address = Bank 0, 27h)
Digital Basic Type A Block 02 Control Register 0 (DBA02CR0, Address = Bank 0, 2Bh)
Digital Basic Type A Block 03 Control Register 0 (DBA03CR0, Address = Bank 0, 2Fh)
Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

9.3.5 Digital Communications Type A Block xx Control Register 0 When Used as UART Receiver

Table 57: Digital Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bit Name	Parity Error	Overrun	Framing Error	RX Active	RX Reg Full	Parity Type	Parity Enable	Enable

Bit 7: **Parity Error**
0 = Indicates no parity error detected in the last byte received
1 = Indicates a parity error detected in the last byte received
Reset when this register is read

Bit 6: **Overrun**
0 = Indicates that no overrun has taken place
1 = Indicates the RX Data register was overwritten with a new byte before the previous one had been read
Reset when this register is read

Bit 5: **Framing Error**
0 = Indicates correct stop bit
1 = Indicates a missing STOP bit
Reset when this register is read

Bit 4: **RX Active**
0 = Indicates no communication currently in progress
1 = Indicates a start bit has been received and a byte is currently being received

Bit 3: **RX Reg Full**
0 = Indicates the RX Data register is empty
1 = Indicates a byte has been loaded into the RX Data register
Interrupt source for RXUART. Reset when the RX Data register is read (Data Register 2)

Bit 2: **Parity Type**
0 = Even
1 = Odd

Bit 1: **Parity Enable**
0 = Parity Disabled
1 = Parity Enabled

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

10.4 Analog Reference Control

The reference generator establishes a set of three internally fixed reference voltages for the whole chip, AGND, RefHi and RefLo. The 8C26xxx is a single supply part, with no negative voltage available or applicable. Analog ground (AGND) is constructed near mid-supply. This ground is routed to all analog blocks and separately buffered within each block. There may be a small offset voltage between buffered analog grounds, as indicated in the AC/DC Characteristics section. RefHi and RefLo signals are generated, buffered and routed to the analog blocks. RefHi is used to set the conversion range (i.e., span) of analog to digital (ADC) and digital to analog (DAC) converters. RefHi and RefLo can be used to set thresholds in comparators.

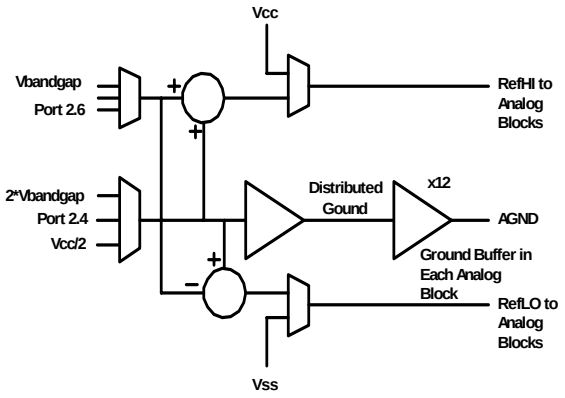

Figure 17: Analog Reference Control Schematic

10.4.1 Bandgap Test

BGT Bandgap Test is used for factory testing of the internal reference voltage testing.

10.4.2 Bias Level

HBE Controls the bias level for all analog functions. It operates with the power setting in each block to set the parameters of that block. Most applications will benefit most from the low bias level. At high bias, the analog block op-amps have faster slew rate but slightly less voltage swing and higher noise.

10.4.3 AGND, RefHI, RefLO

REF Sets Analog Array Reference Control, selecting specific combinations of voltage for analog ground and references. Many of these reference voltages are based on the precision internal reference, a Silicon band gap operating at 1.300 Volts. This reference has good thermal stability and power supply rejection.

Alternatively, the power supply can be scaled to provide analog ground and references; this is particularly useful for signals, which are ratiometric to the power supply voltage.

User supplied external precision references can be connected to Port 2 inputs (available on 28 pin and larger parts). This is useful in setting reference for specific customer applications such as a +/-1.000 V (from AGND) ADC scale. References derived from Port 2 inputs are limited to the same output voltage range as the op-amps in the analog blocks.

divided into distinct bit fields. Some bit fields set the PSoC block's resistor ratios or capacitor values. Others configure switches and multiplexers that form connections between internal block nodes. Additionally, a block may be connected via local interconnection resources to neighboring analog PSoC blocks, reference voltage sources, input multiplexers and output busses. Specific advantages and applications of each type are treated separately below.

10.6.1 Local Interconnect

Analog continuous-time PSoC blocks occupy the top row, (row 0) of the analog array. Designated ACA for analog continuous-time subtype "A," each connects to its neighbors by means of three multiplexers. (Note that unlike the switched capacitor blocks, the continuous time blocks in the current family of parts only have one subtype.) The three are the non-inverting input multiplexer, "PMux," the inverting input multiplexer, "NMux," and the "RBotMux" which controls the node at the bottom of the resistor string. The bit fields, which control these multiplexers, are named PMux, NMux, and RBotMux, respectively. The following diagrams show how each multiplexer connects its ACA block connect to its neighbors. Each arrow points from an input source, either a PSoC block, bus or reference voltage to the block where it is used. Each arrow is labeled with the value to which the bit-field must be set to select that input source.

10.6.1.1 NMux

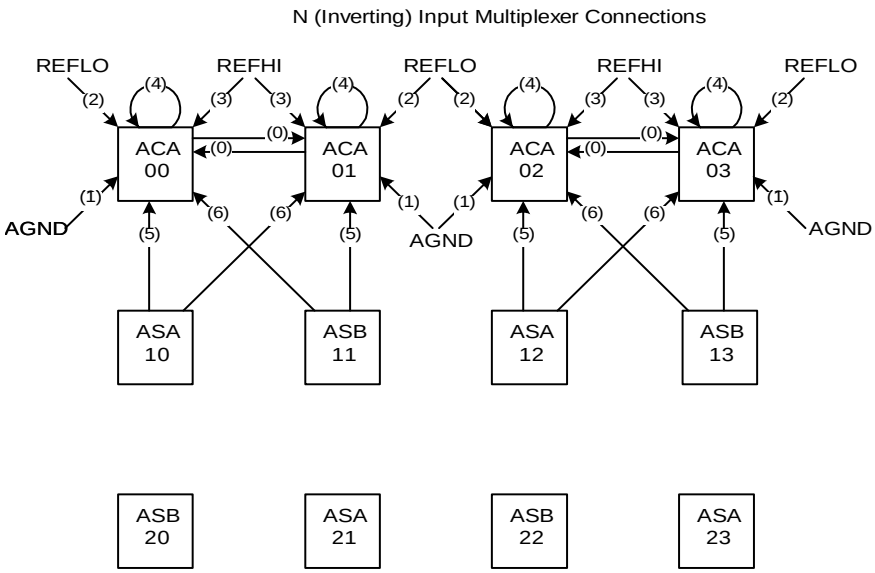

Figure 18: NMux Connections

10.6.1.2 PMux

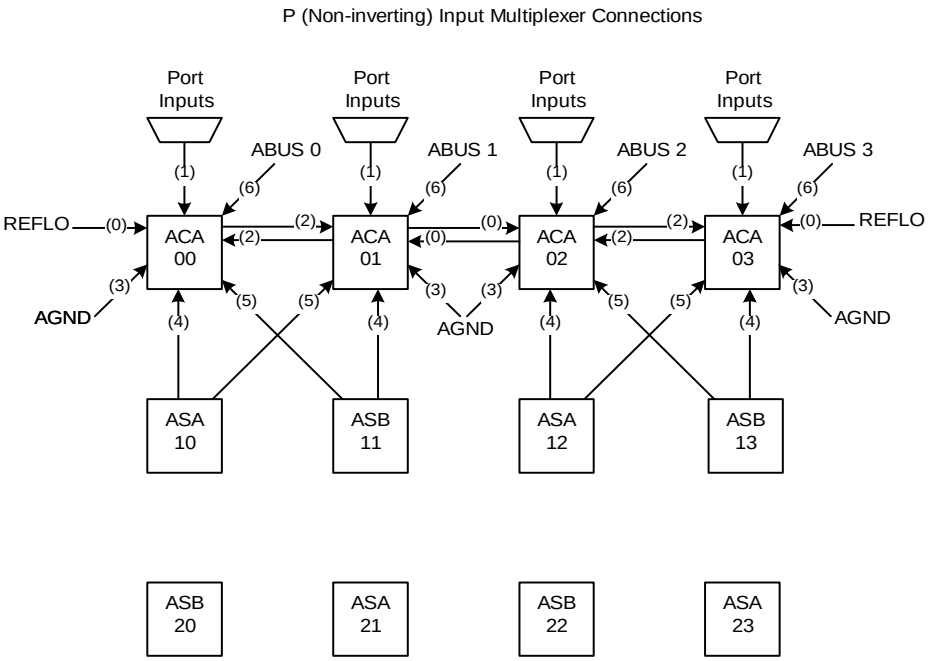

Figure 19: PMux Connections

10.6.1.3 RBotMux

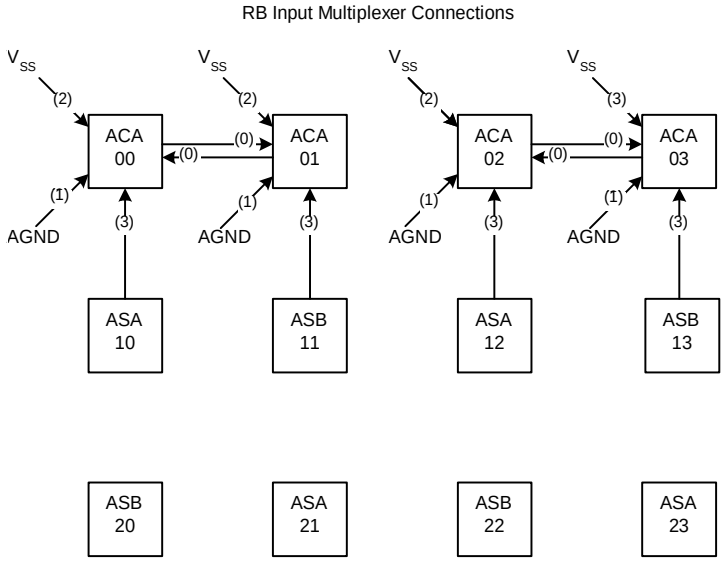

Figure 20: RBotMux Connections

10.7.2.3 Analog Continuous Time Type A Block xx Control 2 Register

CPhase controls which internal clock phase the comparator data is latched on.

CLatch controls whether the latch is active or if it is always transparent.

CompCap controls whether the compensation capacitor is switched in or not in the op-amp. By not switching in the compensation capacitance, a much faster response can be obtained if the amplifier is being used as a comparator.

TestMux – selects block bypass mode for testing and characterization purposes.

Power – encoding for selecting 1 of 4 power levels. The blocks always power up in the off state.

Table 68: Analog Continuous Time Type A Block xx Control 2 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	CPhase	CLatch	CompCap	TestMux[2]	TestMux[1]	TestMux[0]	Power[1]	Power[0]

Bit 7: **CPhase**
0 = Comparator Control latch transparent on PHI1
1 = Comparator Control latch transparent on PHI2

Bit 6: **CLatch**
0 = Comparator Control latch is always transparent
1 = Comparator Control latch is active

Bit 5: **CompCap**
0 = Comparator Mode
1 = Op-amp Mode

Bit [4:2]: **TestMux [2:0]** Select block bypass mode for testing and characterization purposes

	ACA00	ACA01	ACA02	ACA03
1 0 0 = Positive Input to…	ABUS0	ABUS1	ABUS2	ABUS3
1 0 1 = AGND to…	ABUS0	ABUS1	ABUS2	ABUS3
1 1 0 = REFLO to…	ABUS0	ABUS1	ABUS2	ABUS3
1 1 1 = REFHI to…	ABUS0	ABUS1	ABUS2	ABUS3

0 x x = All Paths Off

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = Low (60 µA)
1 0 = Med (150 µA)
1 1 = High (500 µA)

Analog Continuous Time Block 00 Control 2 Register (ACA00CR2, Address = Bank 0/1, 73h)
Analog Continuous Time Block 01 Control 2 Register (ACA01CR2, Address = Bank 0/1, 77h)
Analog Continuous Time Block 02 Control 2 Register (ACA02CR2, Address = Bank 0/1, 7Bh)
Analog Continuous Time Block 03 Control 2 Register (ACA03CR2, Address = Bank 0/1, 7Fh)

10.8.2 Local Interconnect

10.8.2.1 AMux

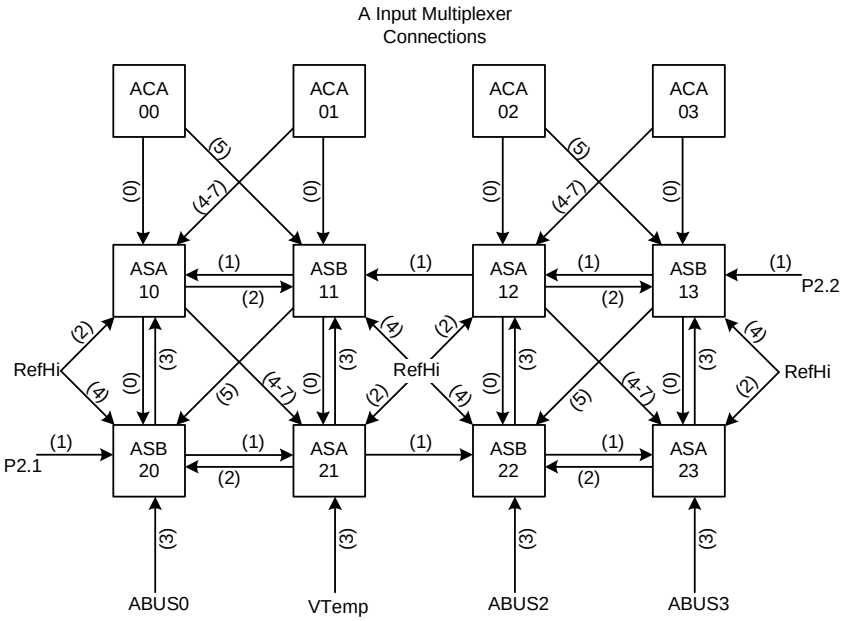

Figure 23: AMux Connections

10.8.2.2 CMux

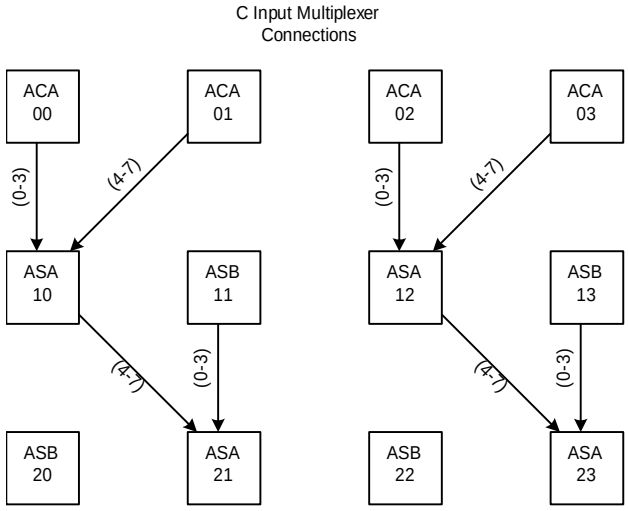

Figure 24: CMux Connections

10.8.3.4 Analog Switch Cap Type A Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASA10CR2, ASA12CR2, ASA21CR2, ASA23CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BMuxSCA controls the muxing to the input of the B capacitor branch.

Power – encoding for selecting 1 of 4 power levels. The block always powers up in the off state.

Table 72: Analog Switch Cap Type A Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BMuxSCA[1]	BMuxSCA[0]	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
1 = If the FSW1 bit is set to 1, the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit [3:2] BMuxSCA [1:0] Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block.)

ASA10	ASA21	ASA12	ASA23
0 0 = ACA00	ASB11	ACA02	ASB13
0 1 = ASB11	ASB20	ASB13	ASB22
1 0 = P2.3	ASB22	ASB11	P2.0
1 1 = ASB20	T_{ref}GND	ASB22	ABUS3

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type A Block 10 Control 3 Register (ASA10CR3, Address = Bank 0/1, 83h)
Analog Switch Cap Type A Block 12 Control 3 Register (ASA12CR3, Address = Bank 0/1, 8Bh)
Analog Switch Cap Type A Block 21 Control 3 Register (ASA21CR3, Address = Bank 0/1, 97h)
Analog Switch Cap Type A Block 23 Control 3 Register (ASA23CR3, Address = Bank 0/1, 9Fh)

10.9 Analog Switch Cap Type B PSoC Blocks

10.9.1 Introduction

The Analog Switch Cap Type B PSoC blocks are built around an operational amplifier. There are several analog muxes that are controlled by register-bit settings in the control registers that determine the signal topology inside the block. There are also four arrays of unit value capacitors that are located in the feedback path for the op-amp, and are switched by two phase clocks, PHI1 and PHI2. These four capacitor arrays are labeled A Cap Array, B Cap Array, C Cap Array, and F Cap Array. There is also an analog comparator connected to the output OUT, which converts analog comparisons into digital signals.

There are three discrete outputs from this block. These outputs are:

1. The analog output bus (ABUS), which is an analog bus resource that is shared by all of the analog blocks in the analog column for that block.

2. The comparator bus (CBUS), which is a digital bus that is a resource that is shared by all of the analog blocks in a column for that block.

3. The output bus (OUT), which is an analog bus resource that is shared by all of the analog blocks in a column and connects to one of the analog output buffers, to send a signal externally to the device.

The SCB block also supports Delta-Sigma, Successive Approximation and Incremental A/D Conversion, Capacitor DACs, and SC filters. It has two input arrays of switched capacitors, and a Non-Switched capacitor feedback array from the output. When preceded by an SC Block A Integrator, the combination can be used to provide a full Switched Capacitor Biquad.

10.9.2.2 Analog Switch Cap Type B Block xx Control 1 Register

AMux controls the input muxing for the A capacitor branch.

The BCap bits set the value of the capacitor in the B path.

Table 74: Analog Switch Cap Type B Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AMux[2]	AMux[1]	AMux[0]	BCap[4]	BCap[3]	BCap[2]	BCap[1]	BCap[0]

Bit [7:5]: **AMux [2:0]** Input muxing select for A capacitor branch. (Note that available mux inputs vary by individual PSoC block.)

ASB11	ASB13	ASB20	ASB22
0 0 0 = ACA01	ACA03	ASA10	ASA12
0 0 1 = ASA12	P2.2	P2.1	ASA21
0 1 0 = ASA10	ASA12	ASA21	ASA23
0 1 1 = ASA21	ASA23	ABUS0	ABUS2
1 0 0 = REFHI	REFHI	REFHI	REFHI
1 0 1 = ACA00	ACA02	ASB11	ASB13
1 1 0 = Reserved	Reserved	Reserved	Reserved
1 1 1 = Reserved	Reserved	Reserved	Reserved

Bit [4:0]: BCap [4:0] Binary encoding for 32 possible capacitor sizes for B Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 1 Register (ASB11CR1, Address = Bank 0/1, 85h)
Analog Switch Cap Type B Block 13 Control 1 Register (ASB13CR1, Address = Bank 0/1, 8Dh)
Analog Switch Cap Type B Block 20 Control 1 Register (ASB20CR1, Address = Bank 0/1, 91h)
Analog Switch Cap Type B Block 22 Control 1 Register (ASB22CR1, Address = Bank 0/1, 99h)

10.12.3 Analog Output Buffers

The user has the option to output up to four analog signals on the pins of the device. This is done by enabling the analog output buffers associated with each Analog Column. The enable bits for the analog output buffers are contained in the Analog Output Buffer Control Register (ABF_CR).

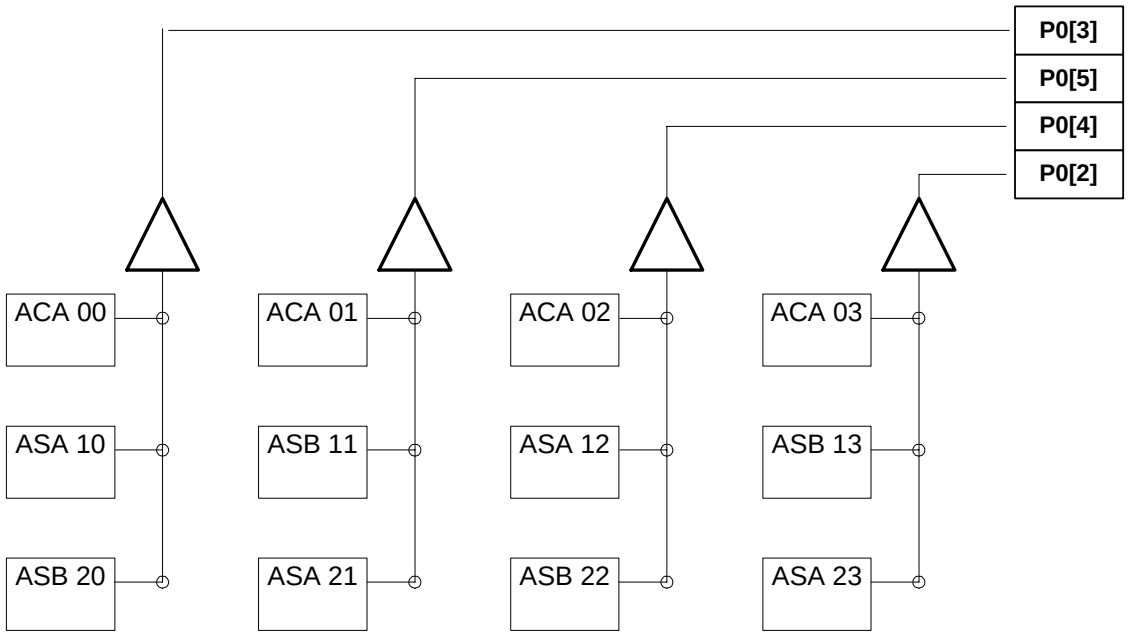

Figure 28: Analog Output Buffers

11.3 Reset

11.3.1 Overview

The microcontroller supports two types of resets. When reset is initiated, all registers are restored to their default states and all interrupts are disabled.

Reset Types: Power On Reset (POR), External Reset (X_{res}), and Watchdog Reset (WDR).

The occurrence of a reset is recorded in the Status and Control Register (CPU_SCR). Bits within this register record the occurrence of POR and WDR Reset respectively. The firmware can interrogate these bits to determine the cause of a reset.

The microcontroller resumes execution from ROM address 0x0000 after a reset. The internal clocking mode is active after a reset, until changed by user firmware. In addition, the Sleep / Watchdog Timer is reset to its minimum interval count.

Important: The CPU clock defaults to divide by 8 mode at POR to guarantee operation at the low Vcc that might be present during the supply ramp.

Table 94: Processor Status and Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	1	0	0	0	0
Read/ Write	R	--	R/C[1]	R/C[1]	RW	--	--	RW
Bit Name	IES	Reserved	WDRS	PORS	Sleep	Reserved	Reserved	Stop

Bit 7: **IES** Global interrupt enable status from CPU Flag register
0 = Global interrupts disabled
1 = Global interrupts enabled

Bit 6: **Reserved**

Bit 5: **WDRS**
WDRS is set by the CPU to indicate that a Watchdog Reset event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit
0 = No WDR
1 = A WDR event has occurred

Bit 4: **PORS**
PORS is set by the CPU to indicate that a Power On Reset event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit
0 = No POR
1 = A POR event has occurred. (Note that WDR events will not occur until this bit is cleared)

Bit 3: **Sleep** Set by the user to enable CPU sleep state. CPU will remain in sleep mode until any interrupt is pending
0 = Normal operation
1 = Sleep

Bit 2: **Reserved**
Bit 1: **Reserved**

Bit 0: **Stop** Set by the user to halt the CPU. The CPU will remain halted until a reset (WDR or POR) has taken place
0 = Normal CPU operation
1 = CPU is halted (not recommended)

1. C = Clear

Status and Control Register (CPU_SCR, Address = Bank 0/1, FFh)

13.2 DC Characteristics

Table 104: DC Operating Specifications

Symbol	DC Operating Specifications	Minimum	Typical	Maximum	Unit
V_{cc}	Supply Voltage	3.00	-	5.25	V
I_{cc}	Supply Current	-	5	8[1]	mA
I_{sb}	Sleep (Mode) Current	-	-	5[2]	µA
I_{sbxtl}	Sleep (Mode) Current with Crystal Oscillator	-	3	5[3]	µA
V_{ref}	Reference Voltage (Bandgap)	1.275	1.3	1.325[4]	V
V_{il}	Input Low Voltage	-	-	0.8	V
V_{ih}	Input High Voltage	2.2	-	-	V
V_h	Hysterisis Voltage	-	60	-	mV
V_{ol}	Output Low Voltage	-	-	Vss+0.75[5]	V
V_{oh}	Output High Voltage	V_{cc}-1.0[6]	-	-	V
R_{pu}	Pull Up Resistor Value	4000	5600	8000	Ω
R_{pd}	Pull Down Resistor Value	4000	5600	8000	Ω
I_{il}	Input Leakage (Absolute Value)	-	0.1	5	µA
C_{in}	Capacitive Load on Pins as Input	0.5	1.7	10[7]	pF
C_{out}	Capacitive Load on Pins as Output	0.5	1.7	10[7]	pF
V_{LVD}	LVD and SMP Tolerance[8]	0.95 x Ideal[8]	Ideal	1.05 x Ideal[8]	V

1. Conditions are 5.0V, 25 ^{o}C, 3 MHz.
2. Without Crystal Oscillator, V_{cc} = 3.3 V, TA <= 85 ^{o}C.
3. Conditions are 3.0V <= V_{cc} <= 3.6V, -40 ^{o}C <= TA <= 85 ^{o}C. Correct operation assumes a properly loaded, 1 uW maximum drive level, 32.768 kHz crystal.
4. Trimmed for appropriate V_{cc}.
5. Isink = 25 mA, V_{cc} = 4.5 V (maximum of 8 IO sinking, 4 on each side of the IC).
6. Isource =10 mA, V_{cc} = 4.5 V (maximum of 8 IO sourcing, 4 on each side of the IC).
7. Package dependent.
8. Ideal values are +/- 5% absolute tolerance and +/- 1% tolerance relative to each other (for adjacent levels).

15.0 Ordering Guide

Table 123: Ordering Guide (Leaded)[1]

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVI	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVI	16	256	Yes	Ind. -40C to +85C
48 Pin (600 Mil) Molded DIP	CY8C26643-24PI[2]	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AI	16	256	Yes	Ind. -40C to +85C

1. Orders for leaded devices will not be accepted after July 2005.
2. 48-PDIP package not offered Pb-Free.

Table 124: Ordering Guide (Pb-Free Denoted with an “X” in Ordering Code)

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PXI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26233-24SXIT	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVXI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP Tape and Reel	CY8C26233-24PVXIT	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26443-24SXIT	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVXI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP Tape and Reel	CY8C26443-24PVXIT	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVXI	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP Tape and Reel	CY8C26643-24PVXIT	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AXI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack Tape and Reel	CY8C26643-24AXIT	16	256	Yes	Ind. -40C to +85C