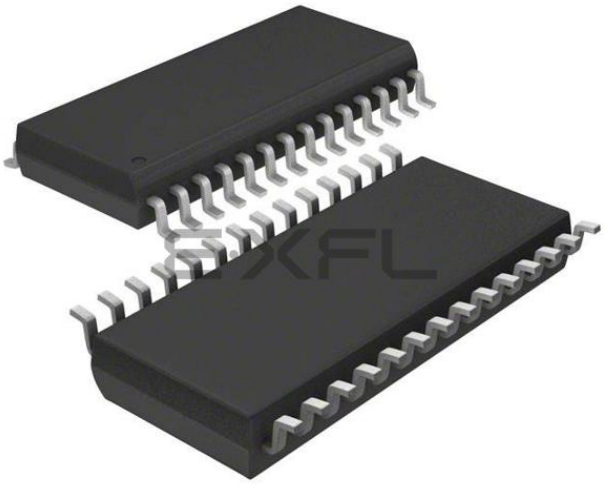

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26443-24pvi

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3.0 Memory Organization

3.1 Flash Program Memory Organization

Table 24: Flash Program Memory Map

Address	Description
0x0000	Reset Vector
0x0004	Supply Monitor Interrupt Vector
0x0008	DBA 00 PSoC Block Interrupt Vector
0x000C	DBA 01 PSoC Block Interrupt Vector
0x0010	DBA 02 PSoC Block Interrupt Vector
0x0014	DBA 03 PSoC Block Interrupt Vector
0x0018	DCA 04 PSoC Block Interrupt Vector
0x001C	DCA 05 PSoC Block Interrupt Vector
0x0020	DCA 06 PSoC Block Interrupt Vector
0x0024	DCA 07 PSoC Block Interrupt Vector
0x0028	Analog Column 0 Interrupt Vector
0x002C	Analog Column 1 Interrupt Vector
0x0030	Analog Column 2 Interrupt Vector
0x0034	Analog Column 3 Interrupt Vector
0x0038	GPIO Interrupt Vector
0x003C	Sleep Timer Interrupt Vector
0x0040	On-Chip User Program Memory Starts Here
	***
	***
	***
0x3FFF	16K Flash Maximum Depending on Version

3.2 RAM Data Memory Organization

The stack on this device grows from low addresses to high addresses. The Linker function within PSoC Designer locates the bottom of the stack after the end of Global Variables. This allows the stack to grow from just after the Global Variables until 0xFF. The stack will wrap back to 0x00 on an overflow condition.

Table 25: RAM Data Memory Map

Address	Description
0x00	First General Purpose RAM Location
0xXX	General Purpose RAM
0xXY	General Purpose RAM
0xXZ	Last General Purpose RAM Location
0xYX	Bottom of Hardware Stack
0xYY	⇓ Stack Grows This Way ⇓
0xFF	Top of Hardware Stack

4.0 Register Organization

4.1 Introduction

There are two register banks implemented on these devices. Each bank contains 256 addresses. The purpose of these register banks is to personalize and parameterize the on-chip resources as well as read and write data values.

The user selects between the two banks by setting the XIO bit in the CPU_F Flag Register.

In some cases, the same register is available on either bank, for convenience. These registers (71h to 9fh) can be accessed from either bank.

Note: All register addresses not shown are reserved and should never be written. In addition, unused or reserved bits in any register should always be written to 0.

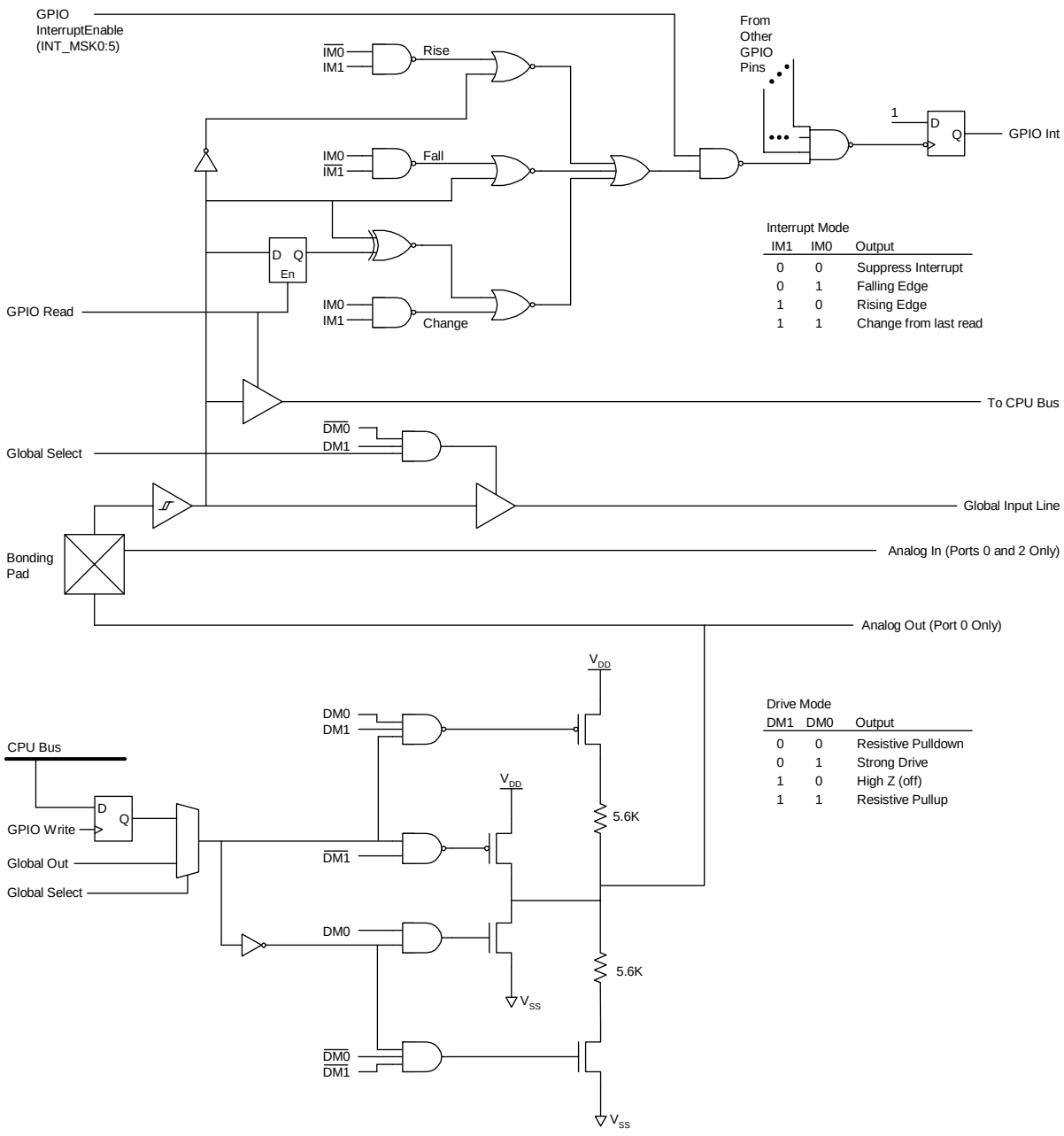

Figure 7: General Purpose I/O Pins

6.3 Port Global Select Registers

Table 30: Port Global Select Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	GlobSel [7]	GlobSel [6]	GlobSel [5]	GlobSel [4]	GlobSel [3]	GlobSel [2]	GlobSel [1]	GlobSel [0]

Bit [7:0]: **Global Select [7:0]** When written determines whether a pin is connected to the Global Input Bus and Global Output Bus
0 = Not Connected
1 = Connected

Drive Mode xx = Global Select Register 0 = Standard CPU controlled port (Default)
Drive Mode 1 0 (High Z) = Global Select Register 1 = Direct Drive of associated Global Input line
Drive Mode 0 0, 0 1, 1 1 = Global Select Register 1 = Direct Receive from associated Global Output line

Port 0 Global Select Register (PRT0GS, Address = Bank 0, 02h)
Port 1 Global Select Register (PRT1GS, Address = Bank 0, 06h)
Port 2 Global Select Register (PRT2GS, Address = Bank 0, 0Ah)
Port 3 Global Select Register (PRT3GS, Address = Bank 0, 0Eh)
Port 4 Global Select Register (PRT4GS, Address = Bank 0, 12h)
Port 5 Global Select Register (PRT5GS, Address = Bank 0, 16h) Note: If implemented, Port 5 is 4-bits wide

6.3.1 Port Drive Mode 0 Registers

Table 31: Port Drive Mode 0 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	DM0 [7]	DM0 [6]	DM0 [5]	DM0 [4]	DM0 [3]	DM0 [2]	DM0 [1]	DM0 [0]

Bit [7:0]: **DM0 [7:0]** The two Drive Mode bits that control a particular port pin are treated as a pair and are decoded as follows:

Port Data Register Bit 0 = Drive Mode 0 0 = 0 Resistive (Default)
Port Data Register Bit 0 = Drive Mode 0 1 = 0 Strong
Port Data Register Bit 0 = Drive Mode 1 0 = High Z
Port Data Register Bit 0 = Drive Mode 1 1 = 0 Strong
Port Data Register Bit 1 = Drive Mode 0 0 = 1 Strong
Port Data Register Bit 1 = Drive Mode 0 1 = 1 Strong
Port Data Register Bit 1 = Drive Mode 1 0 = High Z
Port Data Register Bit 1 = Drive Mode 1 1 = 1 Resistive

Port 0 Drive Mode 0 Register (PRT0DM0, Address = Bank 1, 00h)
Port 1 Drive Mode 0 Register (PRT1DM0, Address = Bank 1, 04h)
Port 2 Drive Mode 0 Register (PRT2DM0, Address = Bank 1, 08h)
Port 3 Drive Mode 0 Register (PRT3DM0, Address = Bank 1, 0Ch)
Port 4 Drive Mode 0 Register (PRT4DM0, Address = Bank 1, 10h)
Port 5 Drive Mode 0 Register (PRT5DM0, Address = Bank 1, 14h) **Note**: Port 5 is 4-bits wide

6.3.2 Port Drive Mode 1 Registers

Table 32: Port Drive Mode 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	DM1 [7]	DM1 [6]	DM1 [5]	DM1 [4]	DM1 [3]	DM1 [2]	DM1 [1]	DM1 [0]
Bit [7:0]: **DM1 [7:0]** See truth table for Port Drive Mode 0 Registers, above								

Port 0 Drive Mode 1 Register (PRT0DM1, Address = Bank 1, 01h)
Port 1 Drive Mode 1 Register (PRT1DM1, Address = Bank 1, 05h)
Port 2 Drive Mode 1 Register (PRT2DM1, Address = Bank 1, 09h)
Port 3 Drive Mode 1 Register (PRT3DM1, Address = Bank 1, 0Dh)
Port 4 Drive Mode 1 Register (PRT4DM1, Address = Bank 1, 11h)
Port 5 Drive Mode 1 Register (PRT5DM1, Address = Bank 1, 15h) **Note**: Port 5 is 4-bits wide

6.3.3 Port Interrupt Control 0 Registers

Table 33: Port Interrupt Control 0 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	IC0 [7]	IC0 [6]	IC0 [5]	IC0 [4]	IC0 [3]	IC0 [2]	IC0 [1]	IC0 [0]
Bit [7:0]: **IC0 [7:0]** The two Interrupt Control bits that control a particular port pin are treated as a pair and are decoded as follows: IC1 [x], IC0 [x] = 0 0 = Disabled (Default) IC1 [x], IC0 [x] = 0 1 = Falling Edge (-) IC1 [x], IC0 [x] = 1 0 = Rising Edge (+) IC1 [x], IC0 [x] = 1 1 = Change from Last Direct Read								

Port 0 Interrupt Control 0 Register (PRT0IC0, Address = Bank 1, 02h)
Port 1 Interrupt Control 0 Register (PRT1IC0, Address = Bank 1, 06h)
Port 2 Interrupt Control 0 Register (PRT2IC0, Address = Bank 1, 0Ah)
Port 3 Interrupt Control 0 Register (PRT3IC0, Address = Bank 1, 0Eh)
Port 4 Interrupt Control 0 Register (PRT4IC0, Address = Bank 1, 12h)
Port 5 Interrupt Control 0 Register (PRT5IC0, Address = Bank 1, 16h) **Note**: Port 5 is 4-bits wide

9.0 Digital PSoC Blocks

9.1 Introduction

PSoC blocks are user configurable system resources. On-chip digital PSoC blocks reduce the need for many MCU part types and external peripheral components. Digital PSoC blocks can be configured to provide a wide variety of peripheral functions. PSoC Designer Software Integrated Development Environment provides automated configuration of PSoC blocks by simply selecting the desired functions. PSoC Designer then generates the proper configuration information and can print a device data sheet unique to that configuration.

Digital PSoC blocks provide up to eight, 8-bit multipurpose timers/counters supporting multiple event timers, real-time clocks, Pulse Width Modulators (PWM), and CRCs. In addition to all PSoC block functions, communication PSoC blocks support full-duplex UARTs and SPI master or slave functions.

As shown in Figure 12:, there are a total of eight 8-bit digital PSoC blocks in this device family configured as a linear array. Four of these are the Digital Basic Type A blocks and four are the Digital Communications Type A blocks. Each of these digital PSoC blocks can be configured independently, or used in combination.

Each digital PSoC block has a unique Interrupt Vector and Interrupt Enable bit. Functions can be stopped or started with a user-accessible Enable bit.

The Timer/Counter/CRC/PRS/Deadband functions are available on the Digital Basic Type A blocks and also the Digital Communications Type A blocks. The UART and SPI communications functions are only available on the Digital Communications Type A blocks.

There are three configuration registers: the Function Register (DBA00FN-DCA07FN) to select the block function and mode, the Input Register (DBA00IN-DCA07IN) to select data input and clock selection, and the Output Register (DBA00OU-DCA07OU) to select and enable function outputs.

The three data registers are designated Data 0 (DBA00DR0-DCA07DR0), Data 1 (DBA00DR1-DCA07DR1), and Data 2 (DBA00DR2-DCA07DR2). The function of these registers and their bit mapping is dependent on the overall block function selected by the user.

The one Control Register (DBA00CR0-DCA07CR0) is designated Control 0. The function of this register and its bit mapping is dependent on the overall block function selected by the user.

If the CPU frequency is 24 MHz and a PSoC timer/counter of 24-bits or longer is operating at 48 MHz, a write to the block Control Register to enable it (for example, a call to Timer_1_Start) may not start the block properly. In the failure case, the first count will typically be indeterminate as the upper bytes fail to make the first count correctly. However, on the first terminal count, the correct period will be loaded and counted thereafter.

Digital Communications Type A Block 05 Function Register (DCA05FN, Address = Bank 1, 34h)
Digital Communications Type A Block 06 Function Register (DCA06FN, Address = Bank 1, 38h)
Digital Communications Type A Block 07 Function Register (DCA07FN, Address = Bank 1, 3Ch)

9.2.2 Digital Basic Type A / Communications Type A Block xx Input Register

The Digital Basic Type A / Communications Type A Block xx Input Register (DBA00IN-DCA07IN) consists of 4 bits [3:0] to select the block input clock and 4 bits [7:4] to select the primary data/enable input. The actual usage of the input data/enable is function dependent.

Table 48: Digital Basic Type A / Communications Type A Block xx Input Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [3]	Data [2]	Data [1]	Data [0]	Clock [3]	Clock [2]	Clock [1]	Clock [0]

Bit [7:4]: **Data [3:0] Data Enable Source Select**
0 0 0 0 = Data = 0
0 0 0 1 = Data = 1
0 0 1 0 = Digital Block 03
0 0 1 1 = Chain Function to Previous Block
0 1 0 0 = Analog Column Comparator 0
0 1 0 1 = Analog Column Comparator 1
0 1 1 0 = Analog Column Comparator 2
0 1 1 1 = Analog Column Comparator 3
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Bit [3:0]: **Clock [3:0] Clock Source Select**
0 0 0 0 = Clock Disabled
0 0 0 1 = Global Output[4] (for Digital Blocks 00 to 03) **or** Global Output[0] (for Digital Blocks 04 to 07)
0 0 1 0 = Digital Block 03 (Primary Output)
0 0 1 1 = Previous Digital PSoC block (Primary Output)
0 1 0 0 = 48M
0 1 0 1 = 24V1
0 1 1 0 = 24V2
0 1 1 1 = 32k
1 0 0 0 = Global Output[0] (for Digital Blocks 00 to 03) **or** Global Output[4] (for Digital Blocks 04 to 07)
1 0 0 1 = Global Output[1] (for Digital Blocks 00 to 03) **or** Global Output[5] (for Digital Blocks 04 to 07)
1 0 1 0 = Global Output[2] (for Digital Blocks 00 to 03) **or** Global Output[6] (for Digital Blocks 04 to 07)
1 0 1 1 = Global Output[3] (for Digital Blocks 00 to 03) **or** Global Output[7] (for Digital Blocks 04 to 07)
1 1 0 0 = Global Input[0] (for Digital Blocks 00 to 03) **or** Global Input[4] (for Digital Blocks 04 to 07)
1 1 0 1 = Global Input[1] (for Digital Blocks 00 to 03) **or** Global Input[5] (for Digital Blocks 04 to 07)
1 1 1 0 = Global Input[2] (for Digital Blocks 00 to 03) **or** Global Input[6] (for Digital Blocks 04 to 07)
1 1 1 1 = Global Input[3] (for Digital Blocks 00 to 03) **or** Global Input[7] (for Digital Blocks 04 to 07)

Digital Basic Type A Block 00 Input Register (DBA00IN, Address = Bank 1, 21h)
Digital Basic Type A Block 01 Input Register (DBA01IN, Address = Bank 1, 25h)
Digital Basic Type A Block 02 Input Register (DBA02IN, Address = Bank 1, 29h)
Digital Basic Type A Block 03 Input Register (DBA03IN, Address = Bank 1, 2Dh)
Digital Communications Type A Block 04 Input Register (DCA04IN, Address = Bank 1, 31h)
Digital Communications Type A Block 05 Input Register (DCA05IN, Address = Bank 1, 35h)

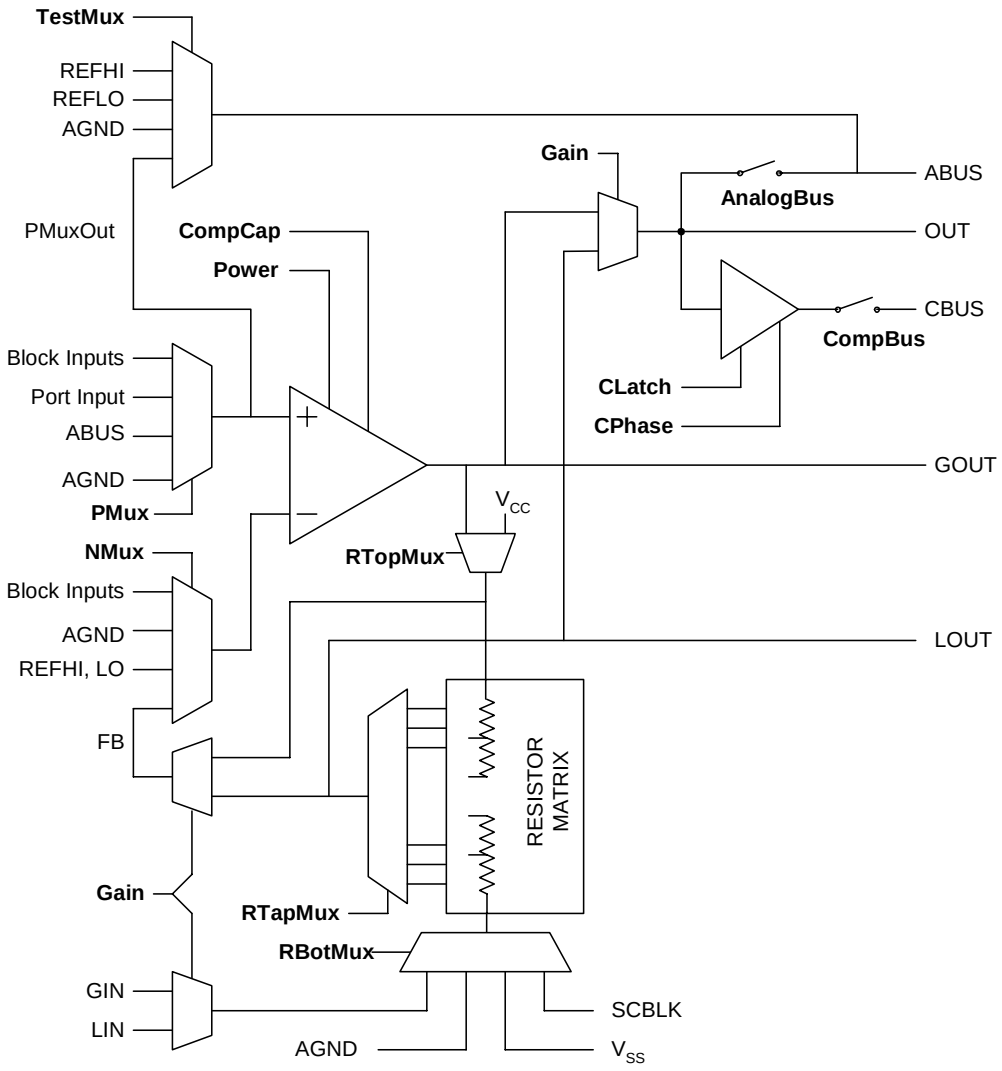

Figure 21: Analog Continuous Time PSoC Blocks

10.7.2 Registers

10.7.2.1 Analog Continuous Time Block xx Control 0 Register

The RTopMux and RBotMux bits control the connection of the two ends of the resistor string. The RTopMux bit controls the top end of the resistor string, which can either be connected to Vcc or to the op-amp output. The RBotMux bits control the connection of the bottom end of the resistor string.

The RTapMux bits control the center tap of the resistor string. Note that only relative weighting of units is given in the table.

The Gain and Loss columns correspond to the gain or loss obtained if the RTopMux and Gain bits are set so that the overall amplifier provides gain or loss.

The Gain bit controls whether the resistor string is connected around the op-amp as for gain (center tap to

10.7.2.2 Analog Continuous Time Block xx Control 1 Register

The PMux bits control the multiplexing of inputs to the non-inverting input of the op-amp. There are physically only 7 inputs.

The 8th code (111) will leave the input floating. This is not desirable, and should be avoided.

The NMux bits control the multiplexing of inputs to the inverting input of the op-amp. There are physically only 7 inputs.

CompBus controls a tri-state buffer that drives the comparator logic. If no PSoC block in the analog column is driving the comparator bus, it will be driven low externally to the blocks.

AnalogBus controls the analog output bus. A CMOS switch connects the op-amp output to the analog bus.

Table 67: Analog Continuous Time Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	NMux2	NMux1	NMux0	PMux2	PMux1	PMux0

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable analog bus driven by this block
1 = Enable analog bus driven by this block
Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable comparator bus driven by this block
1 = Enable comparator bus driven by this block

Bit [5:3]: **NMux [2:0]** Encoding for negative input select

	ACA00	ACA01	ACA02	ACA03
0 0 0 =	ACA01	ACA00	ACA03	ACA02
0 0 1 =	AGND	AGND	AGND	AGND
0 1 0 =	REFLO	REFLO	REFLO	REFLO
0 1 1 =	REFHI	REFHI	REFHI	REFHI
1 0 0[1] =	ACA00	ACA01	ACA02	ACA03
1 0 1 =	ASA10	ASB11	ASA12	ASB13
1 1 0 =	ASB11	ASA10	ASB13	ASA12
1 1 1 =	Reserved	Reserved	Reserved	Reserved

Bit [2:0]: **PMux [2:0]** Encoding for positive input select

	ACA00	ACA01	*ACA02*	ACA03
0 0 0 =	REFLO	ACA02	ACA01	REFLO
0 0 1 =	Port Inputs	Port Inputs	Port Inputs	Port Inputs
0 1 0 =	ACA01	ACA00	ACA03	ACA02
0 1 1 =	AGND	AGND	AGND	AGND
1 0 0 =	ASA10	ASB11	ASA12	ASB13
1 0 1 =	ASB11	ASA10	ASB13	ASA12
1 1 0 =	ABUS0	ABUS1	ABUS2	ABUS3
1 1 1 =	Reserved	Reserved	Reserved	Reserved

1. This in fact is the feedback input of the MUX.

Analog Continuous Time Block 00 Control 1 Register (ACA00CR1, Address = Bank 0/1, 72h)
Analog Continuous Time Block 01 Control 1 Register (ACA01CR1, Address = Bank 0/1, 76h)
Analog Continuous Time Block 02 Control 1 Register (ACA02CR1, Address = Bank 0/1, 7Ah)
Analog Continuous Time Block 03 Control 1 Register (ACA03CR1, Address = Bank 0/1, 7Eh)

10.8.2 Local Interconnect

10.8.2.1 AMux

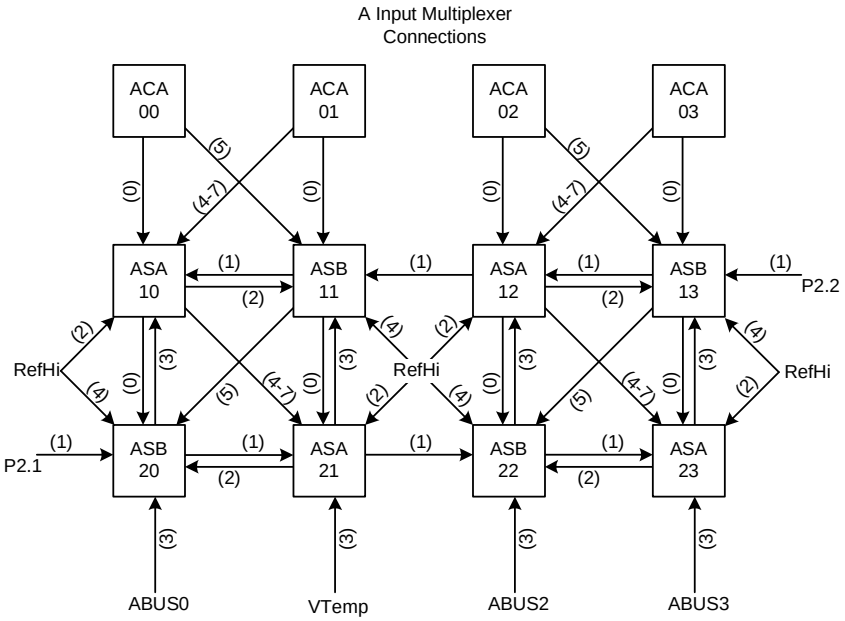

Figure 23: AMux Connections

10.8.2.2 CMux

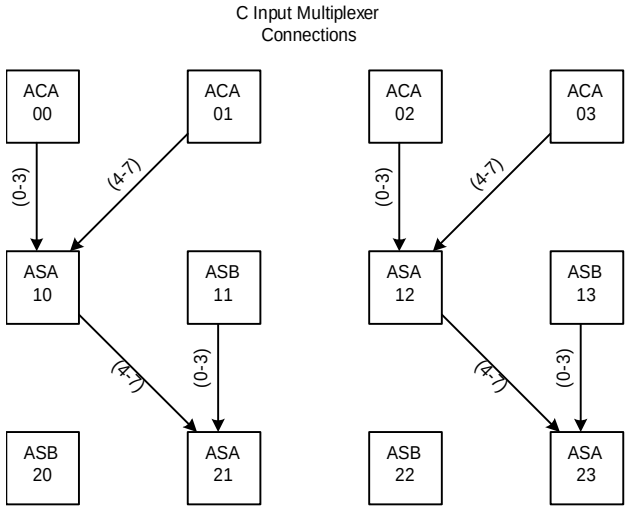

Figure 24: CMux Connections

Table 71: Analog Switch Cap Type A Block xx Control 2 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	AutoZero	CCap[4]	CCap[3]	CCap[2]	CCap[1]	CCap[0]

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable output to analog column bus
1 = Enable output to analog column bus
(The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASA10CR0, ASA12CR0, ASA21CR0, ASA23CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the signal that is output to the analog column bus is selected by the ClockPhase bit. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus.)

Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable output to comparator bus
1 = Enable output to comparator bus

Bit 5: **AutoZero** Bit for controlling gated switches
0 = Shorting switch is not active. Input cap branches shorted to op-amp input
1 = Shorting switch is enabled during internal PHI1. Input cap branches shorted to analog ground during internal PHI1 and to op-amp input during internal PHI2.

Bit [4:0]: **CCap [4:0]** Binary encoding for 32 possible capacitor sizes for C Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type A Block 10 Control 2 Register (ASA10CR2, Address = Bank 0/1, 82h)
Analog Switch Cap Type A Block 12 Control 2 Register (ASA12CR2, Address = Bank 0/1, 8Ah)
Analog Switch Cap Type A Block 21 Control 2 Register (ASA21CR2, Address = Bank 0/1, 96h)
Analog Switch Cap Type A Block 23 Control 2 Register (ASA23CR2, Address = Bank 0/1, 9Eh)

10.12.3 Analog Output Buffers

The user has the option to output up to four analog signals on the pins of the device. This is done by enabling the analog output buffers associated with each Analog Column. The enable bits for the analog output buffers are contained in the Analog Output Buffer Control Register (ABF_CR).

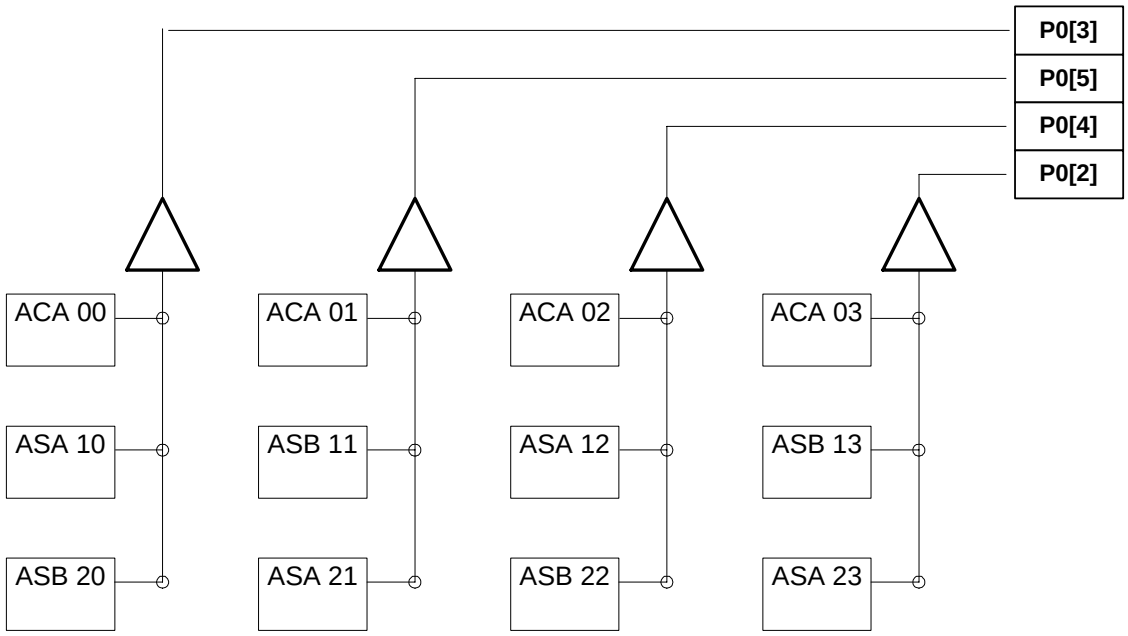

Figure 28: Analog Output Buffers

11.3 Reset

11.3.1 Overview

The microcontroller supports two types of resets. When reset is initiated, all registers are restored to their default states and all interrupts are disabled.

Reset Types: Power On Reset (POR), External Reset (X_{res}), and Watchdog Reset (WDR).

The occurrence of a reset is recorded in the Status and Control Register (CPU_SCR). Bits within this register record the occurrence of POR and WDR Reset respectively. The firmware can interrogate these bits to determine the cause of a reset.

The microcontroller resumes execution from ROM address 0x0000 after a reset. The internal clocking mode is active after a reset, until changed by user firmware. In addition, the Sleep / Watchdog Timer is reset to its minimum interval count.

Important: The CPU clock defaults to divide by 8 mode at POR to guarantee operation at the low Vcc that might be present during the supply ramp.

Table 94: Processor Status and Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	1	0	0	0	0
Read/ Write	R	--	R/C[1]	R/C[1]	RW	--	--	RW
Bit Name	IES	Reserved	WDRS	PORS	Sleep	Reserved	Reserved	Stop

Bit 7: **IES** Global interrupt enable status from CPU Flag register
0 = Global interrupts disabled
1 = Global interrupts enabled

Bit 6: **Reserved**

Bit 5: **WDRS**
WDRS is set by the CPU to indicate that a Watchdog Reset event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit
0 = No WDR
1 = A WDR event has occurred

Bit 4: **PORS**
PORS is set by the CPU to indicate that a Power On Reset event has occurred. The user can read this bit to determine the type of reset that has occurred. The user can clear but not set this bit
0 = No POR
1 = A POR event has occurred. (Note that WDR events will not occur until this bit is cleared)

Bit 3: **Sleep** Set by the user to enable CPU sleep state. CPU will remain in sleep mode until any interrupt is pending
0 = Normal operation
1 = Sleep

Bit 2: **Reserved**
Bit 1: **Reserved**

Bit 0: **Stop** Set by the user to halt the CPU. The CPU will remain halted until a reset (WDR or POR) has taken place
0 = Normal CPU operation
1 = CPU is halted (not recommended)

1. C = Clear

Status and Control Register (CPU_SCR, Address = Bank 0/1, FFh)

11.5 Supply Voltage Monitor

The Supply Voltage Monitor detector generates an interrupt whenever Vcc drops below a pre-programmed value. There are eight voltage trip points that are selectable by setting the VM [2:0] bit in the Voltage Monitor Control Register (VLT_CR). These bits also select the Switch Mode Pump trip points. The Supply Voltage Monitor will remain active when the device enters sleep mode.

Table 96: Voltage Monitor Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	--	--	--	--	W	W	W
Bit Name	SMP	Reserved	Reserved	Reserved	Reserved	VM [2]	VM [1]	VM [0]

Bit 7: **SMP** Disables SMP function
0 = Switch Mode Pump enabled, default
1 = Switch Mode Pump disabled

Bit 6: **Reserved**
Bit 5: **Reserved**
Bit 4: **Reserved**
Bit 3: **Reserved**

Bit [2:0]: **VM [2:0]**

Low Voltage Detection	Switch Mode Pump
0 0 0 = 2.95 Trip Voltage[1]	0 0 0 = 3.17 Trip Voltage
0 0 1 = 3.02 Trip Voltage	0 0 1 = 3.25 Trip Voltage
0 1 0 = 3.17 Trip Voltage	0 1 0 = 3.42 Trip Voltage
0 1 1 = 3.71 Trip Voltage	0 1 1 = 3.94 Trip Voltage
1 0 0 = 4.00 Trip Voltage	1 0 0 = 4.19 Trip Voltage
1 0 1 = 4.48 Trip Voltage	1 0 1 = 4.64 Trip Voltage
1 1 0 = 4.56 Trip Voltage	1 1 0 = 4.82 Trip Voltage
1 1 1 = 4.64 Trip Voltage	1 1 1 = 5.00 Trip Voltage

1. Voltages are ideal typical values. Tolerances are in Table 104 on page 129.

Voltage Monitor Control Register (VLT_CR, Address = Bank 1, E3h)

Table 98: CY8C25122, CY8C26233, CY8C26443, CY8C26643 (256 Bytes of SRAM)

Operation	Function	Accumulator	Input SRAM Data								Output SRAM Data							
			F8h	F9h	FAh	FBh	FCh	FDh	FEh	FFh	F8h	F9h	FAh	FBh	FCh	FDh	FEh	FFh
Reset[1]	Calibrates then sets PC and SP values to 0	00	NA	NA	NA	NA	NA	NA	NA	NA	*	*	*	*	*	*	*	*
Read Block	Move block of 64 bytes of FLASH data into SRAM	01	3Ah	SP +3	Blk ID	Pointer	NA	0	0	0	0	0	*	*	*	*	*	*
Write Block[2]	Program block of FLASH with data from SRAM	02	3Ah	SP +3	Blk ID	Pointer	Clock	0	0	0	0	0	*	*	*	*	*	*
Erase Block	Erase block of FLASH	03	3Ah	SP +3	Blk ID	NA	Clock	0	0	0	0	0	*	*	*	*	*	*
Protect Block[3]	Set memory protection bits[4]	04	3Ah	SP +3	NA	NA	Clock	0	0	0	0	0	*	*	*	*	*	*
Erase All[3]	Erase all FLASH data	05	3Ah	SP +3	NA	NA	Clock	0	0	0	0	0	*	*	*	*	*	*
Table Read	Read device type code	06	3Ah	SP +3	Tbl ID	NA	NA	NA	NA	NA	TV (0)	TV (1)	TV (2)	TV (3)	TV (4)	TV (5)	TV (6)	TV (7)
Checksum	Calculate FLASH checksum for data range specified	07	3Ah	SP +3	Blk Counter	NA	NA	0	0	0	CSH	CSL	*	*	*	*	*	*
Calibrate[5]	Sets user-writable registers to default	08	3Ah	SP +3	NA	NA	NA				0	0	*	*	*	*	*	*

1. This is a software-only reset.
2. This operation should only be invoked by calling a function in the FlashBlock library. **Device specifications are no longer guaranteed if this function is directly called by the user's code**.
3. This function can only be invoked by the device programmer, not by user's code.
4. The address is hard coded by algorithm.
5. User-writeable registers include Main Oscillator Trim (IMO_TR), Internal Low Speed Oscillator Trim (ILO_TR), and Bandgap Trim (BDG_TR).

Notes:

NA: Not applicable

*: Indeterminate

Blk ID: Number of 64-byte block within FLASH memory space

Clock: CPU system clocking signal value

Pointer: Address of first byte of 64-byte block within SRAM memory space

TV: Table value

11.10.1 Data File Read

The user's data file should be read into the programmer. The checksum should be calculated by the programmer for each record and compared to the record checksum stored in the file for each record. If there is an error, a message should be sent to the user explaining that the file has a checksum error and the programming should not be allowed to continue.

11.10.2 Programmer Flow

The following sequence (with descriptions) is the main flow used to program the devices: (Note that failure at any step will result in termination of the flow and an error message to the device programmer's operator.)

11.10.2.1 Verify Silicon ID

The silicon ID is read and verified against the expected value. If it is not the expected value, then the device is failed and an error message is sent to the device programmer's operator.

This test will detect a bad connection to the programmer or an incorrect device selection on the programmer.

The silicon ID test is required to be first in the flow and cannot be bypassed. The sequence is as follows:

```
Set Vcc=0V
Set SDATA=HighZ
Set SCLK=VILP
Set Vcc=Vccp
Start the programmer's SCLK driver
"free running"
WAIT-AND-POLL
ID-SETUP
WAIT-AND-POLL
READ-ID-WORD
```

Notes: See "DC Specifications" table in section 13 for value of Vccp and VILP. See "AC Specifications" table in section 13 for value of frequency for the SCLK driver (Fsclk).

11.10.2.2 Erase

The Flash memory is erased. This is accomplished by the following sequence:

```
SET-CLK-FREQ(num_MHz_times_5)
Erase All
WAIT-AND-POLL
```

11.10.2.3 Program

The Flash is programmed with the contents of the user's programming file. This is accomplished by the following sequence:

```
For num_block = 0 to max_data_block
For address =0 to 63
WRITE-BYTE(address,data):
End for address loop
SET-CLK-FREQ(num_MHz_times_5)
SET-BLOCK-NUM(num_block)
PROGRAM-BLOCK
WAIT-AND-POLL
End for num_block loop
```

11.10.2.4 Verify (at Low Vcc and High Vcc)

The device data is read out to compare to the data in the user's programming file. This is accomplished by the following sequence:

```
For num_block = 0 to max_data_block
SET-BLOCK-NUM (num_block)
VERIFY-SETUP
Wait & POLL the SDATA for a high to
low transition
For address =0 to max_byte_per_block
READ-BYTE(address,data)
End for address loop
End for num_block loop
```

Note: This should be done 2 times; once at Vcc=Vcclv and once at Vcc=Vcchv.

11.10.2.5 Set Security

The security operation protects certain blocks from being read or changed. This is done at the end of the flow so that the security does not interfere with the verify step. Security is set with the following sequence:

```
For address =0 to 63
WRITE-SECURITY-BYTE(address,data):
End for address loop
SET-CLK-FREQ(num_MHz_times_5)
SECURE
WAIT-AND-POLL
```

Note: This sequence is done at Vcc=Vccp.

2. The temperature rise from junction to ambient is package specific. (See Table 122 on page 149 for thermal impedances of available packages.) User must limit power consumption to comply with this requirement.

Table 103: Temperature Specifications

Symbol	Temperature Specifications	Minimum	Typical	Maximum	Unit
T_A	Ambient Temperature	-40	24	+85	^oC
T_J	Junction Temperature	-40		100	^oC

13.2.1.2 3.3V Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 3.3V +/- 10% and -40°C <= T_A <= 85°C. The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switch Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only. For 5V operation, see Table 105 on page 130.

Table 106: 3.3V DC Operational Amplifier Specifications

Symbol	3.3V DC Operational Amplifier Specifications	Minimum	Typical	Maximum	Unit
	Input Offset Voltage (Absolute Value)	-	7	30	mV
	Average Input Offset Voltage Drift	-	+24	-	µV/°C
	Input Leakage Current[1]	-	2	700	nA
	Input Capacitance[2]	.32	.36	.42	pF
	Common Mode Voltage Range[3]	.5	-	V_{cc} - 1.0	VDC
	Common Mode Rejection Ratio	80	-	-	dB
	Open Loop Gain	80	-	-	dB
	High Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 V_{cc} - .4 V_{cc} - .4 V_{cc} - .4	 - - -	 - - -	 V V V
	Low Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 - - -	 - - -	 0.1 0.1 0.1	 V V V
	Supply Current (Including Associated AGND Buffer) Bias = Low Bias = Medium Bias = High	 - - -	 80 112 320	 200 300 800	 µA µA µA
	Supply Voltage Rejection Ratio	60	-	-	dB

1. The leakage current includes the Analog Continuous Time PSoC block mux and the analog input mux. The leakage related to the General Purpose I/O pins is not included here.
2. The Input Capacitance includes the Analog Continuous Time PSoC block mux and the analog input mux. The capacitance of the General Purpose I/O pins is not included here.
3. The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer

Table 120: 3.3V AC Analog Output Buffer Specifications

Symbol	3.3V AC Analog Output Buffer Specifications	Minimum	Typical	Maximum	Unit
	Rising Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	3.2	µs
	Bias = High	-	-	3.2	µs
	Falling Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.6	µs
	Bias = High	-	-	2.6	µs
	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load				
	Bias = Low	.5	-	-	V/µs
	Bias = High	.5	-	-	V/µs
	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load				
	Bias = Low	.5	-	-	V/µs
	Bias = High	.5	-	-	V/µs
	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load				
	Bias = Low	1.3	-	-	MHz
	Bias = High	1.3	-	-	MHz
	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load				
	Bias = Low	360	-	-	kHz
	Bias = High	360	-	-	kHz

13.3.3 AC Programming Specifications

Table 121: AC Programming Specifications

Symbol	AC Programming Specifications	Minimum	Typical	Maximum	Unit
T_{rsclk}	Rise Time of SCLK	1	-	20	ns
T_{fsclk}	Fall Time of SCLK	1	-	20	ns
T_{ssclk}	Data Set up Time to Rising Edge of SCLK	25	-	-	ns
T_{hsclk}	Data Hold Time from Rising Edge of SCLK	25	-	-	ns
F_{sclk}	Frequency of SCLK	2	-	20	MHz
T_{eraseb}	Flash Erase Time (Block)	-	10	-	ms
T_{erasef}	Flash Erase Time (Full)	-	40	-	ms
T_{write}	Flash Block Write Time	2	10	20	ms