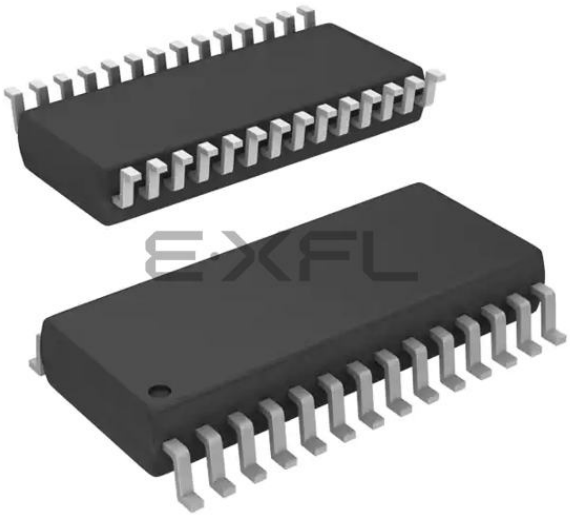

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26443-24si

Table of Contents

1.0 Functional Overview

The CPU heart of this next generation family of microcontrollers is a high performance, 8-bit, M8C Harvard architecture microprocessor. Separate program and memory busses allow for faster overall throughput. Processor clock speeds to 24 MHz are available. The processor may also be run at lower clock speeds for power-sensitive applications. A rich instruction set allows for efficient low-level language support.

All devices in this family include both analog and digital configurable peripherals (PSoC blocks). These blocks enable the user to define unique functions during configuration of the device. Included are twelve analog PSoC blocks and eight digital PSoC blocks. Potential applications for the digital PSoC blocks are timers, counters, UARTs, CRC generators, PWMs, and other functions. The analog PSoC blocks can be used for SAR ADCs, Multi-slope ADCs, programmable gain amplifiers, programmable filters, DACs, and other functions. Higher order User Modules such as modems, complex motor controllers, and complete sensor signal chains can be created from these building blocks. This allows for an unprecedented level of flexibility and integration in microcontroller-based systems.

A Multiplier/Accumulator (MAC) is available on all devices in this family. The MAC is implemented on this device as a peripheral that is mapped into the register space. When an instruction writes to the MAC input registers, the result of an 8x8 multiply and a 32-bit accumulate are available to be read from the output registers on the next instruction cycle.

The number of general purpose I/Os available in this family of parts range from 6 to 44. Each of these I/O pins has a variety of programmable options. In the output mode, the user can select the drive strength desired. Any pin can serve as an interrupt source, and can be selected to trigger on positive edges, negative edges, or any change. Digital signal sources can be routed directly from a pin to the digital PSoC blocks. Some pins have additional capability to route analog signals to the analog PSoC blocks.

Multiple oscillator options are available for use in clocking the CPU, analog PSoC blocks and digital PSoC blocks. These options include an internal main oscillator running at 48/24 MHz, an external crystal oscillator for use with a 32.768 kHz watch crystal, and an internal low-speed oscillator for use in clocking the PSoC blocks and the Watchdog/Sleep timer. User selectable clock divisors allow for optimizing code execution speed and power trade-offs.

The different device types in this family provide various amounts of code and data memory. The code space ranges in size from 4K to 16K bytes of user programmable Flash memory. This memory can be programmed serially in either a programming Pod or on the user board. The endurance on the Flash memory is 50,000 erase/write cycles. The data space is 256 bytes of user SRAM.

A powerful and flexible protection model secures the user's sensitive information. This model allows the user to selectively lock blocks of memory for read and write protection. This allows partial code updates without exposing proprietary information.

Devices in this family range from 8 pins through 48 pins in PDIP, SOIC and SSOP packages.

1.1 Key Features

Table 1: Device Family Key Features

	CY8C25122	CY8C26233	CY8C26443	CY8C26643
Operating Frequency	93.7kHz - 24MHz	93.7kHz - 24MHz	93.7kHz - 24MHz	93.7kHz - 24MHz
Operating Voltage	3.0 - 5.25V	3.0 - 5.25V	3.0 - 5.25V	3.0 - 5.25V
Program Memory (KBytes)	4	8	16	16
Data Memory (Bytes)	256	256	256	256
Digital PSoC Blocks	8	8	8	8
Analog PSoC Blocks	12	12	12	12
I/O Pins	6	16	24	40/44
External Switch Mode Pump	No	Yes	Yes	Yes
Available Packages	8 PDIP	20 PDIP	28 PDIP	48 PDIP
		20 SOIC	28 SOIC	48 SSOP
		20 SSOP	28 SSOP	44 TQFP

2.0 CPU Architecture

2.1 Introduction

This family of microcontrollers is based on a high performance, 8-bit, Harvard architecture microprocessor. Five registers control the primary operation of the CPU core. These registers are affected by various instructions, but are not directly accessible through the register space by the user. For more details on addressing with the register space, see section 4.0.

Table 7: CPU Registers and Mnemonics

Register	Mnemonic
Flags	CPU_F
Program Counter	CPU_PC
Accumulator	CPU_A
Stack Pointer	CPU_SP
Index	CPU_X

The 16 bit Program Counter Register (CPU_PC) allows for direct addressing of the full 16 Kbytes of program memory space available in the largest members of this family. This forms one contiguous program space, and no paging is required.

The Accumulator Register (CPU_A) is the general-purpose register that holds the results of instructions that specify any of the source addressing modes.

The Index Register (CPU_X) holds an offset value that is used in the indexed addressing modes. Typically, this is used to address a block of data within the data memory space.

The Stack Pointer Register (CPU_SP) holds the address of the current top-of-stack in the data memory space. It is affected by the PUSH, POP, LCALL, CALL, RETI, and RET instructions, which manage the software stack. It can also be affected by the SWAP and ADD instructions.

The Flag Register (CPU_F) has three status bits: Zero Flag bit [1]; Carry Flag bit [2]; Supervisory State bit [3]. The Global Interrupt Enable bit [0] is used to globally enable or disable interrupts. An extended I/O space address, bit [4], is used to determine which bank of the register space is in use. The user cannot manipulate the Supervisory State status bit [3]. The flags are affected by arithmetic, logic, and shift operations. The manner in which each flag is changed is dependent upon the instruction being executed (i.e., AND, OR, XOR... See Table 23 on page 25).

7.2.2 24V1/24V2 Frequency Selection

The following table shows the resulting frequencies for 24V1 and 24V2 based on the value written to the OSC_CR1 register.

Table 42: 24V1/24V2 Frequency Selection

Reg. Value	24V1 MHz	24V2 kHz	Reg. Value	24V1 MHz	24V2 kHz	Reg. Value	24V1 MHz	24V2 kHz	Reg. Value	24V1 MHz	24V2 kHz
00	24.00	24000.00	40	4.80	4800.00	80	2.67	2666.67	C0	1.85	1846.15
01	24.00	12000.00	41	4.80	2400.00	81	2.67	1333.33	C1	1.85	923.08
02	24.00	8000.00	42	4.80	1600.00	82	2.67	888.89	C2	1.85	615.38
03	24.00	6000.00	43	4.80	1200.00	83	2.67	666.67	C3	1.85	461.54
04	24.00	4800.00	44	4.80	960.00	84	2.67	533.33	C4	1.85	369.23
05	24.00	4000.00	45	4.80	800.00	85	2.67	444.44	C5	1.85	307.69
06	24.00	3428.57	46	4.80	685.71	86	2.67	380.95	C6	1.85	263.74
07	24.00	3000.00	47	4.80	600.00	87	2.67	333.33	C7	1.85	230.77
08	24.00	2666.67	48	4.80	533.33	88	2.67	296.30	C8	1.85	205.13
09	24.00	2400.00	49	4.80	480.00	89	2.67	266.67	C9	1.85	184.62
0A	24.00	2181.82	4A	4.80	436.36	8A	2.67	242.42	CA	1.85	167.83
0B	24.00	2000.00	4B	4.80	400.00	8B	2.67	222.22	CB	1.85	153.85
0C	24.00	1846.15	4C	4.80	369.23	8C	2.67	205.13	CC	1.85	142.01
0D	24.00	1714.29	4D	4.80	342.86	8D	2.67	190.48	CD	1.85	131.87
0E	24.00	1600.00	4E	4.80	320.00	8E	2.67	177.78	CE	1.85	123.08
0F	24.00	1500.00	4F	4.80	300.00	8F	2.67	166.67	CF	1.85	115.38
10	12.00	12000.00	50	4.00	4000.00	90	2.40	2400.00	D0	1.71	1714.29
11	12.00	6000.00	51	4.00	2000.00	91	2.40	1200.00	D1	1.71	857.14
12	12.00	4000.00	52	4.00	1333.33	92	2.40	800.00	D2	1.71	571.43
13	12.00	3000.00	53	4.00	1000.00	93	2.40	600.00	D3	1.71	428.57
14	12.00	2400.00	54	4.00	800.00	94	2.40	480.00	D4	1.71	342.86
15	12.00	2000.00	55	4.00	666.67	95	2.40	400.00	D5	1.71	285.71
16	12.00	1714.29	56	4.00	571.43	96	2.40	342.86	D6	1.71	244.90
17	12.00	1500.00	57	4.00	500.00	97	2.40	300.00	D7	1.71	214.29
18	12.00	1333.33	58	4.00	444.44	98	2.40	266.67	D8	1.71	190.48
19	12.00	1200.00	59	4.00	400.00	99	2.40	240.00	D9	1.71	171.43
1A	12.00	1090.91	5A	4.00	363.64	9A	2.40	218.18	DA	1.71	155.84
1B	12.00	1000.00	5B	4.00	333.33	9B	2.40	200.00	DB	1.71	142.86
1C	12.00	923.08	5C	4.00	307.69	9C	2.40	184.62	DC	1.71	131.87
1D	12.00	857.14	5D	4.00	285.71	9D	2.40	171.43	DD	1.71	122.45
1E	12.00	800.00	5E	4.00	266.67	9E	2.40	160.00	DE	1.71	114.29
1F	12.00	750.00	5F	4.00	250.00	9F	2.40	150.00	DF	1.71	107.14
20	8.00	8000.00	60	3.43	3428.57	A0	2.18	2181.82	E0	1.60	1600.00
21	8.00	4000.00	61	3.43	1714.29	A1	2.18	1090.91	E1	1.60	800.00
22	8.00	2666.67	62	3.43	1142.86	A2	2.18	727.27	E2	1.60	533.33
23	8.00	2000.00	63	3.43	857.14	A3	2.18	545.45	E3	1.60	400.00
24	8.00	1600.00	64	3.43	685.71	A4	2.18	436.36	E4	1.60	320.00
25	8.00	1333.33	65	3.43	571.43	A5	2.18	363.64	E5	1.60	266.67
26	8.00	1142.86	66	3.43	489.80	A6	2.18	311.69	E6	1.60	228.57
27	8.00	1000.00	67	3.43	428.57	A7	2.18	272.73	E7	1.60	200.00
28	8.00	888.89	68	3.43	380.95	A8	2.18	242.42	E8	1.60	177.78
29	8.00	800.00	69	3.43	342.86	A9	2.18	218.18	E9	1.60	160.00
2A	8.00	727.27	6A	3.43	311.69	AA	2.18	198.35	EA	1.60	145.45
2B	8.00	666.67	6B	3.43	285.71	AB	2.18	181.82	EB	1.60	133.33
2C	8.00	615.38	6C	3.43	263.74	AC	2.18	167.83	EC	1.60	123.08
2D	8.00	571.43	6D	3.43	244.90	AD	2.18	155.84	ED	1.60	114.29
2E	8.00	533.33	6E	3.43	228.57	AE	2.18	145.45	EE	1.60	106.67
2F	8.00	500.00	6F	3.43	214.29	AF	2.18	136.36	EF	1.60	100.00
30	6.00	6000.00	70	3.00	3000.00	B0	2.00	2000.00	F0	1.50	1500.00
31	6.00	3000.00	71	3.00	1500.00	B1	2.00	1000.00	F1	1.50	750.00
32	6.00	2000.00	72	3.00	1000.00	B2	2.00	666.67	F2	1.50	500.00
33	6.00	1500.00	73	3.00	750.00	B3	2.00	500.00	F3	1.50	375.00
34	6.00	1200.00	74	3.00	600.00	B4	2.00	400.00	F4	1.50	300.00
35	6.00	1000.00	75	3.00	500.00	B5	2.00	333.33	F5	1.50	250.00
36	6.00	857.14	76	3.00	428.57	B6	2.00	285.71	F6	1.50	214.29
37	6.00	750.00	77	3.00	375.00	B7	2.00	250.00	F7	1.50	187.50
38	6.00	666.67	78	3.00	333.33	B8	2.00	222.22	F8	1.50	166.67
39	6.00	600.00	79	3.00	300.00	B9	2.00	200.00	F9	1.50	150.00
3A	6.00	545.45	7A	3.00	272.73	BA	2.00	181.82	FA	1.50	136.36
3B	6.00	500.00	7B	3.00	250.00	BB	2.00	166.67	FB	1.50	125.00
3C	6.00	461.54	7C	3.00	230.77	BC	2.00	153.85	FC	1.50	115.38
3D	6.00	428.57	7D	3.00	214.29	BD	2.00	142.86	FD	1.50	107.14
3E	6.00	400.00	7E	3.00	200.00	BE	2.00	133.33	FE	1.50	100.00
3F	6.00	375.00	7F	3.00	187.5	BF	2.00	125.00	FF	1.50	93.75

8.6 GPIO Interrupt

GPIO Interrupts are polarity configurable and pin-wise maskable (within each Port's pin configuration registers). They all share the same interrupt priority and vector.

Any general purpose I/O can be used as an interrupt source. The GPIO bit in the General Interrupt Mask Register (INT_MSK0) must be set to enable pin interrupts, as well as the enable bits for each pin, which are located in the Port x Interrupt Enable Registers (PRTxIE). There are user selectable options to generate an interrupt on 1) any change from the last read state, 2) rising edge, and 3) falling edge.

When Interrupt on Change is selected, the state of the GPIO pin is stored when the port is read. Changes from this state will then assert the interrupt, if enabled.

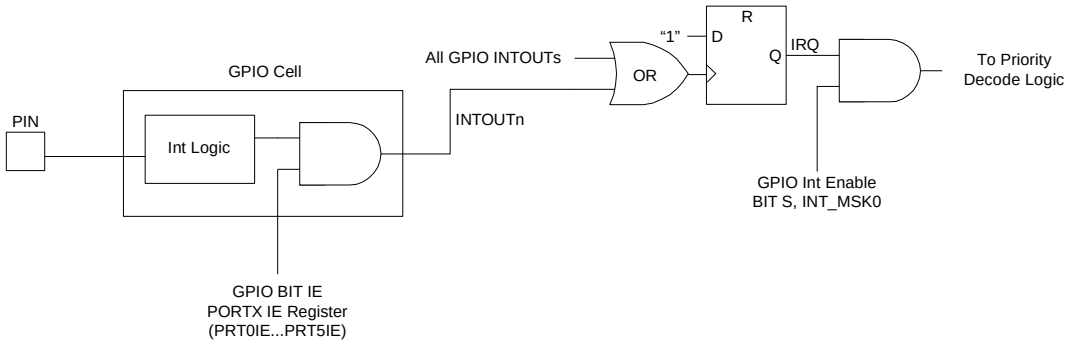

Figure 11: GPIO Interrupt Enable Diagram

For a GPIO interrupt to occur, the following steps must be taken:

1. The pin Drive Mode must be set so the pin can be an input.
2. The pin must be enabled to generate an interrupt by setting the appropriate bit in the Port interrupt Enable Register (PRTxIE).
3. The edge type for the interrupt must be set in the Port Interrupt Control 0 and Control 1 Registers (PRTxIC0 and PRTxIC1). Edge type must be set to a value other than 00.
4. The GPIO bit must be set in the General Interrupt Mask Register (INT_MSK0).
5. The Global Interrupt Enable bit must be set.
6. Because the GPIO interrupts all share the same interrupt vector, the source for the GPIO interrupt must be cleared before any other GPIO interrupt will occur (i.e., the OR gate in Figure 11: "ors" all of the INTOUTn signals together). If any of the INTOUTn signals are high, the flip-flop in Figure 11: will not see a rising edge and no IRQ will occur.

Digital Communications Type A Block 06 Input Register (DCA06IN, Address = Bank 1, 39h)
Digital Communications Type A Block 07 Input Register (DCA07IN, Address = Bank 1, 3Dh)

The Data/Enable source select [3:0] bits select between multiple inputs to the Digital PSoC Blocks. These inputs serve as Clock Enables or Data Input depending on the Digital PSoC Block's programmed function. If "Chain Function to Previous" data input is selected for Data/Enable then the selected Digital PSoC block receives its Data, Enable, Zero Detect, and all chaining information from the previous digital PSoC block. The data inputs that are selected from the GPIO pins (through the Global Input Bus) are synchronized to the 24 MHz clock. The following table shows the function dependent meaning of the data input.

Table 49: Digital Function Data Input Definitions

Function	Data Input
Timer	Positive Edge Capture
Counter	Count Enable (Active High)
CRC	Data Input
PRS	N/A
Deadband	Kill Signal (Active High)
TX UART	N/A
RX UART	RX Data In
SPI Master	MISO (Master In/Slave Out)
SPI Slave	MOSI (Master Out/Slave In)

The Clock[3:0] bits select multiple sources for the clock for each digital PSoC block. The sources for each digital PSoC block clock are selected from the Global Input Bus, System Clocks, and other neighboring digital PSoC blocks. As shown in the table, Digital PSoC Blocks 0-3 can interface to Global I/Os 00-03, and Digital PSoC block 04-07 can interface to Global I/Os 4-7. It is important to note that clock inputs selected from the GPIO pins (through the Global Input Bus) are not synchronized. This may cause indeterminate results if the CPU reads a block register as it is changing in response to an external clock. CPU reads must be manually synchronized, either through the block interrupt, or through a multiple read and voting scheme.

9.2.3 Digital Basic Type A / Communications Type A Block xx Output Register

The digital PSoC block's outputs can be selected to drive associated Global Output Bus signals via the Output Select bits. In addition, the output drive can be selectively enabled in this register. The SPI Slave has an auxiliary input which is also controlled by selections in this register.

9.3.5 Digital Communications Type A Block xx Control Register 0 When Used as UART Receiver

Table 57: Digital Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bit Name	Parity Error	Overrun	Framing Error	RX Active	RX Reg Full	Parity Type	Parity Enable	Enable

Bit 7: **Parity Error**
0 = Indicates no parity error detected in the last byte received
1 = Indicates a parity error detected in the last byte received
Reset when this register is read

Bit 6: **Overrun**
0 = Indicates that no overrun has taken place
1 = Indicates the RX Data register was overwritten with a new byte before the previous one had been read
Reset when this register is read

Bit 5: **Framing Error**
0 = Indicates correct stop bit
1 = Indicates a missing STOP bit
Reset when this register is read

Bit 4: **RX Active**
0 = Indicates no communication currently in progress
1 = Indicates a start bit has been received and a byte is currently being received

Bit 3: **RX Reg Full**
0 = Indicates the RX Data register is empty
1 = Indicates a byte has been loaded into the RX Data register
Interrupt source for RXUART. Reset when the RX Data register is read (Data Register 2)

Bit 2: **Parity Type**
0 = Even
1 = Odd

Bit 1: **Parity Enable**
0 = Parity Disabled
1 = Parity Enabled

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

10.5 Analog PSoC Block Clocking Options

All analog PSoC blocks in a particular Analog Column share the same clock signal. Choosing the clocking for an analog PSoC block is a two-step process.

1. First, if the user wants to use the **ACLK0** and **ACLK1** system-clocking signals, the digital PSoC blocks that serve as the source for these signals must be selected. This selection is made in the Analog Clock Select Register (CLK_CR1).
2. Next, the user must select the source for the **Acolumn0**, **Acolumn1**, **Acolumn2**, and **Acolumn3** system-clocking signals. The user will choose the clock for Acolumnx[1:0] bits in the Analog Column Clock Select Register (CLK_CR0). Each analog PSoC block in a particular Analog Column is clocked from the **Acolumn[x]** system-clocking signal for that column. (Note that the Acolumn[x] signals have a 1:4 divider on them.)

10.5.1 Analog Column Clock Select Register

Table 64: Analog Column Clock Select Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Acolumn3 [1]	Acolumn3 [0]	Acolumn2 [1]	Acolumn2 [0]	Acolumn1 [1]	Acolumn1 [0]	Acolumn0 [1]	Acolumn0 [0]

Bit [7:6]: **Acolumn3 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [5:4]: **Acolumn2 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [3:2]: **Acolumn1 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Bit [1:0]: **Acolumn0 [1:0]**
0 0 = 24V1
0 1 = 24V2
1 0 = ACLK0
1 1 = ACLK1

Analog Column Clock Select Register (CLK_CR0, Address = Bank 1, 60h)

10.7.2.2 Analog Continuous Time Block xx Control 1 Register

The PMux bits control the multiplexing of inputs to the non-inverting input of the op-amp. There are physically only 7 inputs.

The 8th code (111) will leave the input floating. This is not desirable, and should be avoided.

The NMux bits control the multiplexing of inputs to the inverting input of the op-amp. There are physically only 7 inputs.

CompBus controls a tri-state buffer that drives the comparator logic. If no PSoC block in the analog column is driving the comparator bus, it will be driven low externally to the blocks.

AnalogBus controls the analog output bus. A CMOS switch connects the op-amp output to the analog bus.

Table 67: Analog Continuous Time Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	NMux2	NMux1	NMux0	PMux2	PMux1	PMux0

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable analog bus driven by this block
1 = Enable analog bus driven by this block
Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable comparator bus driven by this block
1 = Enable comparator bus driven by this block

Bit [5:3]: **NMux [2:0]** Encoding for negative input select

	ACA00	ACA01	ACA02	ACA03
0 0 0 =	ACA01	ACA00	ACA03	ACA02
0 0 1 =	AGND	AGND	AGND	AGND
0 1 0 =	REFLO	REFLO	REFLO	REFLO
0 1 1 =	REFHI	REFHI	REFHI	REFHI
1 0 0[1] =	ACA00	ACA01	ACA02	ACA03
1 0 1 =	ASA10	ASB11	ASA12	ASB13
1 1 0 =	ASB11	ASA10	ASB13	ASA12
1 1 1 =	Reserved	Reserved	Reserved	Reserved

Bit [2:0]: **PMux [2:0]** Encoding for positive input select

	ACA00	ACA01	*ACA02*	ACA03
0 0 0 =	REFLO	ACA02	ACA01	REFLO
0 0 1 =	Port Inputs	Port Inputs	Port Inputs	Port Inputs
0 1 0 =	ACA01	ACA00	ACA03	ACA02
0 1 1 =	AGND	AGND	AGND	AGND
1 0 0 =	ASA10	ASB11	ASA12	ASB13
1 0 1 =	ASB11	ASA10	ASB13	ASA12
1 1 0 =	ABUS0	ABUS1	ABUS2	ABUS3
1 1 1 =	Reserved	Reserved	Reserved	Reserved

1. This in fact is the feedback input of the MUX.

Analog Continuous Time Block 00 Control 1 Register (ACA00CR1, Address = Bank 0/1, 72h)
Analog Continuous Time Block 01 Control 1 Register (ACA01CR1, Address = Bank 0/1, 76h)
Analog Continuous Time Block 02 Control 1 Register (ACA02CR1, Address = Bank 0/1, 7Ah)
Analog Continuous Time Block 03 Control 1 Register (ACA03CR1, Address = Bank 0/1, 7Eh)

10.8 Analog Switch Cap Type A PSoC Blocks

10.8.1 Introduction

The Analog Switch Cap Type A PSoC blocks are built around an operational amplifier. There are several analog muxes that are controlled by register-bit settings in the control registers that determine the signal topology inside the block. There are also four arrays of unit value capacitors that are located in the feedback path for the op-amp, and are switched by two phase clocks, PHI1 and PHI2. These four capacitor arrays are labeled A Cap Array, B Cap Array, C Cap Array, and F Cap Array. There is also an analog comparator connected to the output OUT, which converts analog comparisons into digital signals.

There are three discrete outputs from this block. These outputs are:

1. The analog output bus (ABUS), which is an analog bus resource that is shared by all of the analog blocks in the analog column for that block.

2. The comparator bus (CBUS), which is a digital bus that is a resource that is shared by all of the analog blocks in a column for that block.

3. The output bus (OUT), which is an analog bus resource that is shared by all of the analog blocks in a column and connects to one of the analog output buffers, to send a signal externally to the device.

SC Integrator Block A supports Delta-Sigma, Successive Approximation and Incremental A/D Conversion, Capacitor DACs, and SC filters. It has three input arrays of binarily-weighted switched capacitors, allowing user programmability of the capacitor weights. This provides summing capability of two (CDAC) scaled inputs, and a non-switched capacitor input. Since the input of SC Block A has this additional switched capacitor, it is configured for the input stage of such a switched capacitor biquad filter. When followed by an SC Block B Integrator, this combination of blocks can be used to provide a full Switched Capacitor Biquad.

Table 71: Analog Switch Cap Type A Block xx Control 2 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	AutoZero	CCap[4]	CCap[3]	CCap[2]	CCap[1]	CCap[0]

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable output to analog column bus
1 = Enable output to analog column bus
(The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASA10CR0, ASA12CR0, ASA21CR0, ASA23CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the signal that is output to the analog column bus is selected by the ClockPhase bit. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus.)

Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable output to comparator bus
1 = Enable output to comparator bus

Bit 5: **AutoZero** Bit for controlling gated switches
0 = Shorting switch is not active. Input cap branches shorted to op-amp input
1 = Shorting switch is enabled during internal PHI1. Input cap branches shorted to analog ground during internal PHI1 and to op-amp input during internal PHI2.

Bit [4:0]: **CCap [4:0]** Binary encoding for 32 possible capacitor sizes for C Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type A Block 10 Control 2 Register (ASA10CR2, Address = Bank 0/1, 82h)
Analog Switch Cap Type A Block 12 Control 2 Register (ASA12CR2, Address = Bank 0/1, 8Ah)
Analog Switch Cap Type A Block 21 Control 2 Register (ASA21CR2, Address = Bank 0/1, 96h)
Analog Switch Cap Type A Block 23 Control 2 Register (ASA23CR2, Address = Bank 0/1, 9Eh)

10.12 Analog I/O

10.12.1 Analog Input Muxing

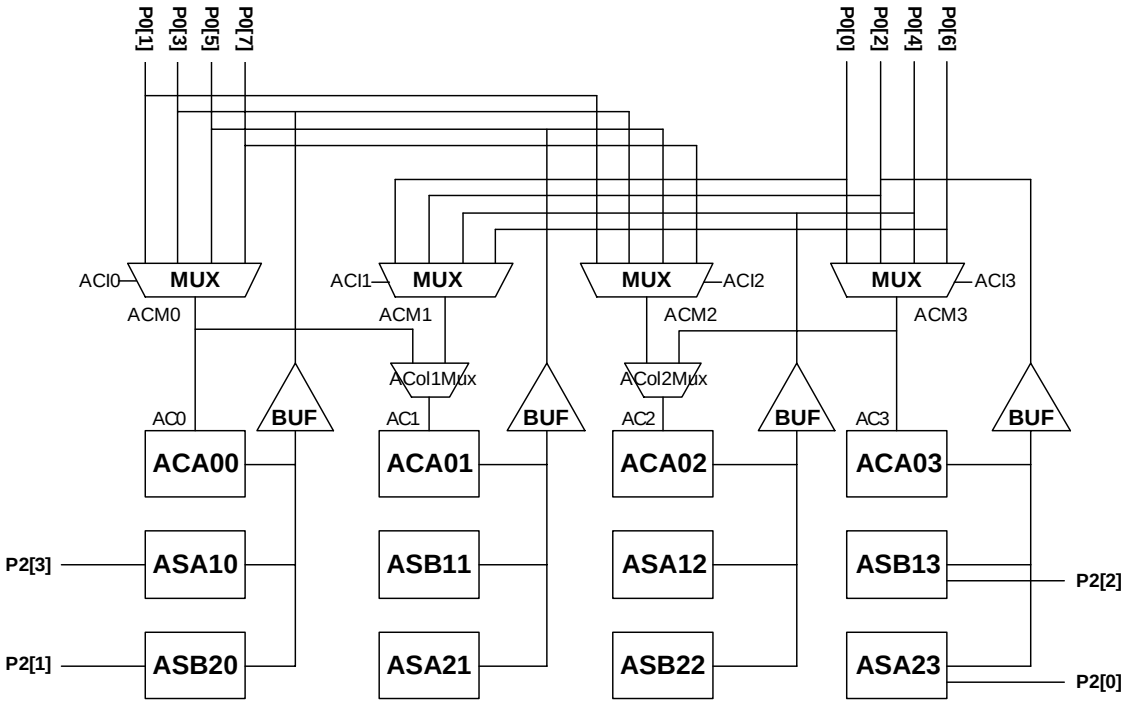

Figure 27: Analog Input Muxing

10.12.2 Analog Input Select Register

This register controls the analog muxes that feed signals in from port pins into each Analog Column. Each of the Analog Columns can have up to four port bits connected to its muxed input. Analog Columns 01 and 02 (ACI1 and ACI2) have additional muxes that allow selection between separate column multiplexers (see Analog Input Muxing diagram above). The AC1Mux and AC2Mux bit fields control the bits for those muxes and are located in the Analog Output Buffer Control Register (ABF_CR). There are four additional analog inputs that go directly into the Switch Capacitor PSoC blocks.

10.12.4 Analog Output Buffer Control Register

Table 81: Analog Output Buffer Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	--	W
Bit Name	ACol1Mux	ACol2Mux	ABUF1EN	ABUF2EN	ABUF0EN	ABUF3EN	Reserved	PWR

Bit 7: **ACol1Mux**
0 = Set column 1 input to column 1 input mux output
1 = Set column 1 input to column 0 input mux output

Bit 6: **ACol2Mux**
0 = Set column 2 input to column 2 input mux output
1 = Set column 2 input to column 3 input mux output

Bit 5: **ABUF1EN** Enables the analog output buffer for Analog Column 1 (Pin P0[5])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 4: **ABUF2EN** Enables the analog output buffer for Analog Column 2 (Pin P0[4])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 3: **ABUF0EN** Enables the analog output buffer for Analog Column 0 (Pin P0[3])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 2: **ABUF3EN** Enables the analog output buffer for Analog Column 3 (Pin P0[2])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit [1]: **Reserved** Must be left as 0

Bit [0]: **PWR** Determines power level of all output buffers
0 = Low output power
1 = High output power

Analog Output Buffer Control Register (ABF_CR, Address = Bank 1, 62h)

10.13 Analog Modulator

The user has the capability to use the Analog Switch Cap Type A PSoC Blocks in Columns 0 and 2 as amplitude modulators. The Analog Modulator Control Register (AMD_CR) allows the user to select the appropriate modulating signal. When the modulating signal is low, the polarity follows the setting of the ASign bit set in the Analog Switch Cap Type A Control 0 Register (ASAxxCR0). When this signal is high, the normal gain polarity of the PSoC block is inverted.

11.7 Internal Voltage Reference

An internal bandgap voltage reference source is provided on-chip. This reference is used for the Supply Voltage Monitor, and can also be accessed by the user as a reference voltage for analog operations. There is a Bandgap Oscillator Trim Register (BDG_TR) used to calibrate this reference into specified tolerance. Factory-programmed trim values are available for 5.0V and 3.3V operation. The 5.0V value is loaded in the BDG_TR register upon reset. This register must be adjusted when operating voltage outside the range for which factory calibration was set. Changing the factory-programmed trim value is done using the Table Read Supervisor Call routine, and is documented in 11.8.

Table 97: Bandgap Trim Register

Bit #	7	6	5	4	3	2	1	0
POR	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]
Read/Write	W	W	W	W	W	W	W	W
Bit Name	FMRD	BGT[2]	BGT[1]	BGT[0]	BGO[3]	BGO[2]	BGO[1]	BGO[0]

Bit 7: **FMRD**
0 = Enable voltage divider between BG and Flash (User must not use other than this setting)
1 = Disable voltage divider between BG and Flash (Test purposes only)

Bit [6:4]: **BGT [2:0]** Provides Temperature Curve compensation

Bit [3:0]: **BGO [3:0]** Provides +/- 5% Offset Trim to center Vbg to 1.30V

1. FS = Factory set trim value

Bandgap Trim Register (BDG_TR, Address = Bank 1, EAh)

11.8 Supervisor ROM/System Supervisor Call Instruction

The parts in this family have a Supervisor ROM to manage the programming, erasure, and protection of the on-chip Flash user program space. The Supervisor ROM also gives the user the capability to read the internal product ID, access factory trim values, as well as calculate checksums on blocks of the Flash memory space.

The System Supervisor Call instruction (SSC, opcode/byte 00h) provides the method for the user to access the pre-existing routines in the Supervisor ROM to implement these functions. This instruction sets the Flags Register (CPU_F) bit 3 to 1 and performs an interrupt to address 0000 into the Supervisory ROM. The flag and old PC are pushed onto the Stack. The fact that the flag pushed has F[3] = 1 is irrelevant as the `RETI` instruction always clears F[3]. The Supervisory code at 0000 does a `JACC` table lookup based on the Accumulator value, which is effectively another level of instruction encoding. This service table implements the vectors to the various supervisory functions. The user must set several parameters when utilizing these functions. The parameters are written to 5 bytes of an 8-byte block near the top of RAM memory space.

Access to these functions must be through the Flash APIs provided in PSoC Designer and described in Application Note AN2015.

The following table documents each function, as well as the required parameter values:

12.2 Integrated Development Environment Subsystems

12.2.1 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

12.2.2 Device Editor

PSoC Designer has several main functions. The Device Editor subsystem lets the user select different onboard analog and digital component configurations for the PSoC blocks. PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at runtime. PSoC Designer can print out a configuration sheet for given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

12.2.3 Assembler

The included CYASM macro assembler supports the M8C microcontroller instruction set and generates a load file ready for device programming or system debugging using the ICE hardware.

12.2.4 C Language Software Development

A C language compiler supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It includes a built-in macro assembler allowing assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

The compiler comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

12.2.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and write program and data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

12.3 Hardware Tools

12.3.1 In-Circuit Emulator

A low cost, high functionality ICE is available for development support. This hardware has the capability to program single devices.

13.2.8 DC Programming Specifications

Table 115: DC Programming Specifications

Symbol	DC Programming Specifications	Minimum	Typical	Maximum	Unit
I_{ccp}	Supply Current During Programming or Verify	-	5	20	mA
V_{ilp}	Input Low Voltage During Programming or Verify	-	-	0.8	V
V_{ihp}	Input High Voltage During Programming or Verify	2.2	-	-	V
I_{ilp}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	-	-	0.2	mA
I_{ihp}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	-	-	1.5[1]	mA
V_{olv}	Output Low Voltage During Programming or Verify	-	-	V_{ss} + 0.75	V
V_{ohv}	Output High Voltage During Programming or Verify	V_{cc} - 1.0	-	V_{cc}	V
$Flash_{enpb}$	Flash Endurance (Per Block)	50,000	-	-	E/W Cycles per Block
$Flash_{ent}$	Flash Endurance (Total)[2]	1,800,000			E/W Cycles
$Flash_{dr}$	Flash Data Retention (After Cycling)	10	-	-	Years

1. Driving internal pull-down resistor.
2. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

   The CY8C25xxx/26xxx family of PSoC devices uses an adaptive algorithm to enhance endurance over the industrial temperature range (-40°C to +85°C ambient). Any temperature range within a 50°C span between 0°C and 85°C is considered constant with respect to endurance enhancements. For instance, if room temperature (25°C) is the nominal operating temperature, then the range from 0°C to 50°C can be approximated by the constant value 25 and a temperature sensor is not needed.

   For the full industrial range, the user must employ a temperature sensor User Module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypressmicro.com under Support or Active Design Support for more information.

13.3 AC Characteristics

Table 116: AC Operating Specifications

Symbol	AC Operating Specifications	Minimum	Typical	Maximum	Unit
F_{CPU1}	CPU Frequency (5 V Nominal)[1,2,3]	91.35	2,400	2,460	kHz
F_{CPU2}	CPU Frequency (3.3V Nominal)[4,3]	91.35	1,200	1,230	kHz
F_{48M}	Digital PSoC Block Frequency		48	49.2[1,5]	MHz
F_{24M}	Digital PSoC Block Frequency		24	24.6[2,4]	MHz
F_{GPIO}	GPIO Operating Frequency		12		MHz
F_{IMO}	Internal Main Oscillator Frequency (0^oC to $+85^oC$)	23.4	24	24.6	MHz
F_{IMOC}	Internal Main Oscillator Frequency Cold (-40^oC to 0^oC)	22.44	24	24.6	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency (Non Sleep)	15[6]	32	50	kHz
F_{32K2}	Internal Low Speed Oscillator Frequency (Sleep or Halt)	15[7]	32	64	kHz
F_{32K3}	External Crystal Oscillator	-	32.768[8]	-	kHz
F_{pll}	PLL Frequency	-	23.986[9]	-	MHz
T_f	Output Fall Time	2[10]	-	12	ns
T_r	Output Rise Time	3[10]	-	18	ns
$T_{pllslew}$	PLL Lock Time	0.5	-	10	ms
SV_{dd}	V_{dd} Rise Rate at Power Up	80[11]	-	-	mV/ms
T_{os}	External Crystal Oscillator Startup to 1%	-	100	500[12]	ms
T_{osacc}	External Crystal Oscillator Startup to 100 ppm	-	150	600[13]	ms
T_{xrst}	External Reset Pulse Width	10	-	-	µs

1. $4.75V < V_{cc} < 5.25V$.
2. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{cc} range.
3. 0^oC to $+85^oC$.
4. $3.0V < V_{cc} < 3.6V$.
5. See Application Note AN2012 ”Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on maximum frequency for User Modules.
6. Limits are valid only when *not* in sleep mode.
7. Limits are valid only when in sleep mode.
8. Accuracy is capacitor and crystal dependent.
9. Is a multiple (x732) of crystal frequency.
10. Load capacitance = 50 pF.
11. To minimum allowable voltage for desired frequency.
12. The crystal oscillator frequency is guaranteed to be within 1% of its final value by the end of the 1s startup timer period. Timer period may be as short as 640 ms for the case where F_{32K1} is 50 kHz. Correct operation assumes a properly loaded 1uW maximum drive level 32.768 kHz crystal.
13. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. $3.0V <= V_{cc} <= 5.5V$, $-40\ ^oC <= T_A <= 85\ ^oC$.

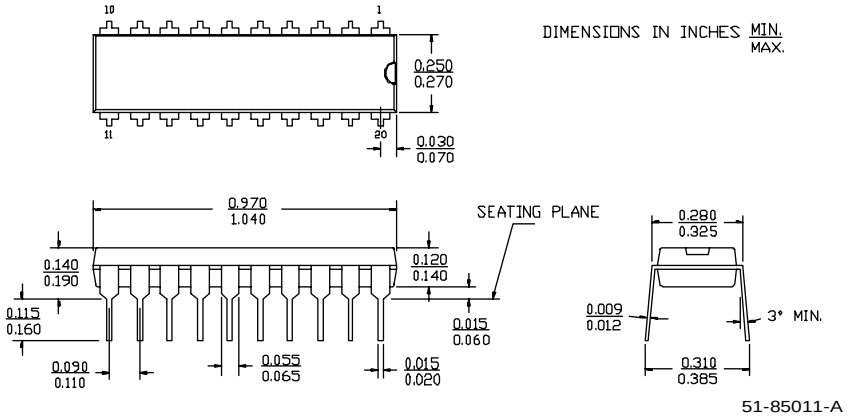

Figure 41: 20-Lead (300-Mil) Molded DIP P5

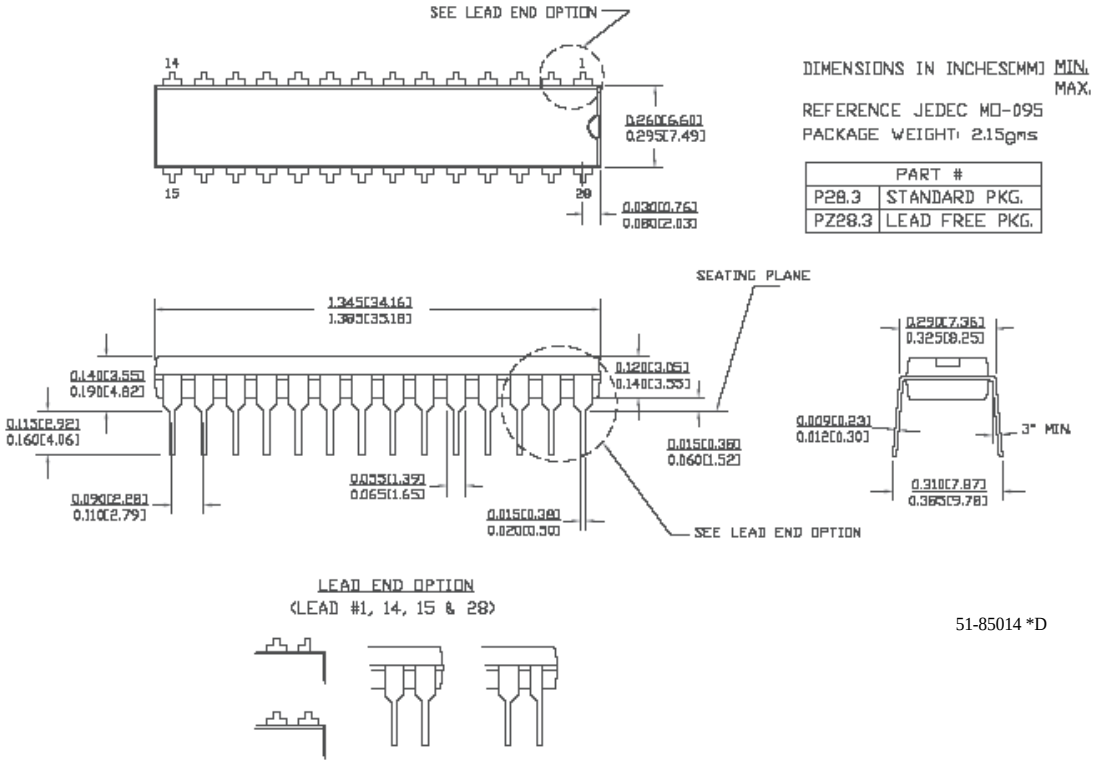

Figure 42: 28-Lead (300-Mil) Molded DIP P21

15.0 Ordering Guide

Table 123: Ordering Guide (Leaded)[1]

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVI	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVI	16	256	Yes	Ind. -40C to +85C
48 Pin (600 Mil) Molded DIP	CY8C26643-24PI[2]	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AI	16	256	Yes	Ind. -40C to +85C

1. Orders for leaded devices will not be accepted after July 2005.
2. 48-PDIP package not offered Pb-Free.

Table 124: Ordering Guide (Pb-Free Denoted with an “X” in Ordering Code)

Type	Ordering Code	Flash (KBytes)	RAM (Bytes)	SMP	Temperature Range
8 Pin (300 Mil) Molded DIP	CY8C25122-24PXI	4	256	No	Ind. -40C to +85C
20 Pin (300 Mil) Molded DIP	CY8C26233-24PXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC	CY8C26233-24SXI	8	256	Yes	Ind. -40C to +85C
20 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26233-24SXIT	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP	CY8C26233-24PVXI	8	256	Yes	Ind. -40C to +85C
20 Pin (210 Mil) SSOP Tape and Reel	CY8C26233-24PVXIT	8	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded DIP	CY8C26443-24PXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC	CY8C26443-24SXI	16	256	Yes	Ind. -40C to +85C
28 Pin (300 Mil) Molded SOIC Tape and Reel	CY8C26443-24SXIT	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP	CY8C26443-24PVXI	16	256	Yes	Ind. -40C to +85C
28 Pin (210 Mil) SSOP Tape and Reel	CY8C26443-24PVXIT	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP	CY8C26643-24PVXI	16	256	Yes	Ind. -40C to +85C
48 Pin (300 Mil) SSOP Tape and Reel	CY8C26643-24PVXIT	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack	CY8C26643-24AXI	16	256	Yes	Ind. -40C to +85C
44 Pin Thin Plastic Quad Flatpack Tape and Reel	CY8C26643-24AXIT	16	256	Yes	Ind. -40C to +85C

16.0 Document Revision History

Table 125: Document Revision History

Document Title: CY8C25122, CY8C26233, CY8C26443, CY8C26643 Device Data Sheet for Silicon Revision D **Document Number**: 38-12010				
Revision	**ECN #**	**Issue Date**	**Origin of Change**	**Description of Change**
**	116628	6/17/2002	CMS Cypress Management. New Silicon Revision.	New document to CY Document Control (Revision **). Revision 3.20 for CMS customers.
*A	127231	5/22/2003	HMT.	Implementing new error tracking and document release procedure. Changes in red for Document #: 38-12010 CY Rev. *A CMS Rev. 3.20a. Changes include: --Bit 6 of the VLT_CR register is RW. Should be changed from "RW" to "--." --Analog Output Buffer Control Register ABF_CR Read/Write in Bank 1 table was corrected to Write Only. --Rewrite of section 10.4 Analog Reference Control . --AC Char. Spec. table changed .080 to 80 in "Vdd Rise Rate at Power Up." On features pg. 2, changed "Up to 10 bit DAC" to "Up to 8 bit DAC." --Adding temp. spec. for 24 MHz at beginning of AC/DC Characteristics section and Absolute Maximum Value table. --In AC Operating Spec. table fixed footnote for Output Rise Time minimum. --In AC Operating Spec. table fixed value for External Reset Pulse Width. --Changed uS to us units in tables. --New intro. --In the Analog Reference Control Register, ARF_CR, state 100 for bits 2:0 should be described as "All Analog Off.“ --Rework title pgs.
*B	127231	5/22/2003	HMT.	Several updates including Thermal Impedances table, 8 PDIP diagram and company address. OSC_CR0 register name.
*C	362598	See ECN	HMT.	Add Pb-Free table. Add “Not Recommended for New Designs“ banner. Update package revisions. Fix register typo’s.
Distribution: External/Public **Posting**: None				