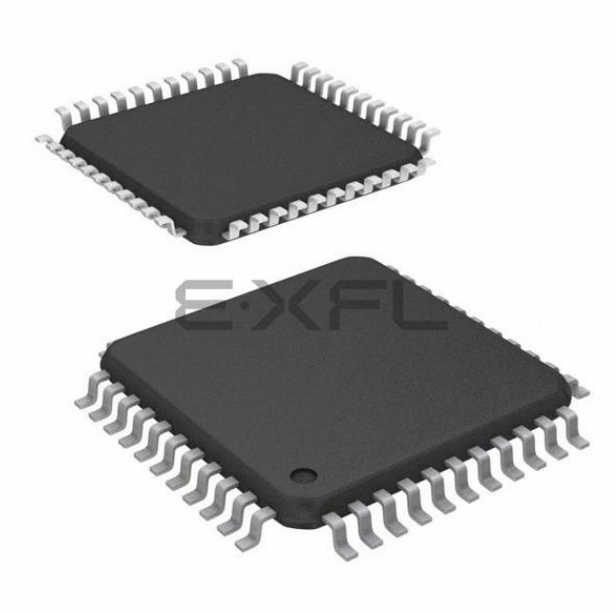

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
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1.2 Pin-out Descriptions

Table 2: Pin-out 8 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P1[1]	I/O	3	Port 1[1] / XtalIn / SCLK
Vss	Power	4	Ground
P1[0]	I/O	5	Port 1[0] / XtalOut / SDATA
P0[2]	I/O	6	Port 0[2] (Analog Input/Output)
P0[4]	I/O	7	Port 0[4] (Analog Input/Output)
Vcc	Power	8	Supply Voltage

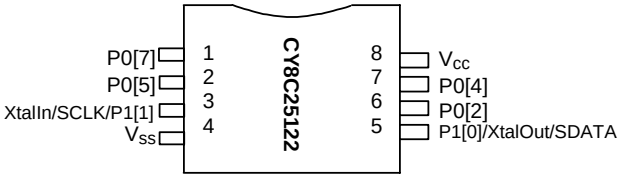

Figure 2: CY8C25122

Table 3: Pin-out 20 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
SMP	O	5	Switch Mode Pump
P1[7]	I/O	6	Port 1[7]
P1[5]	I/O	7	Port 1[5]
P1[3]	I/O	8	Port 1[3]
P1[1]	I/O	9	Port 1[1] / XtalIn / SCLK
Vss	Power	10	Ground
P1[0]	I/O	11	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	12	Port 1[2]
P1[4]	I/O	13	Port 1[4]
P1[6]	I/O	14	Port 1[6]
XRES	I	15	External Reset
P0[0]	I/O	16	Port 0[0] (Analog Input)
P0[2]	I/O	17	Port 0[2] (Analog Input/Output)
P0[4]	I/O	18	Port 0[4] (Analog Input/Output)
P0[6]	I/O	19	Port 0[6] (Analog Input)
Vcc	Power	20	Supply Voltage

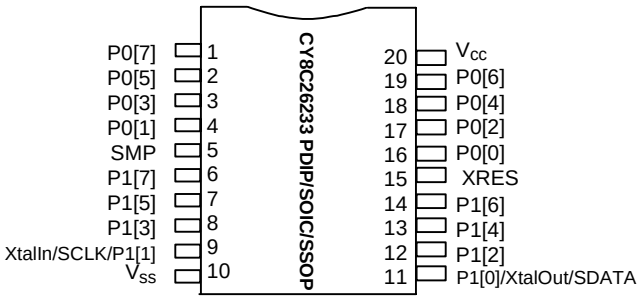

Figure 3: CY8C26233

2.0 CPU Architecture

2.1 Introduction

This family of microcontrollers is based on a high performance, 8-bit, Harvard architecture microprocessor. Five registers control the primary operation of the CPU core. These registers are affected by various instructions, but are not directly accessible through the register space by the user. For more details on addressing with the register space, see section 4.0.

Table 7: CPU Registers and Mnemonics

Register	Mnemonic
Flags	CPU_F
Program Counter	CPU_PC
Accumulator	CPU_A
Stack Pointer	CPU_SP
Index	CPU_X

The 16 bit Program Counter Register (CPU_PC) allows for direct addressing of the full 16 Kbytes of program memory space available in the largest members of this family. This forms one contiguous program space, and no paging is required.

The Accumulator Register (CPU_A) is the general-purpose register that holds the results of instructions that specify any of the source addressing modes.

The Index Register (CPU_X) holds an offset value that is used in the indexed addressing modes. Typically, this is used to address a block of data within the data memory space.

The Stack Pointer Register (CPU_SP) holds the address of the current top-of-stack in the data memory space. It is affected by the PUSH, POP, LCALL, CALL, RETI, and RET instructions, which manage the software stack. It can also be affected by the SWAP and ADD instructions.

The Flag Register (CPU_F) has three status bits: Zero Flag bit [1]; Carry Flag bit [2]; Supervisory State bit [3]. The Global Interrupt Enable bit [0] is used to globally enable or disable interrupts. An extended I/O space address, bit [4], is used to determine which bank of the register space is in use. The user cannot manipulate the Supervisory State status bit [3]. The flags are affected by arithmetic, logic, and shift operations. The manner in which each flag is changed is dependent upon the instruction being executed (i.e., AND, OR, XOR... See Table 23 on page 25).

7.0 Clocking

7.1 Oscillator Options

7.1.1 Internal Main Oscillator

The internal main oscillator outputs two frequencies, 48 MHz and 24 MHz. In the absence of a high-precision input source from the external oscillator, the accuracy of this circuit is +/- 2.5% (between 0°C and +85°C). No external components are required to achieve this level of accuracy. The Internal Main Oscillator Trim Register (IMO_TR) is used to calibrate this oscillator into specified tolerance. Factory-programmed trim values are available for 5.0V and 3.3V operation. The 5.0V value is loaded in the IMO_TR register upon reset. This register must be adjusted when the operating voltage is outside the range for which factory calibration was set. The factory-programmed trim value is selected using the Table Read Supervisor Call, and is documented in 11.8.

There is an option to phase lock this oscillator to the External Crystal Oscillator. The choice of crystal and its inherent accuracy will determine the overall accuracy of the oscillator. The External Crystal Oscillator must be stable prior to locking the frequency of the Internal Main Oscillator to this reference source.

Table 35: Internal Main Oscillator Trim Register

Bit #	7	6	5	4	3	2	1	0
POR	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]	FS[1]
Read/Write	W	W	W	W	W	W	W	W
Bit Name	IMO Trim [7]	IMO Trim [6]	IMO Trim [5]	IMO Trim [4]	IMO Trim [3]	IMO Trim [2]	IMO Trim [1]	IMO Trim [0]
Bit [7:0]: **IMO Trim [7:0]** Data value stored will alter the trimmed frequency of the Internal Main Oscillator. A larger value in this register will increase the speed of the Internal Main Oscillator								

1. FS = Factory set trim value

Internal Main Oscillator Trim Register (IMO_TR, Address = Bank 1, E8h)

7.1.2 Internal Low Speed Oscillator

An internal low speed oscillator of nominally 32 kHz is available to generate sleep wake-up interrupts and Watchdog resets if the user does not want to attach a 32.768 kHz watch crystal. This oscillator can also be used as a clocking source for the digital PSoC blocks.

The oscillator operates in two different modes. A trim value is written to the Internal Low Speed Oscillator Trim Register (ILO_TR), shown below, upon reset. See section 13.0 for accuracy information. When the IC is put into sleep mode this oscillator drops into an ultra low current state and the accuracy is reduced.

This register sets the adjustment for the Internal Low Speed Oscillator. The value placed in this register is based on factory testing. It is recommended that the user not alter this value.

Table 37: External Crystal Oscillator Trim Register

Bit #	7	6	5	4	3	2	1	0
POR	FS[1]	FS[1]	0	0	FS[1]	FS[1]	FS[1]	FS[1]
Read/Write	W	W	--	--	W	W	W	W
Bit Name	PSSDC [1]	PSSDC [0]	Reserved	Reserved	Amp [1]	Amp [0]	Bias [1]	Bias [0]

Bit [7:6]: **PSSDC [1:0]** Power System Sleep Duty Cycle. (Not recommended for customer alteration)
0 0 = 1/128
0 1 = 1/512
1 0 = 1/32
1 1 = 1/8

Bit 5: **Reserved**
Bit 4: **Reserved**

Bit [3:2]: **Amp [1:0]** Sets the amplitude of the adjustment. (Not recommended for customer alteration)

Bit [1:0]: **Bias [1:0]** Sets the bias of the adjustment. (Not recommended for customer alteration)

1. FS = Factory set trim value

External Crystal Oscillator Trim Register (ECO_TR, Address = Bank 1, EBh)

7.1.4 External Crystal Oscillator Component Connections and Selections

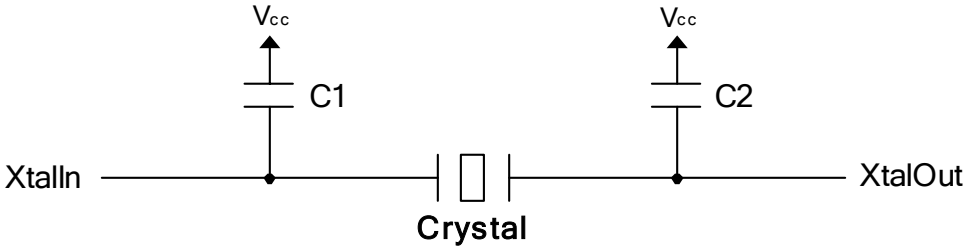

Figure 8: External Crystal Oscillator Connections

- Crystal – 32.768 kHz watch crystal such as EPSON C-002RX (12.5 pF load capacitance)
- Capacitors – C1, C2
  Use NPO-type ceramic caps
  C1 = C2 = 25 pF - (Package Cap) - (Board Parasitic Cap)

Note: Use this equation if you do not employ PLL mode. If you do employ PLL with the External Crystal Oscillator, see Application Note AN2027 under **Support** at http://www.cypressmicro.com for equation and details. An error of 1 pF in C1 and C2 gives about 3 ppm error in frequency.

Table 38: Typical Package Capacitances

Package	Package Capacitance
8 PDIP	0.9 pF
20 PDIP	2 pF
20 SOIC	1 pF
20 SSOP	0.5 pF
28 PDIP	2 pF
28 SOIC	1 pF
28 SSOP	0.5 pF
44 TQFP	0.5 pF
48 PDIP	5 pF
48 SSOP	0.6 pF

8.2 Interrupt Control Architecture

The interrupt controller contains a separate flip-flop for each interrupt. When an interrupt is generated, it is registered as a pending interrupt. It will stay pending until it is serviced, a reset occurs, or there is a write to the INT_VC Register. A pending interrupt will only generate an interrupt request when enabled by the appropriate mask bit in the Digital PSoC Block Interrupt Mask Register (INT_MSK1) or General Interrupt Mask Register (INT_MSK0), and the Global IE bit in the CPU_F register is set.

Additionally, for GPIO Interrupts, the appropriate enable and interrupt-type bits for each I/O pin must be set (see section 6.0, Table 29 on page 31, Table 33 on page 33, and Table 34 on page 34). For Analog Column Interrupts, the interrupt source must be set (see section 10.10 and Table 77 on page 101).

During the servicing of any interrupt, the MSB and LSB of Program Counter and Flag registers (CPU_PC and CPU_F) are stored onto the program stack by an automatic `CALL` instruction (13 cycles) generated during the interrupt acknowledge process. The user firmware may preserve and restore processor state during an interrupt using the `PUSH` and `POP` instructions. The memory oriented CPU architecture requires minimal state saving during interrupts, providing very fast interrupt context switching. The Program Counter and Flag registers (CPU_PC and CPU_F) are restored when the `RETI` instruction is executed. If two or more interrupts are pending at the same time, the higher priority interrupt (lower priority number) will be serviced first.

After a copy of the Flag Register is stored on the stack, the Flag Register is automatically cleared. This disables all interrupts, since the Global IE flag bit is now cleared. Executing a `RETI` instruction restores the Flag register, and re-enables the Global Interrupt bit.

Nested interrupts can be accomplished by re-enabling interrupts inside an interrupt service routine. To do this, set the IE bit in the Flag Register. The user must store sufficient information to maintain machine state if this is done.

Each digital PSoC block has its own unique Interrupt Vector and Interrupt Enable bit. There are also individual interrupt vectors for each of the Analog columns, Supply Voltage Monitor, Sleep Timer and General Purpose I/Os.

8.3 Interrupt Vectors

Table 43: Interrupt Vector Table

Address	Interrupt Priority Number	Description
0x0004	1	Supply Monitor Interrupt Vector
0x0008	2	DBA00 PSoC Block Interrupt Vector
0x000C	3	DBA01 PSoC Block Interrupt Vector
0x0010	4	DBA02 PSoC Block Interrupt Vector
0x0014	5	DBA03 PSoC Block Interrupt Vector
0x0018	6	DCA04 PSoC Block Interrupt Vector
0x001C	7	DCA05 PSoC Block Interrupt Vector
0x0020	8	DCA06 PSoC Block Interrupt Vector
0x0024	9	DCA07 PSoC Block Interrupt Vector
0x0028	10	Acolumn 0 Interrupt Vector
0x002C	11	Acolumn 1 Interrupt Vector
0x0030	12	Acolumn 2 Interrupt Vector
0x0034	13	Acolumn 3 Interrupt Vector
0x0038	14	GPIO Interrupt Vector
0x003C	15	Sleep Timer Interrupt Vector
0x0040		On-Chip Program Memory Starts

The interrupt process vectors the Program Counter to the appropriate address in the Interrupt Vector Table. Typically, these addresses contain `JMP` instructions to the start of the interrupt handling routine for the interrupt.

Table 45: Digital PSoC Block Interrupt Mask Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	DCA07	DCA06	DCA05	DCA04	DBA03	DBA02	DBA01	DBA00

Bit 7: **DCA07 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 6: **DCA06 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 5: **DCA05 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 4: **DCA04 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 3: **DBA03 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 2: **DBA02 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 1: **DBA01 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 0: **DBA00 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Digital PSoC Block Interrupt Mask Register (INT_MSK1, Address = Bank 0, E1h)

8.5 Interrupt Vector Register

Table 46: Interrupt Vector Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

Bit [7:0]: **Data [7:0]**
8-bit data value holds the interrupt vector for the highest priority pending interrupt. Writing to this register will clear all pending interrupts

Interrupt Vector Register (INT_VC, Address = Bank 0, E2h)

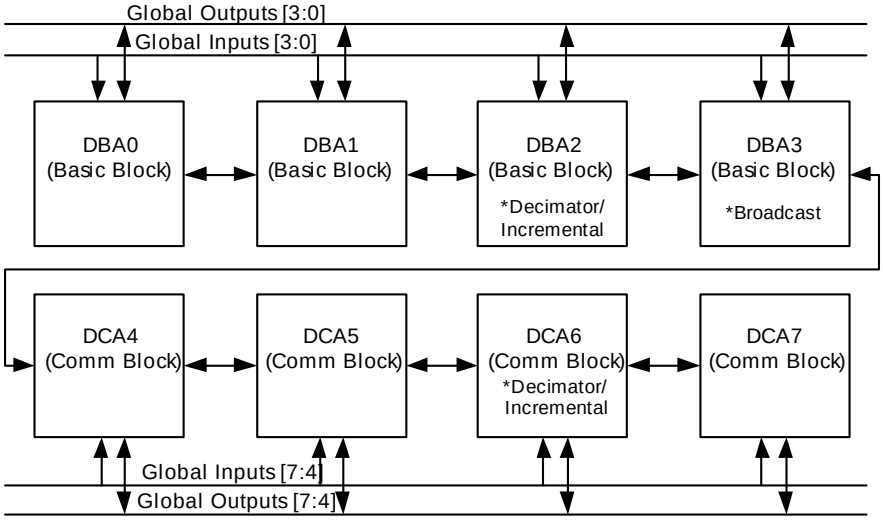

Figure 12: Digital Basic and Digital Communications PSoC Blocks

*Three of the digital blocks have special functions. DBA3 is a Broadcast block, with output directly available to all digital blocks as a clock or data input. Blocks DBA2 and DCA6 have selectable connections to support Delta Sigma and Incremental A/D converters.

9.2 Digital PSoC Block Bank 1 Registers

9.2.1 Digital Basic Type A / Communications Type A Block xx Function Register

The Digital Basic Type A/ Communications Type A Block xx Function Register (DBA00FN-DCA07FN) consists of 3 bits [2:0] to select the block function, 2 bits [4:3] to select mode of operation, and 1 bit [5] to indicate the last block in a group of chained blocks.

directly into Data Register 0 (The block must be disabled when writing this value). Data Register 1 specifies the polynomial and width of the numbers in the sequence (see “Specifying the Polynomial”, below). Once the input bit stream is complete, the result may be read by first reading Data Register 0, which returns 0, then reading Data Register 2, which returns the actual result.

9.5.5.3 Inputs

The clock input determines the rate at which the input sequence is processed. The data input selects the data stream to process. It is assumed that the data is valid on the positive edge of the clock input. The multiplexer for selecting these inputs is controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.5.4 Outputs

Like the PRS, the CRC function drives the output serial data stream with the most significant bit of CRC processing synchronous with the input clock. Normally the CRC output is not used. The output may be driven on the Global Output bus or to the subsequent digital PSoC block. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.5.5 Interrupts

The CRC function provides an interrupt based on the Compare signal between Data Register 0 and Data Register 2.

9.5.5.6 Specifying the Polynomial

Computation of an N-bit result is generally specified by a polynomial with N+1 terms, the last of which is the X^0 term, where X^0=1. For example, the widely used CRC-CCIT 16-bit polynomial is $X^{16}+X^{12}+X^5+1$. The PSoC block CRC function assumes the presence of the X^0 term so that the polynomial for an N-bit result can be expressed by an N-bit rather than N+1 bit specification. To obtain the PSoC block register specification, write an N+1 bit binary number corresponding to the full polynomial, with 1’s for each term present. The CRC-CCIT polynomial would be 10001000000100001b. Simply drop the right-most bit (the X^0 term) to obtain the register specification for the PSoC block. To implement the CRC-CCIT example, two PSoC blocks must be chained together. Data Register 1 in the high-order PSoC block would take the value 10001000b (88h) and the corresponding register in the low-order PSoC block would take 00010000b (10h).

9.5.5.7 Usage Notes

1. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 2 (Seed) is loaded directly into Data Register 0 (LFSR) to initialize or reset the seed value. All outputs are low and the block interrupt is held low.

2. Reading the CRC value

   After the data stream has been processed by the LFSR, the residue is the CRC value. The current LFSR value can only be read when the block is disabled by setting the Control Register bit 0 to low. Each byte of the current LFSR value (in the case of a multi-byte block) must be read individually. The Data Register 0 byte (LFSR) must be read, which returns 0, then the Data Register 2 byte, which returns the actual value.

9.5.6 Universal Asynchronous Receiver

9.5.6.1 Summary

The Universal Asynchronous Receiver implements the input half of a basic 8-bit UART. Start and Stop bits are recognized and stripped. Parity type and parity validation are configurable features. This function requires a Digital Communications Type PSoC block and cannot be chained for longer data words.

9.5.6.2 Registers

The function shifts incoming data into Data Register 0. Once complete, the byte is transferred to Data Register 2 from which it may be read. Data Register 2 acts as a 1 byte receive buffer. Data Register 1 is not used by this function. Control Register 0 (DCA04CR0-DCA07CR0) enables the function, provides the means to configure parity checking, and a full set of status indications. See the register definition for full details.

divided into distinct bit fields. Some bit fields set the PSoC block's resistor ratios or capacitor values. Others configure switches and multiplexers that form connections between internal block nodes. Additionally, a block may be connected via local interconnection resources to neighboring analog PSoC blocks, reference voltage sources, input multiplexers and output busses. Specific advantages and applications of each type are treated separately below.

10.6.1 Local Interconnect

Analog continuous-time PSoC blocks occupy the top row, (row 0) of the analog array. Designated ACA for analog continuous-time subtype "A," each connects to its neighbors by means of three multiplexers. (Note that unlike the switched capacitor blocks, the continuous time blocks in the current family of parts only have one subtype.) The three are the non-inverting input multiplexer, "PMux," the inverting input multiplexer, "NMux," and the "RBotMux" which controls the node at the bottom of the resistor string. The bit fields, which control these multiplexers, are named PMux, NMux, and RBotMux, respectively. The following diagrams show how each multiplexer connects its ACA block connect to its neighbors. Each arrow points from an input source, either a PSoC block, bus or reference voltage to the block where it is used. Each arrow is labeled with the value to which the bit-field must be set to select that input source.

10.6.1.1 NMux

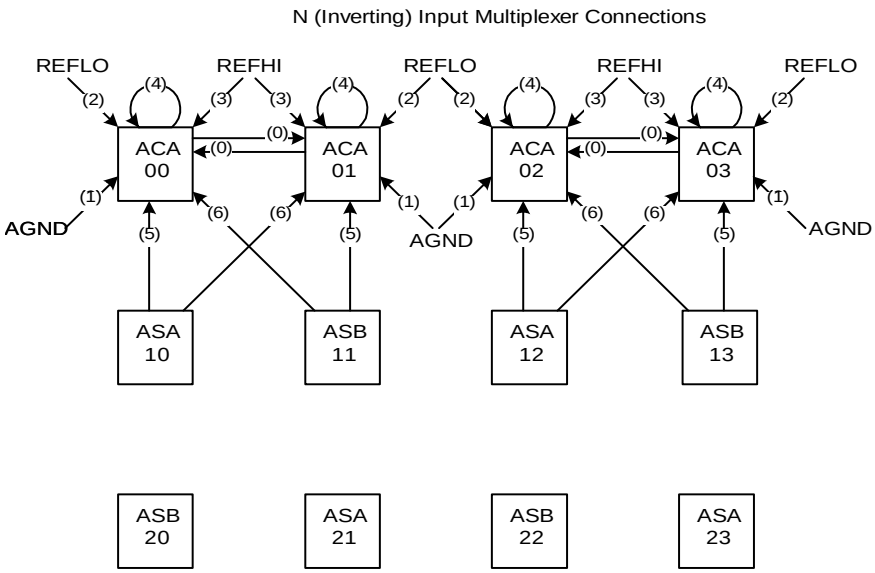

Figure 18: NMux Connections

10.7.2.2 Analog Continuous Time Block xx Control 1 Register

The PMux bits control the multiplexing of inputs to the non-inverting input of the op-amp. There are physically only 7 inputs.

The 8th code (111) will leave the input floating. This is not desirable, and should be avoided.

The NMux bits control the multiplexing of inputs to the inverting input of the op-amp. There are physically only 7 inputs.

CompBus controls a tri-state buffer that drives the comparator logic. If no PSoC block in the analog column is driving the comparator bus, it will be driven low externally to the blocks.

AnalogBus controls the analog output bus. A CMOS switch connects the op-amp output to the analog bus.

Table 67: Analog Continuous Time Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	NMux2	NMux1	NMux0	PMux2	PMux1	PMux0

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable analog bus driven by this block
1 = Enable analog bus driven by this block
Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable comparator bus driven by this block
1 = Enable comparator bus driven by this block

Bit [5:3]: **NMux [2:0]** Encoding for negative input select

	ACA00	ACA01	ACA02	ACA03
0 0 0 =	ACA01	ACA00	ACA03	ACA02
0 0 1 =	AGND	AGND	AGND	AGND
0 1 0 =	REFLO	REFLO	REFLO	REFLO
0 1 1 =	REFHI	REFHI	REFHI	REFHI
1 0 0[1] =	ACA00	ACA01	ACA02	ACA03
1 0 1 =	ASA10	ASB11	ASA12	ASB13
1 1 0 =	ASB11	ASA10	ASB13	ASA12
1 1 1 =	Reserved	Reserved	Reserved	Reserved

Bit [2:0]: **PMux [2:0]** Encoding for positive input select

	ACA00	ACA01	*ACA02*	ACA03
0 0 0 =	REFLO	ACA02	ACA01	REFLO
0 0 1 =	Port Inputs	Port Inputs	Port Inputs	Port Inputs
0 1 0 =	ACA01	ACA00	ACA03	ACA02
0 1 1 =	AGND	AGND	AGND	AGND
1 0 0 =	ASA10	ASB11	ASA12	ASB13
1 0 1 =	ASB11	ASA10	ASB13	ASA12
1 1 0 =	ABUS0	ABUS1	ABUS2	ABUS3
1 1 1 =	Reserved	Reserved	Reserved	Reserved

1. This in fact is the feedback input of the MUX.

Analog Continuous Time Block 00 Control 1 Register (ACA00CR1, Address = Bank 0/1, 72h)
Analog Continuous Time Block 01 Control 1 Register (ACA01CR1, Address = Bank 0/1, 76h)
Analog Continuous Time Block 02 Control 1 Register (ACA02CR1, Address = Bank 0/1, 7Ah)
Analog Continuous Time Block 03 Control 1 Register (ACA03CR1, Address = Bank 0/1, 7Eh)

10.8 Analog Switch Cap Type A PSoC Blocks

10.8.1 Introduction

The Analog Switch Cap Type A PSoC blocks are built around an operational amplifier. There are several analog muxes that are controlled by register-bit settings in the control registers that determine the signal topology inside the block. There are also four arrays of unit value capacitors that are located in the feedback path for the op-amp, and are switched by two phase clocks, PHI1 and PHI2. These four capacitor arrays are labeled A Cap Array, B Cap Array, C Cap Array, and F Cap Array. There is also an analog comparator connected to the output OUT, which converts analog comparisons into digital signals.

There are three discrete outputs from this block. These outputs are:

1. The analog output bus (ABUS), which is an analog bus resource that is shared by all of the analog blocks in the analog column for that block.

2. The comparator bus (CBUS), which is a digital bus that is a resource that is shared by all of the analog blocks in a column for that block.

3. The output bus (OUT), which is an analog bus resource that is shared by all of the analog blocks in a column and connects to one of the analog output buffers, to send a signal externally to the device.

SC Integrator Block A supports Delta-Sigma, Successive Approximation and Incremental A/D Conversion, Capacitor DACs, and SC filters. It has three input arrays of binarily-weighted switched capacitors, allowing user programmability of the capacitor weights. This provides summing capability of two (CDAC) scaled inputs, and a non-switched capacitor input. Since the input of SC Block A has this additional switched capacitor, it is configured for the input stage of such a switched capacitor biquad filter. When followed by an SC Block B Integrator, this combination of blocks can be used to provide a full Switched Capacitor Biquad.

10.8.2 Local Interconnect

10.8.2.1 AMux

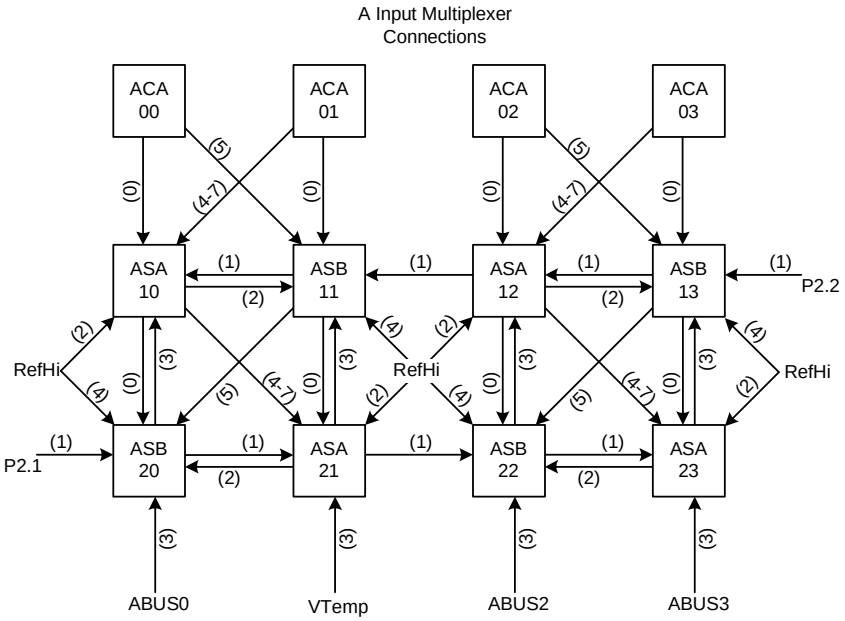

Figure 23: AMux Connections

10.8.2.2 CMux

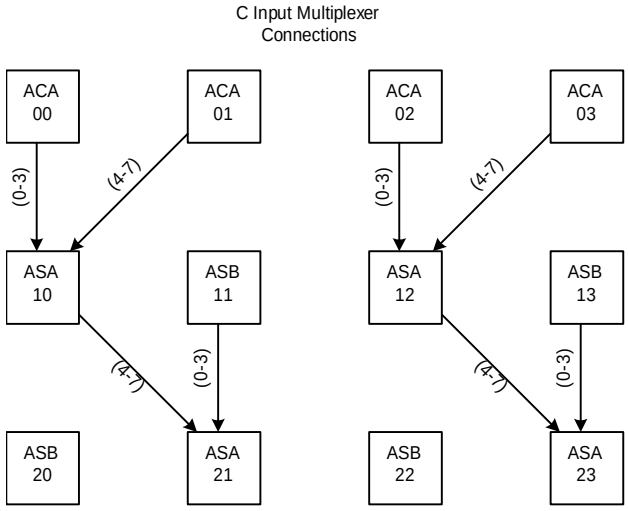

Figure 24: CMux Connections

Table 69: Analog Switch Cap Type A Block xx Control 0 Register, continued

Bit 7: **FCap** F Capacitor value selection bit
0 = 16 capacitor units
1 = 32 capacitor units

Bit 6: **ClockPhase** Clock phase select, will invert clocks internal to the blocks. During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2)

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Select Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s

0 = Internal PHI1 = External PHI1
1 = Internal PHI1 = External PHI2

This bit also affects the latching of the comparator output (CBUS). Both clock phases, PHI1 and PHI2, are involved in the output latching mechanism. The capture of the next value to be output from the latch (capture point event) happens during the falling edge of one clock phase, and the rising edge of the other clock phase will cause the value to come out (output point event). This bit determines which clock phase triggers the capture point event, and the other clock will trigger the output point event. The value output to the comparator bus will remain stable between output point events.

0 = Capture Point Event triggered by Falling PHI2, Output Point Event triggered by Rising PHI1
1 = Capture Point Event triggered by Falling PHI1, Output Point Event triggered by Rising PHI2

Bit 5: **ASign**
0 = Input sampled on Internal PHI1, Reference Input sampled on internal PHI2
1 = Input sampled on Internal PHI2, Reference Input sampled on internal PHI1

Bit [4:0]: **ACap [4:0]** Binary encoding for 32 possible capacitor sizes for A Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type A Block 10 Control 0 Register (ASA10CR0, Address = Bank 0/1, 80h)
Analog Switch Cap Type A Block 12 Control 0 Register (ASA12CR0, Address = Bank 0/1, 88h)
Analog Switch Cap Type A Block 21 Control 0 Register (ASA21CR0, Address = Bank 0/1, 94h)
Analog Switch Cap Type A Block 23 Control 0 Register (ASA23CR0, Address = Bank 0/1, 9Ch)

10.8.3.4 Analog Switch Cap Type A Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASA10CR2, ASA12CR2, ASA21CR2, ASA23CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BMuxSCA controls the muxing to the input of the B capacitor branch.

Power – encoding for selecting 1 of 4 power levels. The block always powers up in the off state.

Table 72: Analog Switch Cap Type A Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BMuxSCA[1]	BMuxSCA[0]	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
1 = If the FSW1 bit is set to 1, the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit [3:2] BMuxSCA [1:0] Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block.)

ASA10	ASA21	ASA12	ASA23
0 0 = ACA00	ASB11	ACA02	ASB13
0 1 = ASB11	ASB20	ASB13	ASB22
1 0 = P2.3	ASB22	ASB11	P2.0
1 1 = ASB20	T_{ref}GND	ASB22	ABUS3

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type A Block 10 Control 3 Register (ASA10CR3, Address = Bank 0/1, 83h)
Analog Switch Cap Type A Block 12 Control 3 Register (ASA12CR3, Address = Bank 0/1, 8Bh)
Analog Switch Cap Type A Block 21 Control 3 Register (ASA21CR3, Address = Bank 0/1, 97h)
Analog Switch Cap Type A Block 23 Control 3 Register (ASA23CR3, Address = Bank 0/1, 9Fh)

Table 73: Analog Switch Cap Type B Block xx Control 0 Register, continued

Bit 7: **FCap** F Capacitor value selection bit
0 = 16 capacitor units
1 = 32 capacitor units

Bit 6: **ClockPhase** Clock phase select, will invert clocks internal to the blocks. During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2)

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Select Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s

0 = Internal PHI1 = External PHI1
1 = Internal PHI1 = External PHI2

This bit also affects the latching of the comparator output (CBUS). Both clock phases, PHI1 and PHI2, are involved in the output latching mechanism. The capture of the next value to be output from the latch (capture point event) happens during the falling edge of one clock phase, and the rising edge of the other clock phase will cause the value to come out (output point event). This bit determines which clock phase triggers the capture point event, and the other clock will trigger the output point event. The value output to the comparator bus will remain stable between output point events.

0 = Capture Point Event triggered by Falling PHI2, Output Point Event triggered by Rising PHI1
1 = Capture Point Event triggered by Falling PHI1, Output Point Event triggered by Rising PHI2

Bit 5: **ASign**
0 = Input sampled on Internal PHI1, Reference Input sampled on internal PHI2
1 = Input sampled on Internal PHI2, Reference Input sampled on internal PHI1

Bit [4:0]: **ACap [4:0]** Binary encoding for 32 possible capacitor sizes for A Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 0 Register (ASB11CR0, Address = Bank 0/1, 84h)
Analog Switch Cap Type B Block 13 Control 0 Register (ASB13CR0, Address = Bank 0/1, 8Ch)
Analog Switch Cap Type B Block 20 Control 0 Register (ASB20CR0, Address = Bank 0/1, 90h)
Analog Switch Cap Type B Block 22 Control 0 Register (ASB22CR0, Address = Bank 0/1, 98h)

Table 75: Analog Switch Cap Type B Block xx Control 2 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AnalogBus	CompBus	AutoZero	CCap[4]	CCap[3]	CCap[2]	CCap[1]	CCap[0]

Bit 7: **AnalogBus** Enable output to the analog bus
0 = Disable output to analog column bus
1 = Enable output to analog column bus
(The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASB11CR0, ASB13CR0, ASB20CR0, ASB22CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the ClockPhase bit selects the signal that is output to the analog column bus. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block output continuously drives the analog column bus)

Bit 6: **CompBus** Enable output to the comparator bus
0 = Disable output to comparator bus
1 = Enable output to comparator bus

Bit 5: **AutoZero** Bit for controlling gated switches
0 = Shorting switch is not active. Input cap branches shorted to op-amp input
1 = Shorting switch is enabled during internal PHI1. Input cap branches shorted to analog ground during internal PHI1 and to op-amp input during internal PHI2.

Bit [4:0]: **CCap [4:0]** Binary encoding for 32 possible capacitor sizes for C Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 2 Register (ASB11CR2, Address = Bank 0/1, 86h)
Analog Switch Cap Type B Block 13 Control 2 Register (ASB13CR2, Address = Bank 0/1, 8Eh)
Analog Switch Cap Type B Block 20 Control 2 Register (ASB20CR2, Address = Bank 0/1, 92h)
Analog Switch Cap Type B Block 22 Control 2 Register (ASB22CR2, Address = Bank 0/1, 9Ah)

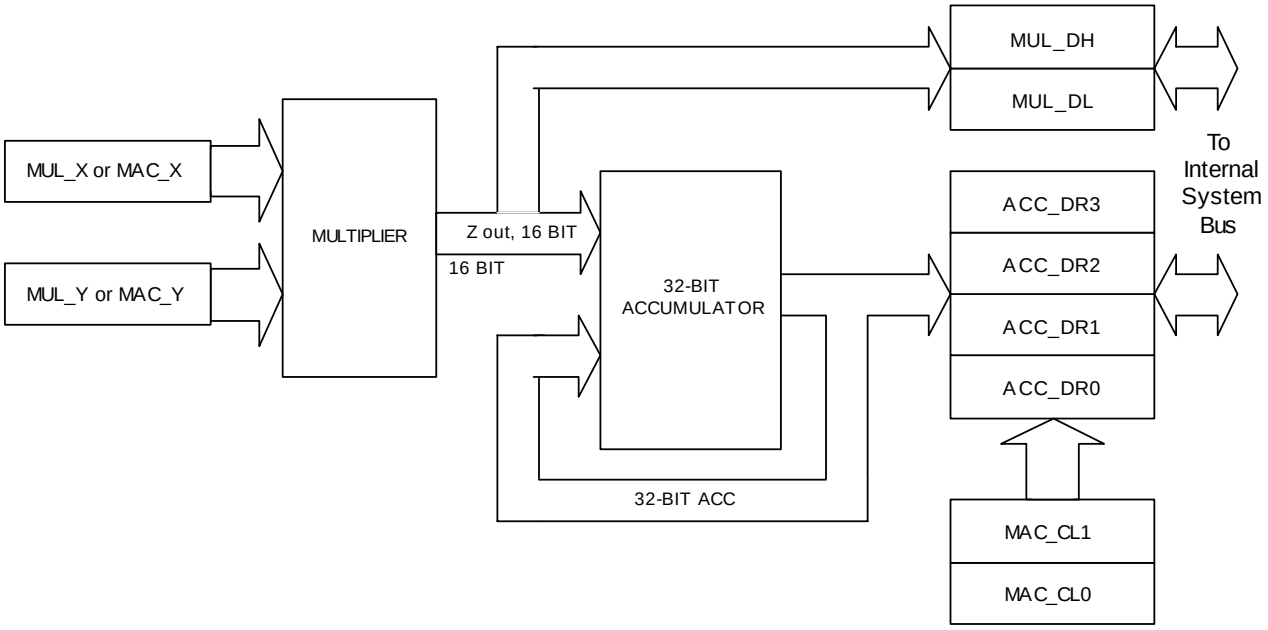

Figure 29: Multiply/Accumulate Block Diagram

Table 83: Multiply Input X Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]** 8-bit data is the input value for X multiplier								

Multiply Input X Register (MUL_X, Address = Bank 0, E8h)

Table 84: Multiply Input Y Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]** 8-bit data is the input value for Y multiplier								

Multiply Input Y Register (MUL_Y, Address = Bank 0, E9h)

13.2 DC Characteristics

Table 104: DC Operating Specifications

Symbol	DC Operating Specifications	Minimum	Typical	Maximum	Unit
V_{cc}	Supply Voltage	3.00	-	5.25	V
I_{cc}	Supply Current	-	5	8[1]	mA
I_{sb}	Sleep (Mode) Current	-	-	5[2]	µA
I_{sbxtl}	Sleep (Mode) Current with Crystal Oscillator	-	3	5[3]	µA
V_{ref}	Reference Voltage (Bandgap)	1.275	1.3	1.325[4]	V
V_{il}	Input Low Voltage	-	-	0.8	V
V_{ih}	Input High Voltage	2.2	-	-	V
V_h	Hysterisis Voltage	-	60	-	mV
V_{ol}	Output Low Voltage	-	-	Vss+0.75[5]	V
V_{oh}	Output High Voltage	V_{cc}-1.0[6]	-	-	V
R_{pu}	Pull Up Resistor Value	4000	5600	8000	Ω
R_{pd}	Pull Down Resistor Value	4000	5600	8000	Ω
I_{il}	Input Leakage (Absolute Value)	-	0.1	5	µA
C_{in}	Capacitive Load on Pins as Input	0.5	1.7	10[7]	pF
C_{out}	Capacitive Load on Pins as Output	0.5	1.7	10[7]	pF
V_{LVD}	LVD and SMP Tolerance[8]	0.95 x Ideal[8]	Ideal	1.05 x Ideal[8]	V

1. Conditions are 5.0V, 25 ^{o}C, 3 MHz.
2. Without Crystal Oscillator, V_{cc} = 3.3 V, TA <= 85 ^{o}C.
3. Conditions are 3.0V <= V_{cc} <= 3.6V, -40 ^{o}C <= TA <= 85 ^{o}C. Correct operation assumes a properly loaded, 1 uW maximum drive level, 32.768 kHz crystal.
4. Trimmed for appropriate V_{cc}.
5. Isink = 25 mA, V_{cc} = 4.5 V (maximum of 8 IO sinking, 4 on each side of the IC).
6. Isource =10 mA, V_{cc} = 4.5 V (maximum of 8 IO sourcing, 4 on each side of the IC).
7. Package dependent.
8. Ideal values are +/- 5% absolute tolerance and +/- 1% tolerance relative to each other (for adjacent levels).