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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26643-24pvi

1.0 Functional Overview

The CPU heart of this next generation family of microcontrollers is a high performance, 8-bit, M8C Harvard architecture microprocessor. Separate program and memory busses allow for faster overall throughput. Processor clock speeds to 24 MHz are available. The processor may also be run at lower clock speeds for power-sensitive applications. A rich instruction set allows for efficient low-level language support.

All devices in this family include both analog and digital configurable peripherals (PSoC blocks). These blocks enable the user to define unique functions during configuration of the device. Included are twelve analog PSoC blocks and eight digital PSoC blocks. Potential applications for the digital PSoC blocks are timers, counters, UARTs, CRC generators, PWMs, and other functions. The analog PSoC blocks can be used for SAR ADCs, Multi-slope ADCs, programmable gain amplifiers, programmable filters, DACs, and other functions. Higher order User Modules such as modems, complex motor controllers, and complete sensor signal chains can be created from these building blocks. This allows for an unprecedented level of flexibility and integration in microcontroller-based systems.

A Multiplier/Accumulator (MAC) is available on all devices in this family. The MAC is implemented on this device as a peripheral that is mapped into the register space. When an instruction writes to the MAC input registers, the result of an 8x8 multiply and a 32-bit accumulate are available to be read from the output registers on the next instruction cycle.

The number of general purpose I/Os available in this family of parts range from 6 to 44. Each of these I/O pins has a variety of programmable options. In the output mode, the user can select the drive strength desired. Any pin can serve as an interrupt source, and can be selected to trigger on positive edges, negative edges, or any change. Digital signal sources can be routed directly from a pin to the digital PSoC blocks. Some pins have additional capability to route analog signals to the analog PSoC blocks.

Multiple oscillator options are available for use in clocking the CPU, analog PSoC blocks and digital PSoC blocks. These options include an internal main oscillator running at 48/24 MHz, an external crystal oscillator for use with a 32.768 kHz watch crystal, and an internal low-speed oscillator for use in clocking the PSoC blocks and the Watchdog/Sleep timer. User selectable clock divisors allow for optimizing code execution speed and power trade-offs.

The different device types in this family provide various amounts of code and data memory. The code space ranges in size from 4K to 16K bytes of user programmable Flash memory. This memory can be programmed serially in either a programming Pod or on the user board. The endurance on the Flash memory is 50,000 erase/write cycles. The data space is 256 bytes of user SRAM.

A powerful and flexible protection model secures the user's sensitive information. This model allows the user to selectively lock blocks of memory for read and write protection. This allows partial code updates without exposing proprietary information.

Devices in this family range from 8 pins through 48 pins in PDIP, SOIC and SSOP packages.

1.1 Key Features

Table 1: Device Family Key Features

	CY8C25122	CY8C26233	CY8C26443	CY8C26643
Operating Frequency	93.7kHz - 24MHz	93.7kHz - 24MHz	93.7kHz - 24MHz	93.7kHz - 24MHz
Operating Voltage	3.0 - 5.25V	3.0 - 5.25V	3.0 - 5.25V	3.0 - 5.25V
Program Memory (KBytes)	4	8	16	16
Data Memory (Bytes)	256	256	256	256
Digital PSoC Blocks	8	8	8	8
Analog PSoC Blocks	12	12	12	12
I/O Pins	6	16	24	40/44
External Switch Mode Pump	No	Yes	Yes	Yes
Available Packages	8 PDIP	20 PDIP	28 PDIP	48 PDIP
		20 SOIC	28 SOIC	48 SSOP
		20 SSOP	28 SSOP	44 TQFP

Table 4: Pin-out 28 Pin

Name	I/O	Pin	Description
P0[7]	I/O	1	Port 0[7] (Analog Input)
P0[5]	I/O	2	Port 0[5] (Analog Input/ Output)
P0[3]	I/O	3	Port 0[3] (Analog Input/ Output)
P0[1]	I/O	4	Port 0[1] (Analog Input)
P2[7]	I/O	5	Port 2[7]
P2[5]	I/O	6	Port 2[5]
P2[3]	I/O	7	Port 2[3] (Non-Multiplexed Analog Input)
P2[1]	I/O	8	Port 2[1] (Non-Multiplexed Analog Input)
SMP	O	9	Switch Mode Pump
P1[7]	I/O	10	Port 1[7]
P1[5]	I/O	11	Port 1[5]
P1[3]	I/O	12	Port 1[3]
P1[1]	I/O	13	Port 1[1] / XtalIn / SCLK
Vss	Power	14	Ground
P1[0]	I/O	15	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	16	Port 1[2]
P1[4]	I/O	17	Port 1[4]
P1[6]	I/O	18	Port 1[6]
XRES	I	19	External Reset
P2[0]	I/O	20	Port 2[0] (Non-Multiplexed Analog Input)
P2[2]	I/O	21	Port 2[2] (Non-Multiplexed Analog Input)
P2[4]	I/O	22	Port 2[4] / External AGNDIn
P2[6]	I/O	23	Port 2[6] / External VREFIn
P0[0]	I/O	24	Port 0[0] (Analog Input)
P0[2]	I/O	25	Port 0[2] (Analog Input/Output)
P0[4]	I/O	26	Port 0[4] (Analog Input/Output)
P0[6]	I/O	27	Port 0[6] (Analog Input)
Vcc	Power	28	Supply Voltage

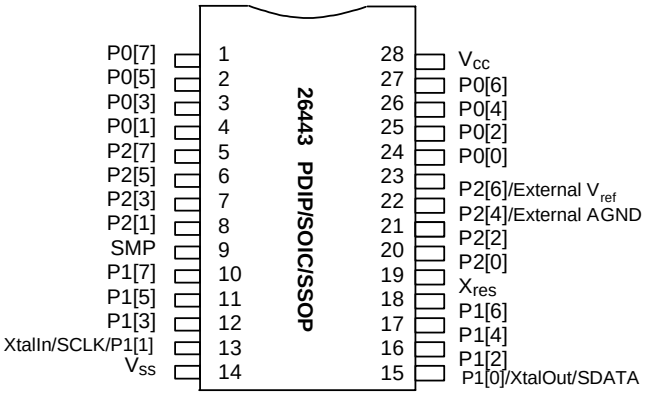

Figure 4: 26443 PDIP/SOIC/SSOP

Table 5: Pin-out 44 Pin

Name	I/O	Pin	Description
P2[5]	I/O	1	Port 2[5]
P2[3]	I/O	2	Port 2[3] (Non-Multiplexed Analog Input)
P2[1]	I/O	3	Port 2[1] (Non-Multiplexed Analog Input)
P3[7]	I/O	4	Port 3[7]
P3[5]	I/O	5	Port 3[5]
P3[3]	I/O	6	Port 3[3]
P3[1]	I/O	7	Port 3[1]
SMP	O	8	Switch Mode Pump
P4[7]	I/O	9	Port 4[7]
P4[5]	I/O	10	Port 4[5]
P4[3]	I/O	11	Port 4[3]
P4[1]	I/O	12	Port 4[1]
P1[7]	I/O	13	Port 1[7]
P1[5]	I/O	14	Port 1[5]
P1[3]	I/O	15	Port 1[3]
P1[1]	I/O	16	Port 1[1] / XtalIn / SCLK
Vss	Power	17	Ground
P1[0]	I/O	18	Port 1[0] / XtalOut / SDATA
P1[2]	I/O	19	Port 1[2]
P1[4]	I/O	20	Port 1[4]
P1[6]	I/O	21	Port 1[6]
P4[0]	I/O	22	Port 4[0]
P4[2]	I/O	23	Port 4[2]
P4[4]	I/O	24	Port 4[4]

Table 6: Pin-out 48 Pin, continued

P5[0]	I/O	29	Port 5[0]
P5[2]	I/O	30	Port 5[2]
P4[0]	I/O	31	Port 4[0]
P4[2]	I/O	32	Port 4[2]
P4[4]	I/O	33	Port 4[4]
P4[6]	I/O	34	Port 4[6]
XRES	I	35	External Reset
P3[0]	I/O	36	Port 3[0]
P3[2]	I/O	37	Port 3[2]
P3[4]	I/O	38	Port 3[4]
P3[6]	I/O	39	Port 3[6]
P2[0]	I/O	40	Port 2[0] (Non-Multiplexed Analog Input)
P2[2]	I/O	41	Port 2[2] (Non-Multiplexed Analog Input)
P2[4]	I/O	42	Port 2[4] / External AGNDIn
P2[6]	I/O	43	Port 2[6] / External VREFIn
P0[0]	I/O	44	Port 0[0] (Analog Input)
P0[2]	I/O	45	Port 0[2] (Analog Input/Output)
P0[4]	I/O	46	Port 0[4] (Analog Input/Output)
P0[6]	I/O	47	Port 0[6] (Analog Input)
Vcc	Power	48	Supply Voltage

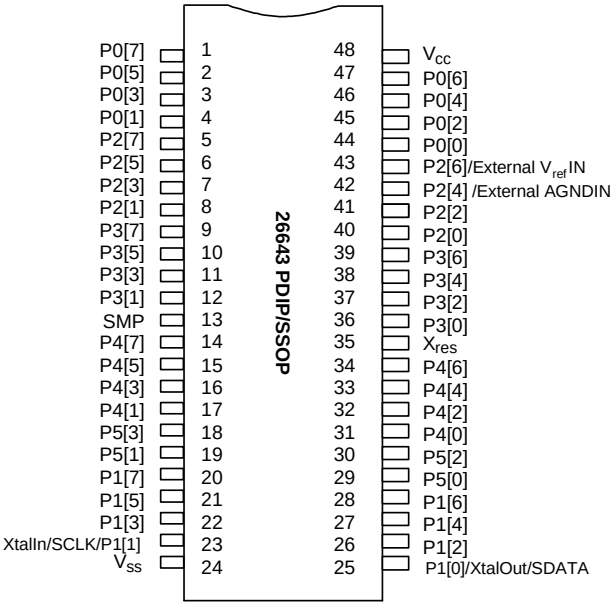

Figure 6: 26643 PDIP/SSOP

Examples:

```
                        ;In this case, the
                        ;value in the memory
                        ;location at address
                        ;7 is added with the
ADD    [7],     A      ;Accumulator, and the
                        ;result is placed in
                        ;the memory location
                        ;at address 7. The
                        ;Accumulator is
                        ;unchanged.
                        ;In this case, the
                        ;Accumulator is moved
                        ;to the register
MOV    REG[8], A        ;space location at
                        ;address 8. The
                        ;Accumulator is
                        ;unchanged.
```

2.3.5 Destination Indexed

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is added to the X register forming the address that points to the location of the result. The source for the instruction is the A register. Arithmetic instructions require two sources, the second source is the location specified by Operand 1 added with the X register. Instructions using this addressing mode are two bytes in length.

Table 17: Destination Indexed

Opcode	Operand 1
Instruction	Destination Index

Example:

```
                        ;In this case, the value
                        ;in the memory location
                        ;at address X+7 is added
                        ;with the Accumulator,
ADD  [X+7],   A         ;and the result is placed
                        ;in the memory location
                        ;at address x+7. The
                        ;Accumulator is
                        ;unchanged.
```

2.3.6 Destination Direct Immediate

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is the address of the result. The source for the instruction is Operand 2, which is an immediate value. Arithmetic instructions require two sources, the second source is the location specified by Operand 1. Instructions using this addressing mode are three bytes in length.

Table 18: Destination Direct Immediate

Opcode	Operand 1	Operand 2
Instruction	Destination Address	Immediate Value

Examples:

```
                        ;In this case, value in
                        ;the memory location at
                        ;address 7 is added to
ADD  [7],     5         ;the immediate value of
                        ;5, and the result is
                        ;placed in the memory
                        ;location at address 7.
                        ;In this case, the
                        ;immediate value of 6 is
MOV  REG[8], 6          ;moved into the register
                        ;space location at
                        ;address 8.
```

2.3.7 Destination Indexed Immediate

The result of an instruction using this addressing mode is placed within either the RAM memory space or the register space. Operand 1 is added to the X register to form the address of the result. The source for the instruction is Operand 2, which is an immediate value. Arithmetic instructions require two sources, the second source is the location specified by Operand 1 added with the X register. Instructions using this addressing mode are three bytes in length.

Table 19: Destination Indexed Immediate

Opcode	Operand 1	Operand 2
Instruction	Destination Index	Immediate Value

Table 37: External Crystal Oscillator Trim Register

Bit #	7	6	5	4	3	2	1	0
POR	FS[1]	FS[1]	0	0	FS[1]	FS[1]	FS[1]	FS[1]
Read/Write	W	W	--	--	W	W	W	W
Bit Name	PSSDC [1]	PSSDC [0]	Reserved	Reserved	Amp [1]	Amp [0]	Bias [1]	Bias [0]

Bit [7:6]: **PSSDC [1:0]** Power System Sleep Duty Cycle. (Not recommended for customer alteration)
0 0 = 1/128
0 1 = 1/512
1 0 = 1/32
1 1 = 1/8

Bit 5: **Reserved**
Bit 4: **Reserved**

Bit [3:2]: **Amp [1:0]** Sets the amplitude of the adjustment. (Not recommended for customer alteration)

Bit [1:0]: **Bias [1:0]** Sets the bias of the adjustment. (Not recommended for customer alteration)

1. FS = Factory set trim value

External Crystal Oscillator Trim Register (ECO_TR, Address = Bank 1, EBh)

7.1.4 External Crystal Oscillator Component Connections and Selections

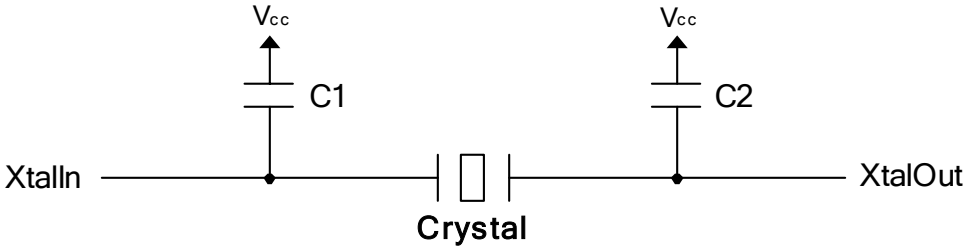

Figure 8: External Crystal Oscillator Connections

- Crystal – 32.768 kHz watch crystal such as EPSON C-002RX (12.5 pF load capacitance)
- Capacitors – C1, C2
  Use NPO-type ceramic caps
  C1 = C2 = 25 pF - (Package Cap) - (Board Parasitic Cap)

Note: Use this equation if you do not employ PLL mode. If you do employ PLL with the External Crystal Oscillator, see Application Note AN2027 under **Support** at http://www.cypressmicro.com for equation and details. An error of 1 pF in C1 and C2 gives about 3 ppm error in frequency.

Table 38: Typical Package Capacitances

Package	Package Capacitance
8 PDIP	0.9 pF
20 PDIP	2 pF
20 SOIC	1 pF
20 SSOP	0.5 pF
28 PDIP	2 pF
28 SOIC	1 pF
28 SSOP	0.5 pF
44 TQFP	0.5 pF
48 PDIP	5 pF
48 SSOP	0.6 pF

8.4 Interrupt Masks

Table 44: General Interrupt Mask Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Sleep	GPIO	Acolumn3	Acolumn2	Acolumn1	Acolumn0	Voltage Monitor

Bit 7: **Reserved**

Bit 6: **Sleep Interrupt Enable Bit (see 11.4)**
0 = Disabled
1 = Enabled

Bit 5: **GPIO Interrupt Enable Bit (see 8.6)**
0 = Disabled
1 = Enabled

Bit [4]: **Acolumn 3 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [3]: **Acolumn 2 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [2]: **Acolumn 1 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit [1]: **Acolumn 0 Interrupt Enable Bit (see 10.0)**
0 = Disabled
1 = Enabled

Bit 0: **Voltage Monitor Interrupt Enable Bit (see 11.5)**
0 = Disabled
1 = Enabled

General Interrupt Mask Register (INT_MSK0, Address = Bank 0, E0h)

Table 47: Digital Basic Type A/ Communications Type A Block xx Function Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Reserved	End	Mode 1	Mode 0	Function [2]	Function [1]	Function [0]

Bit 7: **Reserved**
Bit 6: **Reserved**

Bit 5: **End**
0 = PSoC block is not the end of a chained function (End should not be set to 0 in block DCA07)
1 = PSoC block is the end of a chained function, or is an unchained PSoC block

Bit 4: **Mode 1** The definition of the Mode [1] bit depends on the block function selected
Timer: The Mode [1] bit signifies the Compare Type
0 = Less Than or Equal
1 = Less Than
Counter: The Mode [1] bit signifies the Compare Type
0 = Less Than or Equal
1 = Less Than
CRC/PRS: The Mode [1] bit is unused in this function
Deadband: The Mode [1] bit is unused in this function
UART: The Mode[1] bit signifies the Interrupt Type (Transmitter only)
0 = Transmit: Interrupt on TX_Reg Empty
1 = Transmit: Interrupt on TX Complete
SPI: The Mode[1] bit signifies the Interrupt Type
0 = Master: Interrupt on TX Reg Empty, Slave: Interrupt on RX Reg Full
1 = Master: Interrupt on SPI Complete, Slave: Interrupt on SPI Complete

Bit 3: **Mode 0** The definition of the Mode [0] bit depends on the block function selected
Timer: The Mode [0] bit signifies Interrupt Type
0 = Terminal Count
1 = Compare True
Counter: The Mode [0] bit signifies Interrupt Type
0 = Terminal Count
1 = Compare True
CRC/PRS: The Mode [0] bit is unused in this function
Deadband: The Mode [0] bit is unused in this function
UART: The Mode [0] bit signifies the Direction
0 = Receive
1 = Transmit
SPI: The Mode [0] bit signifies the Type
0 = Master
1 = Slave

Bit [2:0]: **Function [2:0]** The Function [2:0] bits select the block function which determines the basic hardware configuration
0 0 0 = Timer (chainable)
0 0 1 = Counter (chainable)
0 1 0 = CRC/PRS (Cyclical Redundancy Checker or Pseudo Random Sequencer) (chainable)
0 1 1 = Reserved
1 0 0 = Deadband for Pulse Width Modulator
1 0 1 = UART (function only available on DCA type blocks)
1 1 0 = SPI (function only available on DCA type blocks)
1 1 1 = Reserved

Digital Basic Type A Block 00 Function Register (DBA00FN, Address = Bank 1, 20h)
Digital Basic Type A Block 01 Function Register (DBA01FN, Address = Bank 1, 24h)
Digital Basic Type A Block 02 Function Register (DBA02FN, Address = Bank 1, 28h)
Digital Basic Type A Block 03 Function Register (DBA03FN, Address = Bank 1, 2Ch)
Digital Communications Type A Block 04 Function Register (DCA04FN, Address = Bank 1, 30h)

2. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 1 (Period) is loaded directly into Data Register 0 (Counter) to initialize or reset the count. All outputs are low and the block interrupt is held low. Disabling a counter does not affect the current count value and it may be read by the CPU. Two reads are required to read each byte of a multi-byte register. One to transfer each Data Register 0 count value to the associated Data Register 2 capture register, then one to read the result in Data Register 2.

3. Reading the Count Value

   A CPU read of Data Register 0 (count value) will overwrite Data Register 2 (compare value). Therefore, when reading the current count, a previously written compare value will be overwritten.

4. Extra Count

   In a Counter User Module, the data input is an enable for counting. Normally, when the enable goes low, the counter will hold the current count. However, if the enable happens to go low in the same clock period as Terminal Count (count of all 0's), one additional count will occur that will reload the counter from the Period Register. Once the counter is reloaded from the Period Register, counting will stop.

9.5.3 Deadband Generator

9.5.3.1 Summary

The Deadband function produces two output waveforms, F0 and F1, with the same frequency as the input, but “under-lapped” so they are never both high at the same time. An 8-bit down counter controls the length of the “dead time” during which both output signals are low. When the deadband function detects a rising edge on the input waveform, the F1 output signal goes low and the counter decrements from its initial value to its terminal count. When the down counter reaches zero, the F0 output signal goes high. The process reverses on the falling edge of the input waveform so that after the same dead time, F1 goes high until the input signal transitions again. Dead-band generator PSoC blocks cannot be chained to increase the width of the down counter beyond 8 bits or 256 dead-time “ticks.”

9.5.3.2 Registers

Data Register 1 stores the count that controls the elapsed dead time. Data Register 0 holds the current state of the dead-time down counter. If the function is disabled, writing a period into Data Register 1, will automatically load Data Register 0 with the deadband period. This period is automatically re-loaded into the counter on each edge of the input signal. Data Register 2 is unused. Control Register 0 contains one bit to enable/disable the function.

9.5.3.3 Inputs

The input controls the period and duty cycle of the dead-band generator outputs. This input is fixed to be derived from the primary output of the previous block. If this signal is pulse-width modulated, i.e., if a PWM block is configured as the previous block, the dead-band outputs will be similarly modulated. The F0 output corresponds to the duty cycle of the input (less the dead time) and F1 to the duty cycle of the inverted input (again, less the dead time). The clock input to the dead-band generator controls the rate at which the down counter is decremented. The primary data input is the “Kill” Signal. When this signal is asserted high, both F0 and F1 outputs will go low. The multiplexers selecting these input are controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.3.4 Outputs

Both the F0 and F1 outputs can be driven onto the Global Output bus. If the next PSoC block selects “Previous PSoC block” for its clock input, it only “sees” the F0 output of the dead-band function. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.3.5 Interrupts

The rising edge of the F0 signal provides the interrupt for this block.

9.5.3.6 Usage Notes

1. Constraints

   The dead time must not exceed the minimum of the input signal’s pulse-width high and pulse-width low time, less two CPU clocks. Dead time equals the period of the input clock times one plus the value written to Data Register 1.

9.5.4.6 Determining the Polynomial

A simple linear-feedback shift register, or LFSR, uses an XOR gate to “add” the values of one or more bits and feed the result back into the least-significant bit. One possible realization of a 6-bit LFSR providing a maximal sequence of 63 six-bit values is shown here:

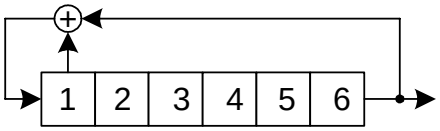

Figure 13: Polynomial LFSR

The PRS function utilizes a different “modular” architecture with one XOR gate between each bit of the shift register. A maximal sequence equivalent to that produced by the previous realization is generated by the following modular LFSR

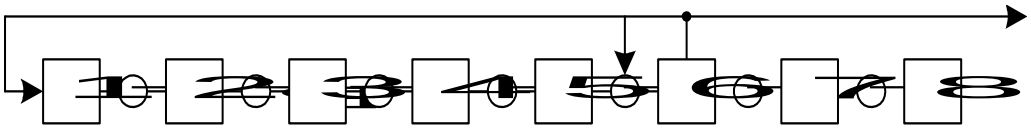

Figure 14: Polynomial PRS

Denote the first implementation as a (6, 1) LFSR, where 6 gives the length of the output codes and 1 indicates the tap which feeds the XOR gate along with the final bit. Then the modular form just shown is denoted as a [6, 5] LFSR. In general, the equivalent modular form of a simple N bit LFSR with M taps denoted by (N, t_1, t_2, …, t_M) is given by the notation [N, N-t_1, N-t_2, …, N-t_M]. Once the form (and thus the notation) is determined, the value of Data Register 1 is easily determined. The bit corresponding to the length and all tap bits are turned on; the others are zero. Thus, the polynomial specification for Data Register 1 to implement a [6, 5] LFSR is 00110000b, or 30h. A maximal sequence PRS for 8-bits giving 255 codes is [8, 4, 3, 2] with polynomial 10001110b or 8Eh.

9.5.4.7 Usage Notes

1. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 2 (Seed) is loaded directly into Data Register 0 (LFSR) to initialize or reset the seed value. All outputs are low and the block interrupt is held low.

2. Reading the LFSR

   The current LFSR value can only be read when the block is disabled by setting the Control Register bit 0 to low. Each byte of the current LFSR value (in the case of a multi-byte block) must be read individually. The Data Register 0 byte (LFSR), which returns 0, then the Data Register 1 byte, which returns the actual value.

9.5.5 CRC - Cyclic Redundancy Check

9.5.5.1 Summary

The CRC uses a shift register and XOR gates like the PRS function. However, instead of an output bit stream, the CRC function expects an input bit stream. Functionally the CRC block is identical to the PRS with the exception of the selected input data. Input data must be presented synchronously to the clock. A polynomial specification permits the length of the input sequence over which the cyclic redundancy check computes a result to be varied. CRC-configured PSoC blocks can be chained to form longer results.

9.5.5.2 Registers

Data Register 0 implements a linear-feedback shift register. Data Register 2 holds the “seed” value and when the block is disabled, a write to Data Register 2 is loaded

directly into Data Register 0 (The block must be disabled when writing this value). Data Register 1 specifies the polynomial and width of the numbers in the sequence (see “Specifying the Polynomial”, below). Once the input bit stream is complete, the result may be read by first reading Data Register 0, which returns 0, then reading Data Register 2, which returns the actual result.

9.5.5.3 Inputs

The clock input determines the rate at which the input sequence is processed. The data input selects the data stream to process. It is assumed that the data is valid on the positive edge of the clock input. The multiplexer for selecting these inputs is controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.5.4 Outputs

Like the PRS, the CRC function drives the output serial data stream with the most significant bit of CRC processing synchronous with the input clock. Normally the CRC output is not used. The output may be driven on the Global Output bus or to the subsequent digital PSoC block. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.5.5 Interrupts

The CRC function provides an interrupt based on the Compare signal between Data Register 0 and Data Register 2.

9.5.5.6 Specifying the Polynomial

Computation of an N-bit result is generally specified by a polynomial with N+1 terms, the last of which is the X^0 term, where X^0=1. For example, the widely used CRC-CCIT 16-bit polynomial is $X^{16}+X^{12}+X^5+1$. The PSoC block CRC function assumes the presence of the X^0 term so that the polynomial for an N-bit result can be expressed by an N-bit rather than N+1 bit specification. To obtain the PSoC block register specification, write an N+1 bit binary number corresponding to the full polynomial, with 1’s for each term present. The CRC-CCIT polynomial would be 10001000000100001b. Simply drop the right-most bit (the X^0 term) to obtain the register specification for the PSoC block. To implement the CRC-CCIT example, two PSoC blocks must be chained together. Data Register 1 in the high-order PSoC block would take the value 10001000b (88h) and the corresponding register in the low-order PSoC block would take 00010000b (10h).

9.5.5.7 Usage Notes

1. Disabled State

   When the Control Register Enable bit is set to ‘0’, the internal block clock is turned off. A write to Data Register 2 (Seed) is loaded directly into Data Register 0 (LFSR) to initialize or reset the seed value. All outputs are low and the block interrupt is held low.

2. Reading the CRC value

   After the data stream has been processed by the LFSR, the residue is the CRC value. The current LFSR value can only be read when the block is disabled by setting the Control Register bit 0 to low. Each byte of the current LFSR value (in the case of a multi-byte block) must be read individually. The Data Register 0 byte (LFSR) must be read, which returns 0, then the Data Register 2 byte, which returns the actual value.

9.5.6 Universal Asynchronous Receiver

9.5.6.1 Summary

The Universal Asynchronous Receiver implements the input half of a basic 8-bit UART. Start and Stop bits are recognized and stripped. Parity type and parity validation are configurable features. This function requires a Digital Communications Type PSoC block and cannot be chained for longer data words.

9.5.6.2 Registers

The function shifts incoming data into Data Register 0. Once complete, the byte is transferred to Data Register 2 from which it may be read. Data Register 2 acts as a 1 byte receive buffer. Data Register 1 is not used by this function. Control Register 0 (DCA04CR0-DCA07CR0) enables the function, provides the means to configure parity checking, and a full set of status indications. See the register definition for full details.

only be input from GPIO input pins (Global Input Bus). There is no way to enable the SS_internally. In SPI modes 2 & 3, where SS is not required between each byte, the external pin may be grounded.

Important: The AUX Out Enable bit (bit 5) of the Output Register (DCA04OU-DCA07OU) must be set to 0 to disable it.

9.5.9.4 Outputs

The function output is the MISO (master-in, slave-out) signal, which may be driven on the Global Output bus and is selected by Output Register (DCA04OU-DCA07OU).

9.5.9.5 Interrupts

When enabled, the function generates an interrupt on RX Reg Full status (Data Register 2 full). If Mode[1] of the Function Register is set, the interrupt will be generated on SPI Complete status.

9.5.9.6 Usage Notes

1. Reading the Status

   Reading Control Register 0, which contains the status bits, automatically resets the status bits to 0 with the exception of TX Reg Empty, which is cleared when a byte is written to the TX Data Register (Data Register 1), and the RX Reg Full, which is cleared when a byte is read from the RX Data Register (Data Register 2).

2. Multi-Slave Environment

   The SS_ signal does not have any affect on the output from the slave. The output of the slave at the end of a reception/transmission is always the first bit sent (the MSB, unless LSBF option is selected, then it's the LSB). To implement a multi-slave environment, a GPIO interrupt may be configured on the SS_ input, and the Slave output strength may be toggled between driving and High Z in firmware.

3. Using Interrupts

   RX Reg Full status or SPI Complete status generates an interrupt. Executing the interrupt routine does not automatically clear status. If SPI Complete is selected as the interrupt source, Control Register 0 (status) must be read in the interrupt routine to clear the status. If RX Reg Full status is selected, a byte must be read from the RX Data Register (Data Register 2) to clear the status. If the interrupting status is not cleared further interrupts will be suppressed.

4. Synchronization of CPU Interaction

   Because the SPI Slave is clocked asynchronously by the master SCLK, transfer of data between the TX Register to shifter and shifter to RX Register occurs asynchronously.

   Either polling or interrupts can be used to detect that a byte has been received and is ready to read. However, on the TX side, the user is responsible for implementing a protocol that ensures there is enough set-up time from the TX Data Register write to the first clock (mode 2, 3) or SS_ (mode 0, 1) from the master.

Table 62: AGND, RefHI, RefLO Operating Parameters

	AGND		RefHI		RefLO		Notes
	Source	**Voltage**	**Source**	**Voltage**	**Source**	**Voltage**	
000	$V_{cc}/2$	2.5 V 1.65 V	V_{cc}+Vbg	3.8 V 2.95 V	V_{cc}-Vbg	1.2 V 0.35 V	5.0 V System 3.3 V System
001	P2[4]	2.2 V[1]	P2[4]+P2[6]	3.2 V[1]	P2[4]-P2[6]	1.2 V[1]	User Adjustable
010	Vcc/2	2.5 V 1.65 V	Vcc	5.0 V 3.3 V	Vss	0.0 V 0.0 V	5.0 V System 3.3 V System
011	2*Vbg	2.6 V	2*Vbg+Vbg	3.9 V	2*Vbg-Vbg	1.3 V	Not for 3.3 V Systems
100	2*Vbg	2.6 V	2*Vbg+P2[6]	3.6 V[1]	2*Vbg-P2[6]	1.6 V[1]	Not for 3.3 V Systems
101	P2[4]	2.2 V[1]	P2[4]+Vbg	3.5 V[1]	P2[4]-Vbg	0.9 V[1]	User Adjustable
110	Reserved						
111	Reserved						

1. Example shown for AGND P2[4] = 2.2 V and Ref P2[6] = 1.0 V

10.4.4 Analog Array Power Control

PWR Sets Analog Array Power Control. Analog array power is controlled through the bias circuits in the Continuous Time blocks and separate bias circuits in the Switched Capacitor blocks. Continuous Time blocks (ACAxx) can be operated to make low power comparators independent of Switched Capacitor (ASAxx and ASBxx) blocks, without their power consumption.

The reference array supplies voltage to all blocks and current to the Switched Capacitor blocks. At higher block clock rates, there is increased reference current demand; the reference power should be set equal to the highest power level of the analog blocks used.

divided into distinct bit fields. Some bit fields set the PSoC block's resistor ratios or capacitor values. Others configure switches and multiplexers that form connections between internal block nodes. Additionally, a block may be connected via local interconnection resources to neighboring analog PSoC blocks, reference voltage sources, input multiplexers and output busses. Specific advantages and applications of each type are treated separately below.

10.6.1 Local Interconnect

Analog continuous-time PSoC blocks occupy the top row, (row 0) of the analog array. Designated ACA for analog continuous-time subtype "A," each connects to its neighbors by means of three multiplexers. (Note that unlike the switched capacitor blocks, the continuous time blocks in the current family of parts only have one subtype.) The three are the non-inverting input multiplexer, "PMux," the inverting input multiplexer, "NMux," and the "RBotMux" which controls the node at the bottom of the resistor string. The bit fields, which control these multiplexers, are named PMux, NMux, and RBotMux, respectively. The following diagrams show how each multiplexer connects its ACA block connect to its neighbors. Each arrow points from an input source, either a PSoC block, bus or reference voltage to the block where it is used. Each arrow is labeled with the value to which the bit-field must be set to select that input source.

10.6.1.1 NMux

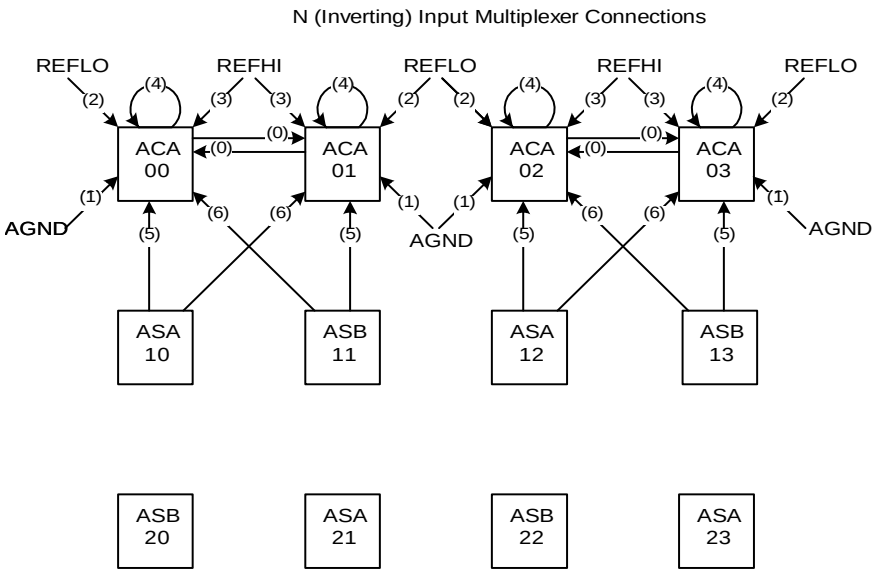

Figure 18: NMux Connections

10.7 Analog Continuous Time PSoC Blocks

10.7.1 Introduction

The Analog Continuous Time PSoC blocks are built around an operational amplifier. There are several analog muxes that are controlled by register-bit settings in the control registers that determine the signal topology inside the block. There is also a precision resistor matrix that is located in the feedback path for the op-amp, and is controlled by register-bit setting. There is also an analog comparator connected to the output OUT, which converts analog comparisons into digital signals.

There are five discrete outputs from this block. These outputs are:

1. The analog output bus (ABUS), which is an analog bus resource that is shared by all of the analog blocks in the analog column for that block.

2. The comparator bus (CBUS), which is a digital bus that is a resource that is shared by all of the analog blocks in a column for that block.

3. The output bus (OUT, GOUT and LOUT), which is an analog bus resource that is shared by all of the analog blocks in a column and connects to one of the analog output buffers, to send a signal externally to the device.

This block supports Programmable Gain or attenuation Op-Amp Circuits, (Differential Gain) Instrumentation Amplifiers (using two CT Blocks), Continuous time high frequency anti-aliasing filters, and modest response-time analog comparators.

inverting op-amp input) or for loss (center tap to output of the block). Note that setting Gain alone does not guarantee a gain or loss block. Routing of the other ends of the resistor determine this.

Note that connections between GIN and GOUT, and LIN and LOUT are automatically resolved by PSoC Designer when they are set in a differential configuration with an adjacent CT block.

Table 66: Analog Continuous Time Block xx Control 0 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	RTap-Mux[3]	RTap-Mux[2]	RTap-Mux[1]	RTap-Mux[0]	Gain	RTopMux	RBotMux[1]	RBotMux[0]

Bit [7:4]: **RTapMux [3:0]** Encoding for selecting 1 of 16 resistor taps
0 0 0 0 = Rf 15 = Ri 01 = Loss .0625 / Gain 16.00
0 0 0 1 = Rf 14 = Ri 02 = Loss .1250 / Gain 8.000
0 0 1 0 = Rf 13 = Ri 03 = Loss .1875 / Gain 5.333
0 0 1 1 = Rf 12 = Ri 04 = Loss .2500 / Gain 4.000
0 1 0 0 = Rf 11 = Ri 05 = Loss .3125 / Gain 3.200
0 1 0 1 = Rf 10 = Ri 06 = Loss .3750 / Gain 2.667
0 1 1 0 = Rf 09 = Ri 07 = Loss .4375 / Gain 2.286
0 1 1 1 = Rf 08 = Ri 08 = Loss .5000 / Gain 2.000
1 0 0 0 = Rf 07 = Ri 09 = Loss .5625 / Gain 1.778
1 0 0 1 = Rf 06 = Ri 10 = Loss .6250 / Gain 1.600
1 0 1 0 = Rf 05 = Ri 11 = Loss .6875 / Gain 1.455
1 0 1 1 = Rf 04 = Ri 12 = Loss .7500 / Gain 1.333
1 1 0 0 = Rf 03 = Ri 13 = Loss .8125 / Gain 1.231
1 1 0 1 = Rf 02 = Ri 14 = Loss .8750 / Gain 1.143
1 1 1 0 = Rf 01 = Ri 15 = Loss .9375 / Gain 1.067
1 1 1 1 = Rf 00 = Ri 16 = Loss 1.000 / Gain 1.000

Bit 3: **Gain** Select gain or loss configuration for output tap
0 = Loss
1 = Gain

Bit 2: **RTopMux** Encoding for feedback resistor select
0 = Rtop to Vcc
1 = Rtop to op-amp's output

Bit [1:0]: **RBotMux [1:0]** Encoding for feedback resistor select

	ACA00	ACA01	ACA02	ACA03
0 0 =	ACA01	ACA00	ACA03	ACA02
0 1 =	AGND	AGND	AGND	AGND
1 0 =	Vss	Vss	Vss	Vss
1 1 =	ASA10	ASB11	ASA12	ASB13

Analog Continuous Time Block 00 Control 0 Register (ACA00CR0, Address = Bank 0/1, 71h)
Analog Continuous Time Block 01 Control 0 Register (ACA01CR0, Address = Bank 0/1, 75h)
Analog Continuous Time Block 02 Control 0 Register (ACA02CR0, Address = Bank 0/1, 79h)
Analog Continuous Time Block 03 Control 0 Register (ACA03CR0, Address = Bank 0/1, 7Dh)

Table 73: Analog Switch Cap Type B Block xx Control 0 Register, continued

Bit 7: **FCap** F Capacitor value selection bit
0 = 16 capacitor units
1 = 32 capacitor units

Bit 6: **ClockPhase** Clock phase select, will invert clocks internal to the blocks. During normal operation of an SC block for the amplifier of a column enabled to drive the output bus, the connection is only made for the last half of PHI2 (during PHI1 and for the first half of PHI2, the output bus floats at the last voltage to which it was driven). This forms a sample and hold operation using the output bus and its associated capacitance. This design prevents the output bus from being perturbed by the intermediate states of the SC operation (often a reset state for PHI1 and settling to the valid state during PHI2)

Following are the exceptions: 1) If the ClockPhase bit in CR0 (for the SC block in question) is set to 1, then the output is enabled for the whole of PHI2. 2) If the SHDIS signal is set in bit 6 of the Analog Clock Select Register, then sample and hold operation is disabled for all columns and all enabled outputs of SC blocks are connected to their respective output busses for the entire period of their respective PHI2s

0 = Internal PHI1 = External PHI1
1 = Internal PHI1 = External PHI2

This bit also affects the latching of the comparator output (CBUS). Both clock phases, PHI1 and PHI2, are involved in the output latching mechanism. The capture of the next value to be output from the latch (capture point event) happens during the falling edge of one clock phase, and the rising edge of the other clock phase will cause the value to come out (output point event). This bit determines which clock phase triggers the capture point event, and the other clock will trigger the output point event. The value output to the comparator bus will remain stable between output point events.

0 = Capture Point Event triggered by Falling PHI2, Output Point Event triggered by Rising PHI1
1 = Capture Point Event triggered by Falling PHI1, Output Point Event triggered by Rising PHI2

Bit 5: **ASign**
0 = Input sampled on Internal PHI1, Reference Input sampled on internal PHI2
1 = Input sampled on Internal PHI2, Reference Input sampled on internal PHI1

Bit [4:0]: **ACap [4:0]** Binary encoding for 32 possible capacitor sizes for A Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 0 Register (ASB11CR0, Address = Bank 0/1, 84h)
Analog Switch Cap Type B Block 13 Control 0 Register (ASB13CR0, Address = Bank 0/1, 8Ch)
Analog Switch Cap Type B Block 20 Control 0 Register (ASB20CR0, Address = Bank 0/1, 90h)
Analog Switch Cap Type B Block 22 Control 0 Register (ASB22CR0, Address = Bank 0/1, 98h)

10.9.2.3 Analog Switch Cap Type B Block xx Control 2 Register

AnalogBus gates the output to the analog column bus. The output on the analog column bus is affected by the state of the ClockPhase bit in Control 0 Register (ASB11CR0, ASB13CR0, ASB20CR0, ASB22CR0). If AnalogBus is set to 0, the output to the analog column bus is tri-stated. If AnalogBus is set to 1, the ClockPhase bit selects the signal that is output to the analog-column bus. If the ClockPhase bit is 0, the block output is gated by sampling clock on last part of PHI2. If the ClockPhase bit is 1, the block ClockPhase continuously drives the analog column bus.

CompBus controls the output to the column comparator bus. Note that if the comparator bus is not driven by anything in the column, it is pulled low. The comparator output is evaluated on the rising edge of internal PHI1 and is latched so it is available during internal PHI2.

AutoZero controls the shorting of the output to the inverting input of the op-amp. When shorted, the op-amp is basically a follower. The output is the op-amp offset. By using the feedback capacitor of the integrator, the block can memorize the offset and create an offset cancellation scheme. AutoZero also controls a pair of switches between the A and B branches and the summing node of the op-amp. If AutoZero is enabled, then the pair of switches is active. AutoZero also affects the function of the FSW1 bit in Control 3 Register.

The CCap bits set the value of the capacitor in the C path.

2. The temperature rise from junction to ambient is package specific. (See Table 122 on page 149 for thermal impedances of available packages.) User must limit power consumption to comply with this requirement.

Table 103: Temperature Specifications

Symbol	Temperature Specifications	Minimum	Typical	Maximum	Unit
T_A	Ambient Temperature	-40	24	+85	^oC
T_J	Junction Temperature	-40		100	^oC

13.2 DC Characteristics

Table 104: DC Operating Specifications

Symbol	DC Operating Specifications	Minimum	Typical	Maximum	Unit
V_{cc}	Supply Voltage	3.00	-	5.25	V
I_{cc}	Supply Current	-	5	8[1]	mA
I_{sb}	Sleep (Mode) Current	-	-	5[2]	µA
I_{sbxtl}	Sleep (Mode) Current with Crystal Oscillator	-	3	5[3]	µA
V_{ref}	Reference Voltage (Bandgap)	1.275	1.3	1.325[4]	V
V_{il}	Input Low Voltage	-	-	0.8	V
V_{ih}	Input High Voltage	2.2	-	-	V
V_h	Hysterisis Voltage	-	60	-	mV
V_{ol}	Output Low Voltage	-	-	Vss+0.75[5]	V
V_{oh}	Output High Voltage	V_{cc}-1.0[6]	-	-	V
R_{pu}	Pull Up Resistor Value	4000	5600	8000	Ω
R_{pd}	Pull Down Resistor Value	4000	5600	8000	Ω
I_{il}	Input Leakage (Absolute Value)	-	0.1	5	µA
C_{in}	Capacitive Load on Pins as Input	0.5	1.7	10[7]	pF
C_{out}	Capacitive Load on Pins as Output	0.5	1.7	10[7]	pF
V_{LVD}	LVD and SMP Tolerance[8]	0.95 x Ideal[8]	Ideal	1.05 x Ideal[8]	V

1. Conditions are 5.0V, 25 ^{o}C, 3 MHz.
2. Without Crystal Oscillator, V_{cc} = 3.3 V, TA <= 85 ^{o}C.
3. Conditions are 3.0V <= V_{cc} <= 3.6V, -40 ^{o}C <= TA <= 85 ^{o}C. Correct operation assumes a properly loaded, 1 uW maximum drive level, 32.768 kHz crystal.
4. Trimmed for appropriate V_{cc}.
5. Isink = 25 mA, V_{cc} = 4.5 V (maximum of 8 IO sinking, 4 on each side of the IC).
6. Isource =10 mA, V_{cc} = 4.5 V (maximum of 8 IO sourcing, 4 on each side of the IC).
7. Package dependent.
8. Ideal values are +/- 5% absolute tolerance and +/- 1% tolerance relative to each other (for adjacent levels).