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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 1x8b, 1x11b, 1x12b; D/A 1x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c26643-24pvit

2.4 Instruction Set Summary

Table 23: Instruction Set Summary (Sorted by Mnemonic)

Opcode Hex	Cycles	Bytes	Instruction Format	Flags	Opcode Hex	Cycles	Bytes	Instruction Format	Flags	Opcode Hex	Cycles	Bytes	Instruction Format	Flags
09	4	2	ADC A, expr	C, Z	76	7	2	INC [expr]	C, Z	20	5	1	POP X	
0A	6	2	ADC A, [expr]	C, Z	77	8	2	INC [X+expr]	C, Z	18	5	1	POP A	Z
0B	7	2	ADC A, [X+expr]	C, Z	Fx	13	2	INDEX	Z	10	4	1	PUSH X	
0C	7	2	ADC [expr], A	C, Z	Ex	7	2	JACC		08	4	1	PUSH A	
0D	8	2	ADC [X+expr], A	C, Z	Cx	5	2	JC		7E	10	1	RETI	C, Z
0E	9	3	ADC [expr], expr	C, Z	8x	5	2	JMP		7F	8	1	RET	
0F	10	3	ADC [X+expr], expr	C, Z	Dx	5	2	JNC		6A	4	1	RLC A	C, Z
01	4	2	ADD A, expr	C, Z	Bx	5	2	JNZ		6B	7	2	RLC [expr]	C, Z
02	6	2	ADD A, [expr]	C, Z	Ax	5	2	JZ		6C	8	2	RLC [X+expr]	C, Z
03	7	2	ADD A, [X+expr]	C, Z	7C	13	3	LCALL		28	11	1	ROMX	Z
04	7	2	ADD [expr], A	C, Z	7D	7	3	LJMP		6D	4	1	RRC A	C, Z
05	8	2	ADD [X+expr], A	C, Z	4F	4	1	MOV X, SP		6E	7	2	RRC [expr]	C, Z
06	9	3	ADD [expr], expr	C, Z	50	4	2	MOV A, expr	Z	6F	8	2	RRC [X+expr]	C, Z
07	10	3	ADD [X+expr], expr	C, Z	51	5	2	MOV A, [expr]	Z	19	4	2	SBB A, expr	C, Z
38	5	2	ADD SP, expr		52	6	2	MOV A, [X+expr]	Z	1A	6	2	SBB A, [expr]	C, Z
21	4	2	AND A, expr	Z	53	5	2	MOV [expr], A		1B	7	2	SBB A, [X+expr]	C, Z
22	6	2	AND A, [expr]	Z	54	6	2	MOV [X+expr], A		1C	7	2	SBB [expr], A	C, Z
23	7	2	AND A, [X+expr]	Z	55	8	3	MOV [expr], expr		1D	8	2	SBB [X+expr], A	C, Z
24	7	2	AND [expr], A	Z	56	9	3	MOV [X+expr], expr		1E	9	3	SBB [expr], expr	C, Z
25	8	2	AND [X+expr], A	Z	57	4	2	MOV X, expr		1F	10	3	SBB [X+expr], expr	C, Z
26	9	3	AND [expr], expr	Z	58	6	2	MOV X, [expr]		00	15	1	SSC	
27	10	3	AND [X+expr], expr	Z	59	7	2	MOV X, [X+expr]		11	4	2	SUB A, expr	C, Z
70	4	2	AND F, expr	C, Z	5A	5	2	MOV [expr], X		12	6	2	SUB A, [expr]	C, Z
41	9	3	AND reg[expr], expr	Z	5B	4	1	MOV A, X	Z	13	7	2	SUB A, [X+expr]	C, Z
42	10	3	AND reg[X+expr], expr	Z	5C	4	1	MOV X, A		14	7	2	SUB [expr], A	C, Z
64	4	1	ASL A	C, Z	5D	6	2	MOV A, reg[expr]	Z	15	8	2	SUB [X+expr], A	C, Z
65	7	2	ASL [expr]	C, Z	5E	7	2	MOV A, reg[X+expr]	Z	16	9	3	SUB [expr], expr	C, Z
66	8	2	ASL [X+expr]	C, Z	5F	10	3	MOV [expr], [expr]		17	10	3	SUB [X+expr], expr	C, Z
67	4	1	ASR A	C, Z	60	5	2	MOV reg[expr], A		4B	5	1	SWAP A, X	Z
68	7	2	ASR [expr]	C, Z	61	6	2	MOV reg[X+expr], A		4C	7	2	SWAP A, [expr]	Z
69	8	2	ASR [X+expr]	C, Z	62	8	3	MOV reg[expr], expr		4D	7	2	SWAP X, [expr]	
9x	11	2	CALL		63	9	3	MOV reg[X+expr], expr		4E	5	1	SWAP A, SP	Z
39	5	2	CMP A, expr	if (A=B) Z=1	3E	10	2	MVI A, [[expr]++]	Z	47	8	3	TST [expr], expr	Z
3A	7	2	CMP A, [expr]	if (A<B) C=1	3F	10	2	MVI [[expr]++], A		48	9	3	TST [X+expr], expr	Z
3B	8	2	CMP A, [X+expr]		40	4	1	NOP		49	9	3	TST reg[expr], expr	Z
3C	8	3	CMP [expr], expr		29	4	2	OR A, expr	Z	4A	10	3	TST reg[X+expr], expr	Z
3D	9	3	CMP [X+expr], expr		2A	6	2	OR A, [expr]	Z	72	4	2	XOR F, expr	C, Z
73	4	1	CPL A	Z	2B	7	2	OR A, [X+expr]	Z	31	4	2	XOR A, expr	Z
78	4	1	DEC A	C, Z	2C	7	2	OR [expr], A	Z	32	6	2	XOR A, [expr]	Z
79	4	1	DEC X	C, Z	2D	8	2	OR [X+expr], A	Z	33	7	2	XOR A, [X+expr]	Z
7A	7	2	DEC [expr]	C, Z	2E	9	3	OR [expr], expr	Z	34	7	2	XOR [expr], A	Z
7B	8	2	DEC [X+expr]	C, Z	2F	10	3	OR [X+expr], expr	Z	35	8	2	XOR [X+expr], A	Z
30	9	1	HALT		43	9	3	OR reg[expr], expr	Z	36	9	3	XOR [expr], expr	Z
74	4	1	INC A	C, Z	44	10	3	OR reg[X+expr], expr	Z	37	10	3	XOR [X+expr], expr	Z
75	4	1	INC X	C, Z	71	4	2	OR F, expr	C, Z	45	9	3	XOR reg[expr], expr	Z
										46	10	3	XOR reg[X+expr], expr	Z

Note: Interrupt acknowledge to Interrupt Vector table = 13 cycles.

6.3.2 Port Drive Mode 1 Registers

Table 32: Port Drive Mode 1 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	DM1 [7]	DM1 [6]	DM1 [5]	DM1 [4]	DM1 [3]	DM1 [2]	DM1 [1]	DM1 [0]
Bit [7:0]: **DM1 [7:0]** See truth table for Port Drive Mode 0 Registers, above								

Port 0 Drive Mode 1 Register (PRT0DM1, Address = Bank 1, 01h)
Port 1 Drive Mode 1 Register (PRT1DM1, Address = Bank 1, 05h)
Port 2 Drive Mode 1 Register (PRT2DM1, Address = Bank 1, 09h)
Port 3 Drive Mode 1 Register (PRT3DM1, Address = Bank 1, 0Dh)
Port 4 Drive Mode 1 Register (PRT4DM1, Address = Bank 1, 11h)
Port 5 Drive Mode 1 Register (PRT5DM1, Address = Bank 1, 15h) **Note**: Port 5 is 4-bits wide

6.3.3 Port Interrupt Control 0 Registers

Table 33: Port Interrupt Control 0 Registers

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	IC0 [7]	IC0 [6]	IC0 [5]	IC0 [4]	IC0 [3]	IC0 [2]	IC0 [1]	IC0 [0]
Bit [7:0]: **IC0 [7:0]** The two Interrupt Control bits that control a particular port pin are treated as a pair and are decoded as follows: IC1 [x], IC0 [x] = 0 0 = Disabled (Default) IC1 [x], IC0 [x] = 0 1 = Falling Edge (-) IC1 [x], IC0 [x] = 1 0 = Rising Edge (+) IC1 [x], IC0 [x] = 1 1 = Change from Last Direct Read								

Port 0 Interrupt Control 0 Register (PRT0IC0, Address = Bank 1, 02h)
Port 1 Interrupt Control 0 Register (PRT1IC0, Address = Bank 1, 06h)
Port 2 Interrupt Control 0 Register (PRT2IC0, Address = Bank 1, 0Ah)
Port 3 Interrupt Control 0 Register (PRT3IC0, Address = Bank 1, 0Eh)
Port 4 Interrupt Control 0 Register (PRT4IC0, Address = Bank 1, 12h)
Port 5 Interrupt Control 0 Register (PRT5IC0, Address = Bank 1, 16h) **Note**: Port 5 is 4-bits wide

7.2.3 Digital PSoC Block Clocking Options

All digital PSoC block clocks are a user-selectable choice of **48M**, **24V1**, **24V2**, or **32K**, as well as clocking signals from other digital PSoC blocks or general purpose I/O pins. There are a total of 16 possible clock options for each digital PSoC block. See the **Digital PSoC Block** section for details.

8.0 Interrupts

8.1 Overview

Interrupts can be generated by the General Purpose I/O lines, the Power monitor, the internal Sleep Timer, the eight Digital PSoC blocks, and the four analog columns. Every interrupt has a separate enable bit, which is contained in the General Interrupt Mask Register (INT_MSK0) and the Digital PSoC Block Interrupt Mask Register (INT_MSK1). When the user writes a “1” to a particular bit position, this enables the interrupt associated with that position. There is a single Global Interrupt Enable bit in the Flags Register (CPU_F), which can disable all interrupts, or enable those interrupts that also have their individual interrupt bit enabled. During a reset, the enable bits in the General Interrupt Mask Register (INT_MASK0), the enable bits in the Digital PSoC Block Interrupt Mask Register (INT_MSK1) and the Global Interrupt Enable bit in the Flags Register (CPU_F) are all cleared. The Interrupt Vector Register (INT_VC) holds the interrupt vector for the highest priority pending interrupt when read, and when written will clear all pending interrupts.

If there is only one interrupt pending and an instruction is executed that would mask that pending interrupt (by clearing the corresponding bit in either of the interrupt mask registers at address E0h or E1h in Bank 0), the CPU will take that interrupt. Since the pending interrupt has been cleared and there are no others, the resulting interrupt vector is 0000h and the CPU will jump to the user code at the beginning of Flash. To address this issue, use the macro defined in *m8c.inc* called "M8C_DisableIntMask" in PSoC Designer. This macro brackets the register write with a disable then an enable of global interrupts.

Table 45: Digital PSoC Block Interrupt Mask Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	DCA07	DCA06	DCA05	DCA04	DBA03	DBA02	DBA01	DBA00

Bit 7: **DCA07 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 6: **DCA06 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 5: **DCA05 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 4: **DCA04 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 3: **DBA03 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 2: **DBA02 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 1: **DBA01 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Bit 0: **DBA00 Interrupt Enable Bit**
0 = Disabled
1 = Enabled

Digital PSoC Block Interrupt Mask Register (INT_MSK1, Address = Bank 0, E1h)

8.5 Interrupt Vector Register

Table 46: Interrupt Vector Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

Bit [7:0]: **Data [7:0]**
8-bit data value holds the interrupt vector for the highest priority pending interrupt. Writing to this register will clear all pending interrupts

Interrupt Vector Register (INT_VC, Address = Bank 0, E2h)

9.0 Digital PSoC Blocks

9.1 Introduction

PSoC blocks are user configurable system resources. On-chip digital PSoC blocks reduce the need for many MCU part types and external peripheral components. Digital PSoC blocks can be configured to provide a wide variety of peripheral functions. PSoC Designer Software Integrated Development Environment provides automated configuration of PSoC blocks by simply selecting the desired functions. PSoC Designer then generates the proper configuration information and can print a device data sheet unique to that configuration.

Digital PSoC blocks provide up to eight, 8-bit multipurpose timers/counters supporting multiple event timers, real-time clocks, Pulse Width Modulators (PWM), and CRCs. In addition to all PSoC block functions, communication PSoC blocks support full-duplex UARTs and SPI master or slave functions.

As shown in Figure 12:, there are a total of eight 8-bit digital PSoC blocks in this device family configured as a linear array. Four of these are the Digital Basic Type A blocks and four are the Digital Communications Type A blocks. Each of these digital PSoC blocks can be configured independently, or used in combination.

Each digital PSoC block has a unique Interrupt Vector and Interrupt Enable bit. Functions can be stopped or started with a user-accessible Enable bit.

The Timer/Counter/CRC/PRS/Deadband functions are available on the Digital Basic Type A blocks and also the Digital Communications Type A blocks. The UART and SPI communications functions are only available on the Digital Communications Type A blocks.

There are three configuration registers: the Function Register (DBA00FN-DCA07FN) to select the block function and mode, the Input Register (DBA00IN-DCA07IN) to select data input and clock selection, and the Output Register (DBA00OU-DCA07OU) to select and enable function outputs.

The three data registers are designated Data 0 (DBA00DR0-DCA07DR0), Data 1 (DBA00DR1-DCA07DR1), and Data 2 (DBA00DR2-DCA07DR2). The function of these registers and their bit mapping is dependent on the overall block function selected by the user.

The one Control Register (DBA00CR0-DCA07CR0) is designated Control 0. The function of this register and its bit mapping is dependent on the overall block function selected by the user.

If the CPU frequency is 24 MHz and a PSoC timer/counter of 24-bits or longer is operating at 48 MHz, a write to the block Control Register to enable it (for example, a call to Timer_1_Start) may not start the block properly. In the failure case, the first count will typically be indeterminate as the upper bytes fail to make the first count correctly. However, on the first terminal count, the correct period will be loaded and counted thereafter.

Table 51: Digital Function Outputs

Function	Primary Output	Auxiliary Output	Auxiliary Input
Timer	Terminal Count	Compare True	N/A
Counter	Compare True	Terminal Count	N/A
CRC	N/A	Compare True	N/A
PRS	Serial Data	Compare True	N/A
Deadband	F0	F1	N/A
TX UART	TX Data Out	N/A	N/A
RX UART	N/A	N/A	N/A
SPI Master	MOSI	SCLK	N/A
SPI Slave	MISO	N/A	SS_

9.3 Digital PSoC Block Bank 0 Registers

There are four user registers within each digital PSoC block: three data registers, and one status/control register. The three data registers are DR0, which is a shifter/ counter, and DR1 and DR2 registers, which contain data used during the operation. The status/control register (CR0) contains an enable bit that is used for all configurations. In addition, it contains function-specific status and control, which is outlined below.

9.3.1 Digital Basic Type A / Communications Type A Block xx Data Register 0,1,2

Table 52: Digital Basic Type A / Communications Type A Block xx Data Register 0,1,2

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]	VF[1]
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]
Bit [7:0]: **Data [7:0]**								

1. Varies by function/User Module selection. (See Table 53 on page 55.)

Digital Basic Type A Block 00 Data Register 0 (DBA00DR0, Address = Bank 0, 20h)
Digital Basic Type A Block 00 Data Register 1 (DBA00DR1, Address = Bank 0, 21h)
Digital Basic Type A Block 00 Data Register 2 (DBA00DR2, Address = Bank 0, 22h)
Digital Basic Type A Block 01 Data Register 0 (DBA01DR0, Address = Bank 0, 24h)
Digital Basic Type A Block 01 Data Register 1 (DBA01DR1, Address = Bank 0, 25h)
Digital Basic Type A Block 01 Data Register 2 (DBA01DR2, Address = Bank 0, 26h)
Digital Basic Type A Block 02 Data Register 0 (DBA02DR0, Address = Bank 0, 28h)
Digital Basic Type A Block 02 Data Register 1 (DBA02DR1, Address = Bank 0, 29h)
Digital Basic Type A Block 02 Data Register 2 (DBA02DR2, Address = Bank 0, 2Ah)
Digital Basic Type A Block 03 Data Register 0 (DBA03DR0, Address = Bank 0, 2Ch)
Digital Basic Type A Block 03 Data Register 1 (DBA03DR1, Address = Bank 0, 2Dh)
Digital Basic Type A Block 03 Data Register 2 (DBA03DR2, Address = Bank 0, 2Eh)
Digital Communications Type A Block 04 Data Register 0 (DCA04DR0, Address = Bank 0, 30h)
Digital Communications Type A Block 04 Data Register 1 (DCA04DR1, Address = Bank 0, 31h)
Digital Communications Type A Block 04 Data Register 2 (DCA04DR2, Address = Bank 0, 32h)
Digital Communications Type A Block 05 Data Register 0 (DCA05DR0, Address = Bank 0, 34h)
Digital Communications Type A Block 05 Data Register 1 (DCA05DR1, Address = Bank 0, 35h)
Digital Communications Type A Block 05 Data Register 2 (DCA05DR2, Address = Bank 0, 36h)
Digital Communications Type A Block 06 Data Register 0 (DCA06DR0, Address = Bank 0, 38h)
Digital Communications Type A Block 06 Data Register 1 (DCA06DR1, Address = Bank 0, 39h)

9.3.5 Digital Communications Type A Block xx Control Register 0 When Used as UART Receiver

Table 57: Digital Communications Type A Block xx Control Register 0...

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	RW	RW	RW
Bit Name	Parity Error	Overrun	Framing Error	RX Active	RX Reg Full	Parity Type	Parity Enable	Enable

Bit 7: **Parity Error**
0 = Indicates no parity error detected in the last byte received
1 = Indicates a parity error detected in the last byte received
Reset when this register is read

Bit 6: **Overrun**
0 = Indicates that no overrun has taken place
1 = Indicates the RX Data register was overwritten with a new byte before the previous one had been read
Reset when this register is read

Bit 5: **Framing Error**
0 = Indicates correct stop bit
1 = Indicates a missing STOP bit
Reset when this register is read

Bit 4: **RX Active**
0 = Indicates no communication currently in progress
1 = Indicates a start bit has been received and a byte is currently being received

Bit 3: **RX Reg Full**
0 = Indicates the RX Data register is empty
1 = Indicates a byte has been loaded into the RX Data register
Interrupt source for RXUART. Reset when the RX Data register is read (Data Register 2)

Bit 2: **Parity Type**
0 = Even
1 = Odd

Bit 1: **Parity Enable**
0 = Parity Disabled
1 = Parity Enabled

Bit 0: **Enable**
0 = Function Disabled
1 = Function Enabled

Digital Communications Type A Block 04 Control Register 0 (DCA04CR0, Address = Bank 0, 33h)
Digital Communications Type A Block 05 Control Register 0 (DCA05CR0, Address = Bank 0, 37h)
Digital Communications Type A Block 06 Control Register 0 (DCA06CR0, Address = Bank 0, 3Bh)
Digital Communications Type A Block 07 Control Register 0 (DCA07CR0, Address = Bank 0, 3Fh)

2. Enabling

   The data input to the Dead-Band function is hardware to the primary output of the previous block, which is typically programmed to be a PWM. The proper order for enabling these blocks (writing the Control Register 0) is PWM first, then Dead-Band.

3. Disabled State

   When the Control Register Enable bit is set to '0', the internal block clock is turned off. A write to Data Register 1 (Period) is loaded directly into Data Register 0 (Counter) to initialize or reset the dead-band time. All outputs are low and the block interrupt is held low.

4. Asserting the Kill Signal

   When the Kill signal is asserted high, both outputs FO and F1 are held low. When the Kill signal is selected from an external source through a Global Input, it is synchronized to the 24 MHz clock and therefore has up to 42 ns of latency.

5. Negating the Kill Signal

   The Kill signal may be negated at any time. However, the output may be enabled at an arbitrary time with respect to the F0 and F1 generation. If exact timing is required when re-enabling the F0 and F1 outputs, the following procedure is recommended:

   1.Kill is asserted.

   2.Write to Control Register 0 to disable the block.

   3.Write to Data Register 1 (Deadband time) to initialize the period.

   4.Kill is eventually negated.

   5.Write to Control Register 0 to enable the block.

9.5.4 PRS - Pseudo-Random Sequence Generator

9.5.4.1 Summary

The PRS function generates an output waveform corresponding to a sequence of pseudo-random numbers. A linear-feedback shift register generates the sequence according to a user-specified polynomial. The width of the numbers in the sequence is variable and the initial value is determined by a user-defined "seed" value. PRS PSoC blocks can be chained to increase the width of the numbers and, hence, the length of the sequence. A chain of N PSoC blocks can generate numbers from 2- to 8N-bits wide and sequences of up to 2^{8N}-1 distinct values.

9.5.4.2 Registers

Data Register 0 implements a linear-feedback shift register. Data Register 2 holds the "seed" value and when the block is disabled, a write to Data Register 2 is loaded directly into Data Register 0 (The block must be disabled when writing this value). Data Register 1 specifies the polynomial and width of the numbers in the sequence (see 9.5.4.6).

9.5.4.3 Inputs

The clock input determines the rate at which the output sequence is produced. The data input must be set to low for the block to function as a PRS. The multiplexer for selecting these inputs is controlled by the PSoC block Input Register (DBA00IN-DCA07IN).

9.5.4.4 Outputs

The PRS function drives the output serial data stream synchronous with the input clock. The output bits change on the rising edge of the input clock. The output may be driven on the Global Output bus or to the subsequent digital PSoC block. The PSoC block Output Register (DBA00OU-DCA07OU) controls output options.

9.5.4.5 Interrupts

The PRS function provides an interrupt based on the Compare signal between Data Register 0 and Data Register 2. Data Register 2 is initially loaded with the "seed" value, and therefore a periodic interrupt will be generated when the PRS count matches the seed value.

Table 62: AGND, RefHI, RefLO Operating Parameters

	AGND		RefHI		RefLO		Notes
	Source	**Voltage**	**Source**	**Voltage**	**Source**	**Voltage**	
000	$V_{cc}/2$	2.5 V 1.65 V	V_{cc}+Vbg	3.8 V 2.95 V	V_{cc}-Vbg	1.2 V 0.35 V	5.0 V System 3.3 V System
001	P2[4]	2.2 V[1]	P2[4]+P2[6]	3.2 V[1]	P2[4]-P2[6]	1.2 V[1]	User Adjustable
010	Vcc/2	2.5 V 1.65 V	Vcc	5.0 V 3.3 V	Vss	0.0 V 0.0 V	5.0 V System 3.3 V System
011	2*Vbg	2.6 V	2*Vbg+Vbg	3.9 V	2*Vbg-Vbg	1.3 V	Not for 3.3 V Systems
100	2*Vbg	2.6 V	2*Vbg+P2[6]	3.6 V[1]	2*Vbg-P2[6]	1.6 V[1]	Not for 3.3 V Systems
101	P2[4]	2.2 V[1]	P2[4]+Vbg	3.5 V[1]	P2[4]-Vbg	0.9 V[1]	User Adjustable
110	Reserved						
111	Reserved						

1. Example shown for AGND P2[4] = 2.2 V and Ref P2[6] = 1.0 V

10.4.4 Analog Array Power Control

PWR Sets Analog Array Power Control. Analog array power is controlled through the bias circuits in the Continuous Time blocks and separate bias circuits in the Switched Capacitor blocks. Continuous Time blocks (ACAxx) can be operated to make low power comparators independent of Switched Capacitor (ASAxx and ASBxx) blocks, without their power consumption.

The reference array supplies voltage to all blocks and current to the Switched Capacitor blocks. At higher block clock rates, there is increased reference current demand; the reference power should be set equal to the highest power level of the analog blocks used.

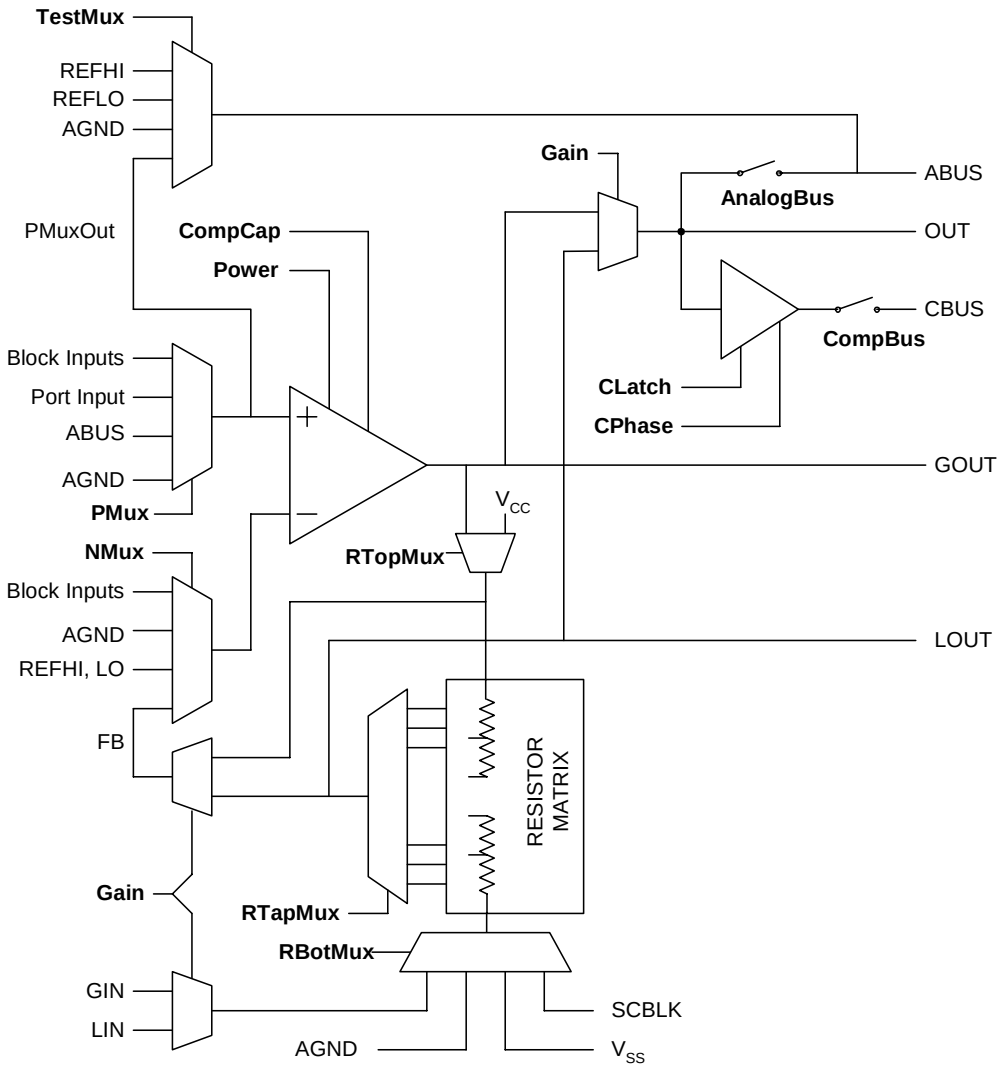

Figure 21: Analog Continuous Time PSoC Blocks

10.7.2 Registers

10.7.2.1 Analog Continuous Time Block xx Control 0 Register

The RTopMux and RBotMux bits control the connection of the two ends of the resistor string. The RTopMux bit controls the top end of the resistor string, which can either be connected to Vcc or to the op-amp output. The RBotMux bits control the connection of the bottom end of the resistor string.

The RTapMux bits control the center tap of the resistor string. Note that only relative weighting of units is given in the table.

The Gain and Loss columns correspond to the gain or loss obtained if the RTopMux and Gain bits are set so that the overall amplifier provides gain or loss.

The Gain bit controls whether the resistor string is connected around the op-amp as for gain (center tap to

10.9.2.2 Analog Switch Cap Type B Block xx Control 1 Register

AMux controls the input muxing for the A capacitor branch.

The BCap bits set the value of the capacitor in the B path.

Table 74: Analog Switch Cap Type B Block xx Control 1 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	AMux[2]	AMux[1]	AMux[0]	BCap[4]	BCap[3]	BCap[2]	BCap[1]	BCap[0]

Bit [7:5]: **AMux [2:0]** Input muxing select for A capacitor branch. (Note that available mux inputs vary by individual PSoC block.)

ASB11	ASB13	ASB20	ASB22
0 0 0 = ACA01	ACA03	ASA10	ASA12
0 0 1 = ASA12	P2.2	P2.1	ASA21
0 1 0 = ASA10	ASA12	ASA21	ASA23
0 1 1 = ASA21	ASA23	ABUS0	ABUS2
1 0 0 = REFHI	REFHI	REFHI	REFHI
1 0 1 = ACA00	ACA02	ASB11	ASB13
1 1 0 = Reserved	Reserved	Reserved	Reserved
1 1 1 = Reserved	Reserved	Reserved	Reserved

Bit [4:0]: BCap [4:0] Binary encoding for 32 possible capacitor sizes for B Capacitor:

0 0 0 0 0 = 0 Capacitor units in array	1 0 0 0 0 = 16 Capacitor units in array
0 0 0 0 1 = 1 Capacitor units in array	1 0 0 0 1 = 17 Capacitor units in array
0 0 0 1 0 = 2 Capacitor units in array	1 0 0 1 0 = 18 Capacitor units in array
0 0 0 1 1 = 3 Capacitor units in array	1 0 0 1 1 = 19 Capacitor units in array
0 0 1 0 0 = 4 Capacitor units in array	1 0 1 0 0 = 20 Capacitor units in array
0 0 1 0 1 = 5 Capacitor units in array	1 0 1 0 1 = 21 Capacitor units in array
0 0 1 1 0 = 6 Capacitor units in array	1 0 1 1 0 = 22 Capacitor units in array
0 0 1 1 1 = 7 Capacitor units in array	1 0 1 1 1 = 23 Capacitor units in array
0 1 0 0 0 = 8 Capacitor units in array	1 1 0 0 0 = 24 Capacitor units in array
0 1 0 0 1 = 9 Capacitor units in array	1 1 0 0 1 = 25 Capacitor units in array
0 1 0 1 0 = 10 Capacitor units in array	1 1 0 1 0 = 26 Capacitor units in array
0 1 0 1 1 = 11 Capacitor units in array	1 1 0 1 1 = 27 Capacitor units in array
0 1 1 0 0 = 12 Capacitor units in array	1 1 1 0 0 = 28 Capacitor units in array
0 1 1 0 1 = 13 Capacitor units in array	1 1 1 0 1 = 29 Capacitor units in array
0 1 1 1 0 = 14 Capacitor units in array	1 1 1 1 0 = 30 Capacitor units in array
0 1 1 1 1 = 15 Capacitor units in array	1 1 1 1 1 = 31 Capacitor units in array

Analog Switch Cap Type B Block 11 Control 1 Register (ASB11CR1, Address = Bank 0/1, 85h)
Analog Switch Cap Type B Block 13 Control 1 Register (ASB13CR1, Address = Bank 0/1, 8Dh)
Analog Switch Cap Type B Block 20 Control 1 Register (ASB20CR1, Address = Bank 0/1, 91h)
Analog Switch Cap Type B Block 22 Control 1 Register (ASB22CR1, Address = Bank 0/1, 99h)

10.9.2.4 Analog Switch Cap Type B Block xx Control 3 Register

ARefMux selects the reference input of the A capacitor branch.

FSW1 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to the integrating cap. The state of the switch is affected by the state of the AutoZero bit in Control 2 Register (ASB11CR2, ASB13CR2, ASB20CR2, ASB22CR2). If the FSW1 bit is set to 0, the switch is always disabled. If the FSW1 bit is set to 1, the AutoZero bit determines the state of the switch. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high.

FSW0 is used to control a switch in the integrator capacitor path. It connects the output of the op-amp to analog ground.

BSW is used to control switching in the B branch. If disabled, the B capacitor branch is a continuous time branch like the C branch of the SC A Block. If enabled, then on internal PHI1, both ends of the cap are switched to analog ground. On internal PHI2, one end is switched to the B input and the other end is switched to the summing node.

BMuxSCB controls muxing to the input of the B capacitor branch. The B branch can be switched or unswitched.

Table 76: Analog Switch Cap Type B Block xx Control 3 Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	ARefMux[1]	ARefMux[0]	FSW[1]	FSW[0]	BSW	BMuxSCB	Power[1]	Power[0]

Bit [7:6]: **ARefMux [1:0]** Encoding for selecting reference input
0 0 = Analog ground is selected
0 1 = REFHI input selected (This is usually the high reference)
1 0 = REFLO input selected (This is usually the low reference)
1 1 = Reference selection is driven by the comparator (When output comparator node is set high, the input is set to REFHI. When set low, the input is set to REFLO)

Bit 5: **FSW1** Bit for controlling gated switches
0 = Switch is disabled
FSW1 bit is set to 1; the state of the switch is determined by the AutoZero bit. If the AutoZero bit is 0, the switch is enabled at all times. If the AutoZero bit is 1, the switch is enabled only when the internal PHI2 is high

Bit 4: **FSW0** Bits for controlling gated switches
0 = Switch is disabled
1 = Switch is enabled when PHI1 is high

Bit 3: **BSW** Enable switching in branch
0 = B branch is a continuous time path
1 = B branch is switched with internal PHI2 sampling

Bit 2: **BMuxSCB** Encoding for selecting B inputs. (Note that the available mux inputs vary by individual PSoC block)
ASB11 ASB13 ASB20 ASB22
0 = ACA00 ACA02 ASB11 ASB13
1 = ACA01 ACA03 ASA10 ASA12

Bit [1:0]: **Power [1:0]** Encoding for selecting 1 of 4 power levels
0 0 = Off
0 1 = 10 µA, typical
1 0 = 50 µA, typical
1 1 = 200 µA, typical

Analog Switch Cap Type B Block 11 Control 3 Register (ASB11CR3, Address = Bank 0/1, 87h)
Analog Switch Cap Type B Block 13 Control 3 Register (ASB13CR3, Address = Bank 0/1, 8Fh)
Analog Switch Cap Type B Block 20 Control 3 Register (ASB20CR3, Address = Bank 0/1, 93h)
Analog Switch Cap Type B Block 22 Control 3 Register (ASB22CR3, Address = Bank 0/1, 9Bh)

10.12.4 Analog Output Buffer Control Register

Table 81: Analog Output Buffer Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	W	W	W	W	W	W	--	W
Bit Name	ACol1Mux	ACol2Mux	ABUF1EN	ABUF2EN	ABUF0EN	ABUF3EN	Reserved	PWR

Bit 7: **ACol1Mux**
0 = Set column 1 input to column 1 input mux output
1 = Set column 1 input to column 0 input mux output

Bit 6: **ACol2Mux**
0 = Set column 2 input to column 2 input mux output
1 = Set column 2 input to column 3 input mux output

Bit 5: **ABUF1EN** Enables the analog output buffer for Analog Column 1 (Pin P0[5])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 4: **ABUF2EN** Enables the analog output buffer for Analog Column 2 (Pin P0[4])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 3: **ABUF0EN** Enables the analog output buffer for Analog Column 0 (Pin P0[3])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit 2: **ABUF3EN** Enables the analog output buffer for Analog Column 3 (Pin P0[2])
0 = Disable analog output buffer
1 = Enable analog output buffer

Bit [1]: **Reserved** Must be left as 0

Bit [0]: **PWR** Determines power level of all output buffers
0 = Low output power
1 = High output power

Analog Output Buffer Control Register (ABF_CR, Address = Bank 1, 62h)

10.13 Analog Modulator

The user has the capability to use the Analog Switch Cap Type A PSoC Blocks in Columns 0 and 2 as amplitude modulators. The Analog Modulator Control Register (AMD_CR) allows the user to select the appropriate modulating signal. When the modulating signal is low, the polarity follows the setting of the ASign bit set in the Analog Switch Cap Type A Control 0 Register (ASAxxCR0). When this signal is high, the normal gain polarity of the PSoC block is inverted.

This filter is implemented using a combination of hardware and software resources. Hardware is used to accumulate the high-speed in-coming data while the software is used to process the lower speed, enhanced resolution data for output.

Table 91: Decimator/Incremental Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	IGEN [3]	IGEN [2]	IGEN [1]	IGEN [0]	ICCKSEL	DCol [1]	DCol [0]	DCLKSEL

Bit [7:4]: **IGEN [3:0]** Individual enables for each analog column that gates the Analog Comparator based on the ICCKSEL input (Bit 3)

Bit 3: **ICCKSEL** Clock select for Incremental gate function
0 = Digital Basic Type A Block 02
1 = Digital Communications Type A Block 06

Bit [2:1]: **DCol [1:0]** Selects Analog Column Comparator source
0 0 = Analog Column Comparator 0
0 1 = Analog Column Comparator 1
1 0 = Analog Column Comparator 2
1 1 = Analog Column Comparator 3

Bit 0: **DCLKSEL** Clock select for Decimator latch
0 = Digital Basic Type A Block 02
1 = Digital Communications Type A Block 06

Decimator Incremental Register (DEC_CR, Address = Bank 0, E6h)

Table 92: Decimator Data High Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the high order byte within the 16-bit decimator data registers
Any 8-bit data value when written will cause both the Decimator Data High (DEC_DH) and Decimator Data Low (DEC_DL) registers to be cleared

Decimator High Register (DEC_DH / DEC_CL, Address = Bank 0, E4h)

Table 93: Decimator Data Low Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Bit Name	Data [7]	Data [6]	Data [5]	Data [4]	Data [3]	Data [2]	Data [1]	Data [0]

Bit [7:0]: **Data [7:0]**
8-bit data value when read is the low order byte within the 16 bit decimator data registers

Decimator Data Low Register (DEC_DL, Address = Bank 0, E5h)

11.6 Switch Mode Pump

This feature is available on the CY8C26xxx versions within this family. During the time Vcc is ramping from 0 Volts to POR V_{trip} (2.2V +/- 12%), IC operation is held off by the POR circuit and the Switch Mode Pump is enabled. The pump is realized by connecting an external inductor between the battery voltage and SMP, with an external diode pointing from SMP to the V_{cc} pin (which must have a bypass capacitance of at least 0.1uF connected to V_{cc}). This circuitry will pump Vcc to the Switch Mode Pump value specified in the Voltage Monitor Control Register (VLT_CR), shown above. Battery voltage values down to 0.9 V during operation are supported, but this circuitry is not guaranteed to start for battery voltages below 1.2 V. Once the IC is enabled after its power up and boot sequence, firmware can disable the SMP function by writing Voltage Monitor Control Register (VLT_CR) bit 7 to a 1.

When the IC is put into sleep mode, the power supply pump will remain running to maintain voltage. This may result in higher than specification sleep current depending upon application. If the user desires, the pump may be disabled during precision measurements (such as A/D conversions) and then re-enabled (writing B7 to 1 and then back to 0 again). The user, however, is responsible for making the operation happen quickly enough to guarantee supply holdup (by the bypass capacitor) sufficient for continued operation.

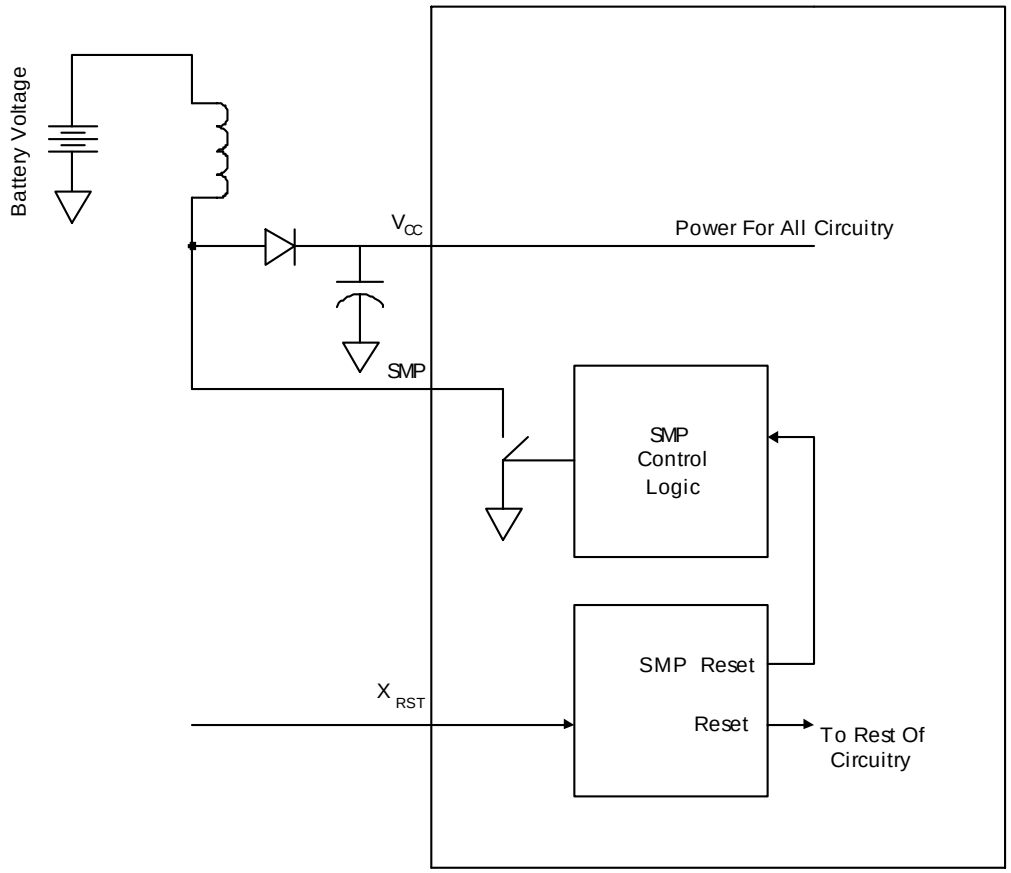

Figure 33: Switch Mode Pump

11.8.1 Additional Function for Table Read Supervisory Call

The Table Read supervisory operation will return the Version ID in the Accumulator. The value in the Accumulator is divided into a high and low nibble, indicating major and minor revisions, respectively. **Note**: The value in the X register is modified during the Table Read Supervisory Call, and must be saved and restored if needed after the call completes.

- A[7:4]: Major silicon revisions.
- A[3:0]: Minor silicon revisions.

Table 99: Table Read for Supervisory Call Functions

Table ID	Function	TV(0)	TV(1)	TV(2)	TV(3)	TV(4)	TV(5)	TV(6)	TV(7)
00[1]	Production Silicon ID	Silicon ID 1	Silicon ID 0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
01	Provides trim value for Internal Main Oscillator and Internal Voltage Reference	Internal Voltage Reference trim value for 3.3V	Internal Main Oscillator trim value for 3.3V	Reserved	Reserved	Internal Voltage Reference trim value for 5.0V	Internal Main Oscillator trim value for 5.0V	Reserved	Reserved

1. Determines silicon revision values in Accumulator and X registers.

11.9 Flash Program Memory Protection

The user has the option to define the access to the Flash memory. A flexible system allows the user to select one of four protection modes for each 64-byte block within the Flash, based on the particular application. The protection mechanism is implemented by a device programmer using the System Supervisor Call. When this command is executed, two bits within the data programmed into the Flash will select the protection mode. It is not intended that the protection byte will be modified by the user's code. The following table lists the available protection options:

Table 100: Flash Program Memory Protection

Mode Bits	Mode Name	External Read	External Write	Internal Write
00	Unprotected	Enabled	Enabled	Enabled
01	Factory Upgrade	Disabled	Enabled	Enabled
10	Field Upgrade	Disabled	Disabled	Enabled
11	Full Protection	Disabled	Disabled	Disabled

Note: Mode 10 is the default.

11.10 Programming Requirements and Step Descriptions

The pins in the following table are critical for the programmer:

Table 101: Programmer Requirements

Pin Name	Function	Programmer HW Pin Requirements
SDATA	Serial Data In/Out	Drive TTL Levels, Read TTL, High Z
SCLK	Serial Clock	Drive TTL levEl Clock Signal
V_{ss}	Power Supply Ground Connection	Low Resistance Ground Connection
V_{cc}	Power Supply Positive Voltage	0V, 3.0V, 5V, & 5.4V. 0.1V Accuracy. 20mA Current Capability

12.0 Development Tools

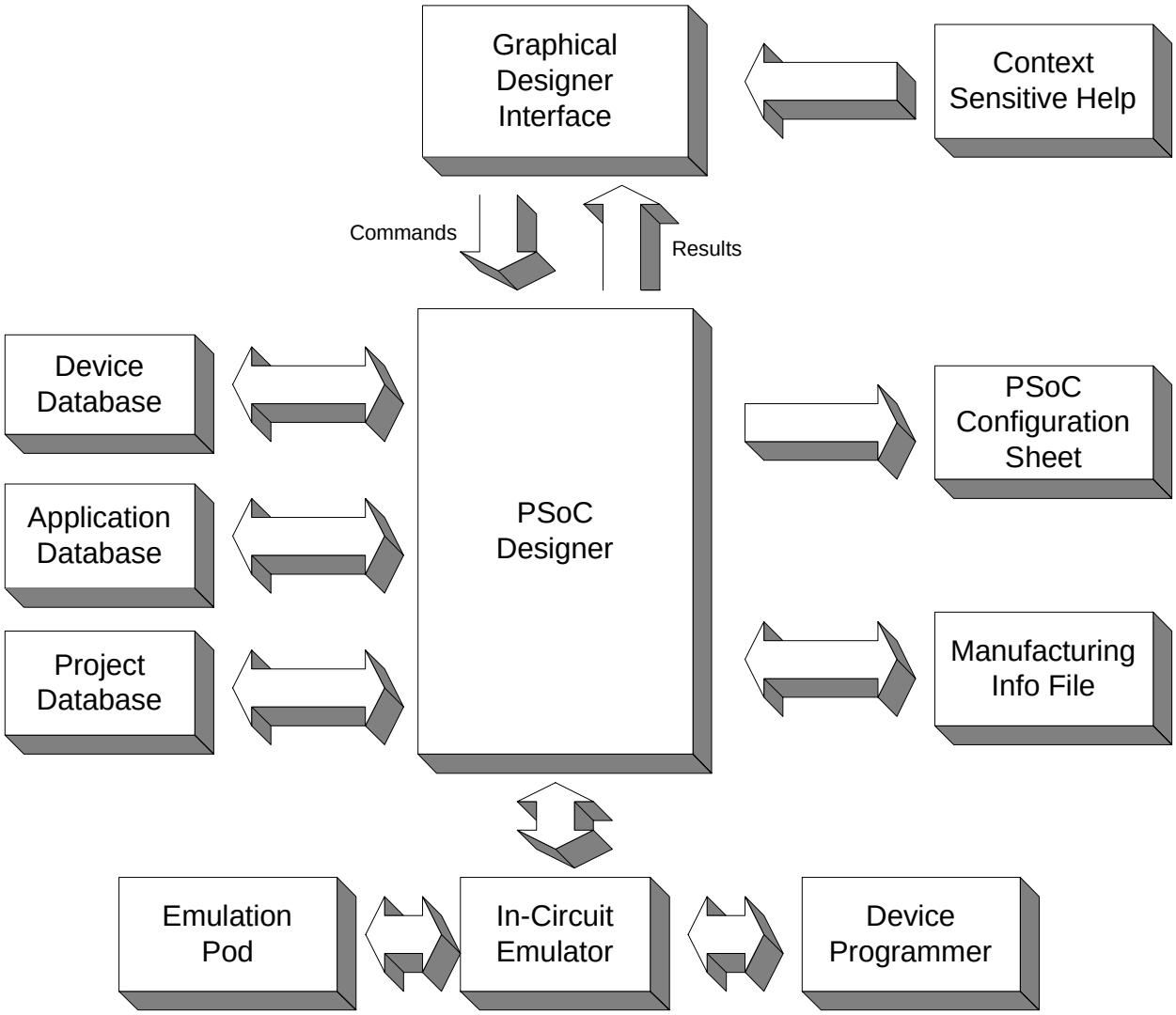

Figure 35: PSoC Designer Functional Flow

12.1 Overview

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP.

PSoC Designer helps the customer to select an operating configuration for the microcontroller, write application code that uses the microcontroller, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

13.2.1.2 3.3V Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 3.3V +/- 10% and -40°C <= T_A <= 85°C. The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switch Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only. For 5V operation, see Table 105 on page 130.

Table 106: 3.3V DC Operational Amplifier Specifications

Symbol	3.3V DC Operational Amplifier Specifications	Minimum	Typical	Maximum	Unit
	Input Offset Voltage (Absolute Value)	-	7	30	mV
	Average Input Offset Voltage Drift	-	+24	-	µV/°C
	Input Leakage Current[1]	-	2	700	nA
	Input Capacitance[2]	.32	.36	.42	pF
	Common Mode Voltage Range[3]	.5	-	V_{cc} - 1.0	VDC
	Common Mode Rejection Ratio	80	-	-	dB
	Open Loop Gain	80	-	-	dB
	High Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 V_{cc} - .4 V_{cc} - .4 V_{cc} - .4	 - - -	 - - -	 V V V
	Low Output Voltage Swing (Worst Case Internal Load) Bias = Low Bias = Medium Bias = High	 - - -	 - - -	 0.1 0.1 0.1	 V V V
	Supply Current (Including Associated AGND Buffer) Bias = Low Bias = Medium Bias = High	 - - -	 80 112 320	 200 300 800	 µA µA µA
	Supply Voltage Rejection Ratio	60	-	-	dB

1. The leakage current includes the Analog Continuous Time PSoC block mux and the analog input mux. The leakage related to the General Purpose I/O pins is not included here.
2. The Input Capacitance includes the Analog Continuous Time PSoC block mux and the analog input mux. The capacitance of the General Purpose I/O pins is not included here.
3. The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer

13.2.6 DC Analog Reference Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and -40°C <= TA <= 85°C. The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The bias levels for AGND refer to the bias of the Analog Continuous Time PSoC block. The bias levels for RefHi and RefLo refer to the Analog Reference Control Register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25C and are for design guidance only. (3.3V replaces 5V for the 3.3V DC Analog Reference Specifications.)

Table 112: 5V DC Analog Reference Specifications

Symbol	5V DC Analog Reference Specifications	Minimum	Typical	Maximum	Unit
	AGND = Vcc/2[1] CT Block Bias = High	V_{cc}/2 - 0.010	V_{cc}/2 - 0.004	V_{cc}/2 + 0.003	V
	AGND = 2*BandGap[1] CT Block Bias = High	2*BG - 0.043	2*BG - 0.010	2*BG + 0.024	V
	AGND = P2[4] (P2[4] = Vcc/2)[1] CT Block Bias = High	P24 - 0.013	P24 0.001	P24 + 0.014	V
	AGND Column to Column Variation (AGND=Vcc/2)[1] CT Block Bias = High	-0.034	0.000	0.034	mV
	REFHI = Vcc/2 + BandGap Ref Control Bias = High	V_{cc}/2+BG - 0.140	V_{cc}/2+BG - 0.018	V_{cc}/2+BG + 0.103	V
	REFHI = 3*BandGap Ref Control Bias = High	3*BG - 0.112	3*BG - 0.018	3*BG + 0.076	V
	REFHI = 2*BandGap + P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG+P2[6] - 0.113	2*BG+P2[6] - 0.018	2*BG+P2[6]+ 0.077	V
	REFHI = P2[4] + BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]+BG - 0.130	P2[4]+BG - 0.016	P2[4]+BG + 0.098	V
	REFHI = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]+P2[6] - 0.133	P2[4]+P2[6] - 0.016	P2[4]+P2[6]+ 0.100	V
	REFLO = Vcc/2 – BandGap Ref Control Bias = High	V_{cc}/2-BG - 0.051	V_{cc}/2-BG + 0.024	V_{cc}/2-BG + 0.098	V
	REFLO = BandGap Ref Control Bias = High	BG - 0.082	BG + 0.023	BG + 0.129	V
	REFLO = 2*BandGap - P2[6] (P2[6] = 1.3V) Ref Control Bias = High	2*BG-P2[6] - 0.084	2*BG-P2[6] + 0.025	2*BG-P2[6] + 0.134	V
	REFLO = P2[4] – BandGap (P2[4] = Vcc/2) Ref Control Bias = High	P2[4]-BG - 0.056	P2[4]-BG + 0.026	P2[4]-BG + 0.107	V
	REFLO = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V) Ref Control Bias = High	P2[4]-P2[6] - 0.057	P24-P26 + 0.026	P2[4]-P2[6] + 0.110	V

13.3.2 AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges, 5V +/- 5% and –40°C <= T_A <= 85°C. Typical parameters are provided for design guidance only. Typical parameters apply to 5V and 25°C. For 3.3V operation, see Table 120 on page 142.

Table 119: 5V AC Analog Output Buffer Specifications

Symbol	5V AC Analog Output Buffer Specifications	Minimum	Typical	Maximum	Unit
	Rising Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.5	µs
	Bias = High	-	-	2.5	µs
	Falling Settling Time to 0.1%, 1V Step, 100pF Load				
	Bias = Low	-	-	2.2	µs
	Bias = High	-	-	2.2	µs
	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load				
	Bias = Low	.9	-	-	V/µs
	Bias = High	.9	-	-	V/µs
	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load				
	Bias = Low	.9	-	-	V/µs
	Bias = High	.9	-	-	V/µs
	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load				
	Bias = Low	1.5	-	-	MHz
	Bias = High	1.5	-	-	MHz
	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load				
	Bias = Low	600	-	-	kHz
	Bias = High	600	-	-	kHz