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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0113hj005sg">https://www.e-xfl.com/product-detail/zilog/z8f0113hj005sg</a>

Table 34.	LED Drive Level Low Register (LEDLVLL) . . . . .	53
Table 35.	Trap and Interrupt Vectors in Order of Priority . . . . .	55
Table 36.	Interrupt Request 0 Register (IRQ0) . . . . .	59
Table 37.	Interrupt Request 1 Register (IRQ1) . . . . .	60
Table 38.	Interrupt Request 2 Register (IRQ2) . . . . .	61
Table 39.	IRQ0 Enable and Priority Encoding . . . . .	61
Table 40.	IRQ0 Enable High Bit Register (IRQ0ENH) . . . . .	62
Table 41.	IRQ0 Enable Low Bit Register (IRQ0ENL) . . . . .	62
Table 42.	IRQ1 Enable and Priority Encoding . . . . .	63
Table 43.	IRQ1 Enable Low Bit Register (IRQ1ENL) . . . . .	64
Table 44.	IRQ1 Enable High Bit Register (IRQ1ENH) . . . . .	64
Table 45.	IRQ2 Enable and Priority Encoding . . . . .	65
Table 46.	IRQ2 Enable High Bit Register (IRQ2ENH) . . . . .	65
Table 47.	IRQ2 Enable Low Bit Register (IRQ2ENL) . . . . .	66
Table 48.	Interrupt Edge Select Register (IRQES) . . . . .	66
Table 49.	Shared Interrupt Select Register (IRQSS) . . . . .	67
Table 50.	Interrupt Control Register (IRQCTL) . . . . .	68
Table 51.	Timer 0–1 High Byte Register (TxH) . . . . .	84
Table 52.	Timer 0–1 Low Byte Register (TxL) . . . . .	84
Table 53.	Timer 0–1 Reload High Byte Register (TxRH) . . . . .	85
Table 54.	Timer 0–1 Reload Low Byte Register (TxRL) . . . . .	85
Table 55.	Timer 0–1 PWM High Byte Register (TxPWMH) . . . . .	86
Table 56.	Timer 0–1 PWM Low Byte Register (TxPWML) . . . . .	86
Table 57.	Timer 0–1 Control Register 0 (TxCTL0) . . . . .	87
Table 58.	Timer 0–1 Control Register 1 (TxCTL1) . . . . .	88
Table 59.	Watchdog Timer Approximate Time-Out Delays . . . . .	91
Table 60.	Watchdog Timer Control Register (WDTCTL) . . . . .	94
Table 61.	Watchdog Timer Reload Upper Byte Register (WDTU) . . . . .	95
Table 62.	Watchdog Timer Reload High Byte Register (WDTH) . . . . .	95
Table 63.	Watchdog Timer Reload Low Byte Register (WDTL) . . . . .	95
Table 64.	UART Transmit Data Register (U0TXD) . . . . .	109
Table 65.	UART Receive Data Register (U0RXD) . . . . .	109
Table 66.	UART Status 0 Register (U0STAT0) . . . . .	110
Table 67.	UART Status 1 Register (U0STAT1) . . . . .	111
Table 68.	UART Control 0 Register (U0CTL0) . . . . .	112
Table 69.	UART Control 1 Register (U0CTL1) . . . . .	113

# Pin Description

Z8 Encore! XP F0823 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and pin configurations available for each of the package styles. For information about physical package specifications, see the [Packaging](#) chapter on page 210.

## Available Packages

Table 2 lists the package styles that are available for each device in the F0823 Series product line.

**Table 2. F0823 Series Package Options**

Part Number	ADC	8-pin PDIP	8-pin SOIC	20-pin PDIP	20-pin SOIC	20-pin SSOP	28-pin PDIP	28-pin SOIC	28-pin SSOP	8-pin QFN/MLF-S
Z8F0823	Yes	X	X	X	X	X	X	X	X	X
Z8F0813	No	X	X	X	X	X	X	X	X	X
Z8F0423	Yes	X	X	X	X	X	X	X	X	X
Z8F0413	No	X	X	X	X	X	X	X	X	X
Z8F0223	Yes	X	X	X	X	X	X	X	X	X
Z8F0213	No	X	X	X	X	X	X	X	X	X
Z8F0123	Yes	X	X	X	X	X	X	X	X	X
Z8F0113	No	X	X	X	X	X	X	X	X	X

## Pin Configurations

Figures 2 through 4 display the pin configurations for all packages available in the F0823 Series. For description of signals, see Table 3. The analog input alternate functions (ANAx) are not available on the Z8F0x13 devices. The analog supply pins ( $AV_{DD}$  and  $AV_{SS}$ ) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all pins of Ports A, B, and C default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general-purpose input ports until programmed otherwise.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

Table 17. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B <sup>3</sup>	PB03	Reserved		AFS1[0]: 0
		ANA0	ADC Analog Input	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1	ADC Analog Input	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2	ADC Analog Input	AFS1[2]: 1
	PB3	CLKIN	External Clock Input	AFS1[3]: 0
		ANA3	ADC Analog Input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC Analog Input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		V <sub>REF</sub> <sup>4</sup>	ADC Voltage Reference	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Notes:

1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 automatically enables the associated alternate function.
2. Whether PA0/PA6 take on the timer input or timer output complement function depends on the timer configuration as described in the [Timer Pin Signal Operation](#) section on page 83.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, alternate function selection as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 must also be enabled.
4. V<sub>REF</sub> is available on PB5 in 28-pin products only.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, Alternate Function selection as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 must also be enabled.
6. V<sub>REF</sub> is available on PC2 in 20-pin parts only.



Table 17. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C <sup>4</sup>	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or Comparator Input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or Comparator Input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/V <sub>REF</sub> <sup>6</sup>	ADC Analog Input or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1

Notes:

1. Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 automatically enables the associated alternate function.
2. Whether PA0/PA6 take on the timer input or timer output complement function depends on the timer configuration as described in the [Timer Pin Signal Operation](#) section on page 83.
3. Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, alternate function selection as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 must also be enabled.
4. V<sub>REF</sub> is available on PB5 in 28-pin products only.
5. Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set register AFS2 is implemented but not used to select the function. Also, Alternate Function selection as described in the [Port A–C Alternate Function Subregisters](#) section on page 43 must also be enabled.
6. V<sub>REF</sub> is available on PC2 in 20-pin parts only.

## Direct LED Drive

The Port C pins provide a current sinked output capable of driving an LED without requiring an external resistor. The output sinks current at programmable levels of 3mA, 7mA, 13mA, and 20mA. This mode is enabled through the LED control registers. The LED Drive Enable (LEDEN) register turns on the drivers. The LED Drive Level (LEDLVLH and LEDLVLL) registers select the sink current.

**Table 23. Port A–C Alternate Function Subregisters (PxAF)**

Bit	7	6	5	4	3	2	1	0
Field	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
RESET	00H (Ports A–C); 04H (Port A of 8-pin device)							
R/W	R/W							
Address	If 02H in Port A–C Address Register, accessible through the Port A–C Control Register							

Bit	Description
[7:0] AFx	<b>Port Alternate Function enabled</b> 0 = The port pin is in NORMAL Mode and the DDx bit in the Port A–C Data Direction Subregister determines the direction of the pin. 1 = The alternate function selected through Alternate Function Set subregisters is enabled. Port pin operation is controlled by the alternate function.

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–C Output Control Subregisters

The Port A–C Output Control Subregister (Table 24) is accessed through the Port A–C Control Register by writing 03H to the Port A–C Address Register. Setting the bits in the Port A–C Output Control subregisters to 1 configures the specified port pins for open-drain operation. These subregisters affect the pins directly and, as a result, alternate functions are also affected.

**Table 24. Port A–C Output Control Subregisters (PxOC)**

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–C Address Register, accessible through the Port A–C Control Register							

Bit	Description
[7:0] POCx	<b>Port Output Control</b> These bits function independently of the alternate function bit and always disable the drains if set to 1. 0 = The drains are enabled for any output mode (unless overridden by the alternate function). 1 = The drain of the associated pin is disabled (open-drain mode).

Note: x indicates the specific GPIO port pin number (7–0).

## LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 34). These two bits select between four programmable drive levels. Each pin is individually programmable.

**Table 34. LED Drive Level Low Register (LEDLVLL)**

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

Bit	Description
[7:0]	<b>LED Level High Bit</b>
LEDLVLL	{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA. 01 = 7mA. 10 = 13mA. 11 = 20mA.

# Interrupt Controller

The interrupt controller on the Z8 Encore! XP F0823 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 unique interrupt vectors
  - 12 GPIO port pin interrupt sources (two are shared)
  - 8 on-chip peripheral interrupt sources (two are shared)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the [eZ8 CPU Core User Manual \(UM0128\)](#) available for download at [www.zilog.com](http://www.zilog.com).

## Interrupt Vector Listing

Table 35 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

---

► **Note:** Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

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$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

## **CAPTURE Mode**

In CAPTURE Mode, the current timer count value is recorded when the appropriate external Timer Input transition occurs. The capture count value is written to the Timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the capture occurs on a rising edge or a falling edge of the Timer Input signal. When the capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in TxCTL1 Register is set to indicate the timer interrupt is because of an input capture event.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting. The INPCAP bit in TxCTL1 Register clears indicating the timer interrupt is not because of an input capture event.

Observe the following steps to configure a timer for CAPTURE Mode and initiating the count:

1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for CAPTURE Mode
  - Set the prescale value
  - Set the capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a capture or a reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both

# Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which can place Z8 Encore! XP F0823 Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

## Operation

The WDT is a retriggerable one-shot timer that resets or interrupts F0823 Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT\_AO Flash Option Bit. The WDT\_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable down counter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTM[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 59 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

**Table 59. Watchdog Timer Approximate Time-Out Delays**

WDT Reload Value (Hex)	WDT Reload Value (Decimal)	Approximate Time-Out Delay (with 10kHz typical WDT oscillator frequency)	
		Typical	Description
000004	4	400 μs	Minimum time-out delay
FFFFFF	16,777,215	28 minutes	Maximum time-out delay

- Set or clear the CTSE bit to enable or disable control from the remote receiver using the  $\overline{\text{CTS}}$  pin
6. Check the TDRE bit in the UART Status 0 Register to determine if the Transmit Data Register is empty (indicated by a 1). If empty, continue to [Step 7](#). If the Transmit Data Register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data Register becomes available to receive new data.
  7. Write the UART Control 1 Register to select the outgoing address bit.
  8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
  9. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
  10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR Mode is enabled,.
  11. To transmit additional bytes, return to [Step 5](#).

## Transmitting Data Using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data Register to accept new data for transmission. Observe the following steps to configure the UART for interrupt-driven data transmission:

1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
5. Write to the UART Control 1 Register to enable MULTIPROCESSOR (9-bit) Mode functions, if MULTIPROCESSOR Mode is appropriate.
6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.
7. Write to the UART Control 0 Register to:
  - Set the transmit enable bit (TEN) to enable the UART for data transmission.
  - Enable parity, if appropriate and if MULTIPROCESSOR Mode is not enabled, and select either even or odd parity.

## Receiving IrDA Data

Data received from the infrared transceiver using the IR\_RXD signal through the RXD pin is decoded by the infrared endec and passed to the UART. The UART's baud rate clock is used by the infrared endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 18 displays data reception. When the infrared endec is enabled, the UART's RXD signal is internal to the Z8 Encore! XP F0823 Series products while the IR\_RXD signal is received through the RXD pin.

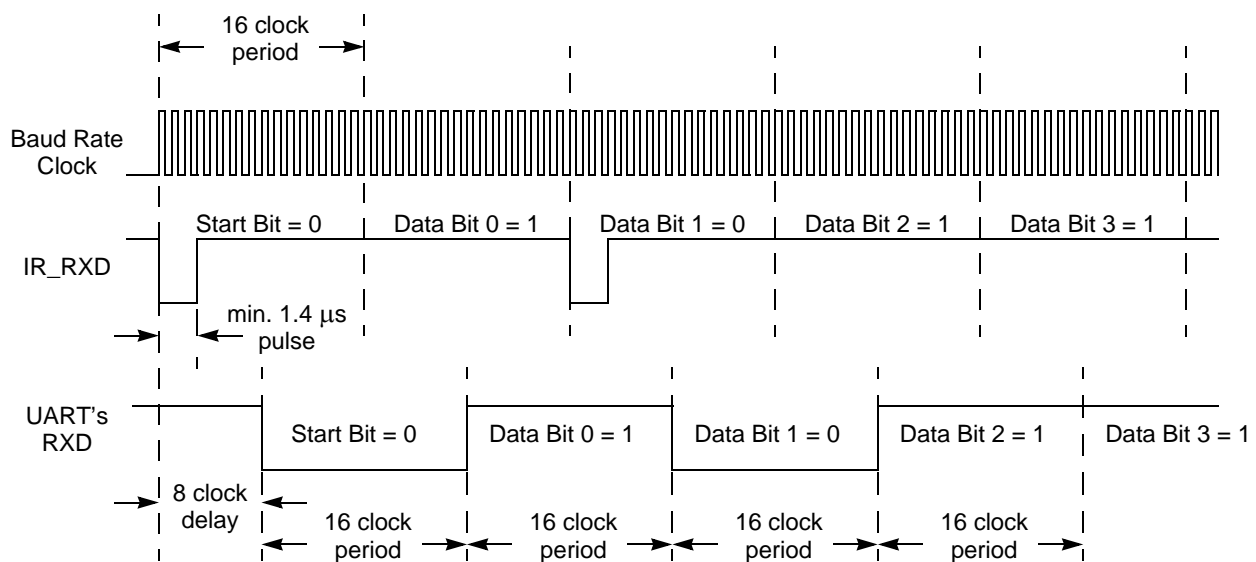


Figure 18. IrDA Data Reception

## Infrared Data Reception

**! Caution:** The system clock frequency must be at least 1.0MHz to ensure proper reception of the 1.4 $\mu$ s minimum width pulses allowed by the IrDA standard.

## Endec Receiver Synchronization

The IrDA receiver uses a local baud rate clock counter (0 to 15 clock periods) to generate an input stream for the UART and to create a sampling window for detection of incoming pulses. The generated UART input (UART RXD) is delayed by 8 baud rate clock periods with respect to the incoming IrDA data stream. When a falling edge in the input data stream is detected, the endec counter is reset. When the count reaches a value of 8, the UART RXD value is updated to reflect the value of the decoded data. When the count reaches 12 baud clock periods, the sampling window for the next incoming pulse opens.



## Comparator Control Register Definition

The Comparator Control Register (CMPCTL) configures the comparator inputs and sets the value of the internal voltage reference.

**Table 78. Comparator Control Register (CMP0)**

Bit	7	6	5	4	3	2	1	0
Field	INPSEL	INNSEL	REFLVL				Reserved	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Bit	Description
[7] INPSEL	<b>Signal Select for Positive Input</b> 0 = GPIO pin used as positive comparator input. 1 = temperature sensor used as positive comparator input.
[6] INNSEL	<b>Signal Select for Negative Input</b> 0 = internal reference disabled, GPIO pin used as negative comparator input. 1 = internal reference enabled as negative comparator input.
[5:2] REFLVL	<b>Internal Reference Voltage Level</b> 0000 = 0.0V. 0001 = 0.2V. 0010 = 0.4V. 0011 = 0.6V. 0100 = 0.8V. 0101 = 1.0V (Default). 0110 = 1.2V. 0111 = 1.4V. 1000 = 1.6V. 1001 = 1.8V. 1010–1111 = Reserved. <b>Note:</b> This reference is independent of the ADC voltage reference.
[1:0]	<b>Reserved</b> These bits are reserved; R/W bits must be programmed to 00 during writes and to 00 when read.

**Figure 20. Flash Memory Arrangement**

## Flash Information Area

The Flash information area is separate from program memory and is mapped to the address range `FE00H` to `FFFFH`. Not all these addresses are accessible. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

## Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

Figure 21 displays a basic Flash Controller flow. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase, and Mass Erase) displayed in Figure 21.

Bit	Description (Continued)
[3] VBO_AO	<b>Voltage Brown-Out Protection Always ON</b> 0 = Voltage Brown-Out Protection can be disabled in STOP Mode to reduce total power consumption. For the block to be disabled, the power control register bit must also be written (see the <a href="#">Power Control Register 0</a> section on page 31). 1 = Voltage Brown-Out Protection is always enabled including during STOP Mode. This setting is the default for unprogrammed (erased) Flash.
[2] FRP	<b>Flash Read Protect</b> 0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger. 1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.
[1]	<b>Reserved</b> This bit is reserved and must be programmed to 1.
[0] FWP	<b>Flash Write Protect</b> This Option Bit provides Flash Program Memory protection: 0 = Programming and erasure disabled for all of Flash Program Memory. Programming, Page Erase, and Mass Erase through User Code is disabled. Mass Erase is available using the On-Chip Debugger. 1 = Programming, Page Erase, and Mass Erase are enabled for all of Flash program memory.

**Table 90. Flash Options Bits at Program Memory Address 0001H**

Bit	7	6	5	4	3	2	1	0
Field	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0001H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

- If the PA2/ $\overline{\text{RESET}}$  pin is held Low while a 32-bit key sequence is issued to the PA0/DBG pin, the DBG feature is unlocked. After releasing PA2/ $\overline{\text{RESET}}$ , it is pulled high. At this point, the PA0/DBG pin can be used to autobaud and cause the device to enter DEBUG Mode. For more details, see the [OCD Unlock Sequence \(8-Pin Devices Only\)](#) section on page 161.

### Exiting DEBUG Mode

The device exits DEBUG Mode following any of these operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset
- Watchdog Timer reset
- Asserting the  $\overline{\text{RESET}}$  pin Low to initiate a Reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a system reset

### OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 Start bit, 8 data bits (least-significant bit first), and 1 Stop bit as displayed in Figure 25.

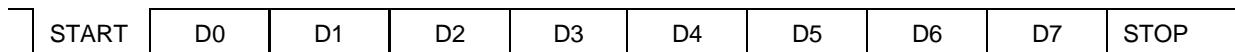


Figure 25. OCD Data Format

► **Note:** When responding to a request for data, the OCD may commence transmitting immediately after receiving the stop bit of an incoming frame. Therefore, when sending the stop bit, the host must not actively drive the DBG pin High for more than 0.5 bit times. Zilog recommends that, if possible, the host drives the DBG pin using an open-drain output.

### OCD Autobaud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the OCD contains an auto-baud detector/generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits Low (one Start bit plus 7 data

bits), framed between High bits. The auto-baud detector measures this period and sets the OCD baud rate generator accordingly.

The auto-baud detector/generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by eight. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by four, but this theoretical maximum is possible only for low noise designs with clean signals. Table 100 lists minimum and recommended maximum baud rates for sample crystal frequencies.

**Table 100. OCD Baud-Rate Limits**

<b>System Clock Frequency (MHz)</b>	<b>Recommended Maximum Baud Rate (kbps)</b>	<b>Recommended Standard PC Baud Rate (bps)</b>	<b>Minimum Baud Rate (kbps)</b>
5.5296	1382.4	691,200	1.08
0.032768 (32kHz)	4.096	2400	0.064

If the OCD receives a Serial Break (nine or more continuous bits Low) the auto-baud detector/generator resets. Reconfigure the auto-baud detector/generator by sending 80H.

## **OCD Serial Errors**

The OCD detects any of the following error conditions on the DBG pin:

- Serial Break (a minimum of nine continuous bits Low)
- Framing Error (received Stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a four character long Serial Break back to the host, and resets the auto-baud detector/generator. A Framing Error or Transmit Collision may be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to the F0823 Series devices or when recovering from an error. A Serial Break from the host resets the auto-baud generator/detector but does not reset the OCD Control Register. A Serial Break leaves the device in DEBUG Mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns High. Because of the open-drain nature of the DBG pin, the host sends a Serial Break to the OCD even if the OCD is transmitting a character.

Table 102. OCD Control Register (OCDCTL)

Bit	7	6	5	4	3	2	1	0
Field	DBGMODE	BRKEN	DBGACK	Reserved				RST
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R	R/W

Bit	Description
[7] DBGMODE	<p><b>DEBUG Mode</b></p> <p>The device enters DEBUG Mode when this bit is 1. When in DEBUG Mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to restart. This bit is automatically set when a BRK instruction is decoded and breakpoints are enabled. If the Flash Read Protect Option Bit is enabled, this bit can only be cleared by resetting the device. It cannot be written to 0.</p> <p>0 = F0823 Series device is operating in NORMAL Mode. 1 = F0823 Series device is in DEBUG Mode.</p>
[6] BRKEN	<p><b>Breakpoint Enable</b></p> <p>This bit controls the behavior of the BRK instruction (opcode 00H). By default, breakpoints are disabled and the BRK instruction behaves similar to an NOP instruction. If this bit is 1, when a BRK instruction is decoded, the DBGMODE bit of the OCDCTL register is automatically set to 1.</p> <p>0 = Breakpoints are disabled. 1 = Breakpoints are enabled.</p>
[5] DBGACK	<p><b>Debug Acknowledge</b></p> <p>This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.</p> <p>0 = Debug Acknowledge is disabled. 1 = Debug Acknowledge is enabled.</p>
[4:1]	<p><b>Reserved</b></p> <p>These bits are reserved and must be 00000 when read.</p>
[0] RST	<p><b>Reset</b></p> <p>Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the OCD is not reset. This bit is automatically cleared to 0 at the end of reset.</p> <p>0 = No effect. 1 = Reset the Flash Read Protect Option Bit device.</p>

**Table 105. Oscillator Control Register (OSCCTL)**

Bit	7	6	5	4	3	2	1	0
Field	INTEN	Reserved	WDTEN	POFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

Bit	Description
[7] INTEN	<b>Internal Precision Oscillator Enable</b> 1 = Internal precision oscillator is enabled. 0 = Internal precision oscillator is disabled.
[6]	<b>Reserved</b> This bit is reserved and must be programmed to 0 during writes and to 0 when read.
[5] WDTEN	<b>Watchdog Timer Oscillator Enable</b> 1 = Watchdog Timer oscillator is enabled. 0 = Watchdog Timer oscillator is disabled.
[4] POFEN	<b>Primary Oscillator Failure Detection Enable</b> 1 = Failure detection and recovery of primary oscillator is enabled. 0 = Failure detection and recovery of primary oscillator is disabled.
[3] WDFEN	<b>Watchdog Timer Oscillator Failure Detection Enable</b> 1 = Failure detection of Watchdog Timer oscillator is enabled. 0 = Failure detection of Watchdog Timer oscillator is disabled.
[2:0] SCKSEL	<b>System Clock Oscillator Select</b> 000 = Internal precision oscillator functions as system clock at 5.53MHz. 001 = Internal precision oscillator functions as system clock at 32kHz. 010 = Reserved. 011 = Watchdog Timer oscillator functions as system clock. 100 = External clock signal on PB3 functions as system clock. 101 = Reserved. 110 = Reserved. 111 = Reserved.

Table 117. Rotate and Shift Instructions (Continued)

Mnemonic	Operands	Instruction
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

## eZ8 CPU Instruction Summary

Table 118 summarizes the eZ8 CPU instruction set. The table identifies the addressing modes employed by the instruction, the effect upon the Flags Register, the number of CPU clock cycles required for the instruction fetch, and the number of CPU clock cycles required for the instruction execution.

Table 118. eZ8 CPU Instruction Summary

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
ADC dst, src	$\text{dst} \leftarrow \text{dst} + \text{src} + \text{C}$	r	r	12	*	*	*	*	0	*	2	3
		r	lr	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	$\text{dst} \leftarrow \text{dst} + \text{src} + \text{C}$	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3

Note: Flags Notation:

\* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.



General Purpose I/O Port Output Timing

Figure 30 and Table 131 provide timing information for GPIO Port pins.

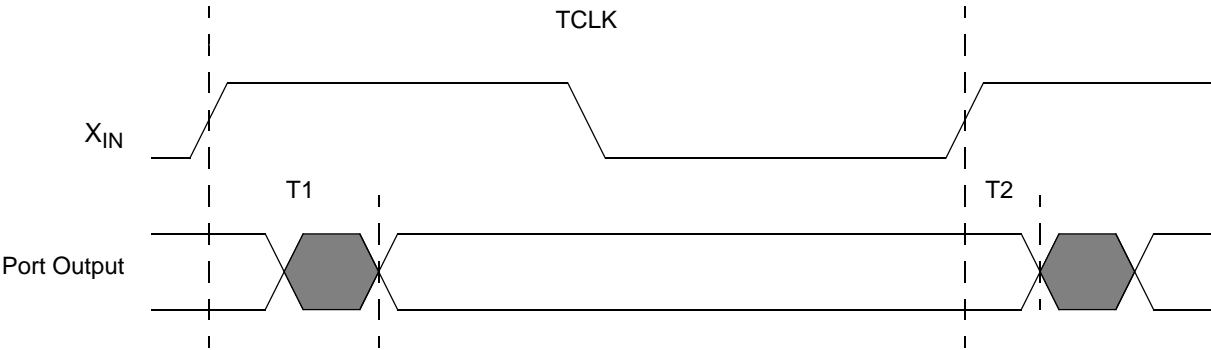


Figure 30. GPIO Port Output Timing

Table 131. GPIO Port Output Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
GPIO Port pins			
T <sub>1</sub>	X <sub>IN</sub> Rise to Port Output Valid Delay	–	15
T <sub>2</sub>	X <sub>IN</sub> Rise to Port Output Hold Time	2	–