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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0113pj005sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Note: *Analog input alternate functions (ANA) are not available on Z8F0x13 devices.

Signal Descriptions

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Table 3 lists the Z8 Encore! XP F0823 Series signals. To determine the signals available for the specific package styles, see the Pin Configurations section on page 7.

Signal Mnemonic	I/O	Description
General-Purpose I/C	O Ports	A–D
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[7:0] ¹	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
UART Controllers		
TXD0	0	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	Ι	Clear To Send. This signal is the flow control input for the UART.
DE	0	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT/T1OUT	0	Timer Output 0–1. These signals are output from the timers.
T0OUT/T1OUT	0	Timer Complement Output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN	Ι	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed T0OUT signals.
Comparator		
CINP/CINN	Ι	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
Notes:		

Table 3. Signal Descriptions

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS} .

2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

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PA0 and PA6 contain two different timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the timer mode. For more details, see the <u>Timers</u> chapter on page 69.

Caution: For pins with multiple alternate functions, Zilog recommends writing to the AFS1 and AFS2 subregisters before enabling the alternate function via the AF Subregister. This prevents spurious transitions through unwanted alternate function modes.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Select Register AFS1	Alternate Function Select Register AFS2
Port A	PA0	TOIN	Timer 0 Input	AFS1[0]: 0	AFS2[0]: 0
		Reserved		AFS1[0]: 0	AFS2[0]: 1
		Reserved		AFS1[0]: 1	AFS2[0]: 0
		T0OUT	Timer 0 Output Complement	AFS1[0]: 1	AFS2[0]: 1
	PA1	T0OUT	Timer 0 Output	AFS1[1]: 0	AFS2[1]: 0
		Reserved		AFS1[1]: 0	AFS2[1]: 1
		CLKIN	External Clock Input	AFS1[1]: 1	AFS2[1]: 0
		Analog Functions*	ADC Analog Input/V _{REF}	AFS1[1]: 1	AFS2[1]: 1
	PA2	DE0	UART 0 Driver Enable	AFS1[2]: 0	AFS2[2]: 0
		RESET	External Reset	AFS1[2]: 0	AFS2[2]: 1
		T1OUT	Timer 1 Output	AFS1[2]: 1	AFS2[2]: 0
		Reserved		AFS1[2]: 1	AFS2[2]: 1
	PA3	CTS0	UART 0 Clear to Send	AFS1[3]: 0	AFS2[3]: 0
		COUT	Comparator Output	AFS1[3]: 0	AFS2[3]: 1
		T1IN	Timer 1 Input	AFS1[3]: 1	AFS2[3]: 0
		Analog Functions*	ADC Analog Input	AFS1[3]: 1	AFS2[3]: 1
	PA4	RXD0	UART 0 Receive Data	AFS1[4]: 0	AFS2[4]: 0
		Reserved		AFS1[4]: 0	AFS2[4]: 1
		Reserved		AFS1[4]: 1	AFS2[4]: 0
		Analog Functions*	ADC/Comparator Input (N)	AFS1[4]: 1	AFS2[4]: 1
	PA5	TXD0	UART 0 Transmit Data	AFS1[5]: 0	AFS2[5]: 0
		T1OUT	Timer 1 Output Complement	AFS1[5]: 0	AFS2[5]: 1
		Reserved		AFS1[5]: 1	AFS2[5]: 0
		Analog Functions*	ADC/Comparator Input (P)	AFS1[5]: 1	AFS2[5]: 1

Table 16. Port Alternate Function Mapping (8-Pin Parts)

Note: *Analog Functions include ADC inputs, ADC reference and comparator inputs. Also, alternate function selection as described in the Port A–C Alternate Function Subregisters section on page 43 must be enabled.



Port A–C Data Direction Subregisters

The Port A–C Data Direction Subregister is accessed through the Port A–C Control Register by writing 01H to the Port A–C Address Register; see Table 22.

Bit	7	6	5	4	3	2	1	0		
Field	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0		
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	lf 01H ir	If 01H in Port A–C Address Register, accessible through the Port A–C Control Register.								

Table 22. Port A–C Data Direction Subregisters (PxDD)

Bit	Description
[7:0]	Data Direction
DDx	 These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting. 0 = Output. Data in the Port A–C Output Data Register is driven onto the port pin. 1 = Input. The port pin is sampled and the value written into the Port A–C Input Data Register. The output driver is tristated.

Note: x indicates the specific GPIO port pin number (7–0).

Port A–C Alternate Function Subregisters

The Port A–C Alternate Function Subregister (Table 23) is accessed through the Port A–C Control Register by writing 02H to the Port A–C Address Register. The Port A–C Alternate Function subregisters enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the the <u>Port A–C Alternate Function Set 1</u> <u>Subregisters</u> section on page 48 and the <u>Port A–C Alternate Function Set 2 Subregisters</u> section on page 49. See the <u>GPIO Alternate Functions</u> section on page 34 to determine the alternate function associated with each port pin.

Caution: Do not enable alternate functions for GPIO port pins for which there is no associated alternate function. Failure to follow this guideline can result in unpredictable operation.

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enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for COUNTER Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer.
 - Configure the timer for COUNTER Mode.
 - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER Mode. After the first timer reload in COUNTER Mode, counting always begins at the reset value of 0001H. In COUNTER Mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control Register to enable the timer.

In COUNTER Mode, the number of timer input transitions since the timer start is computed via the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value – Start Value

COMPARATOR COUNTER Mode

In COMPARATOR COUNTER Mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPAR-ATOR COUNTER Mode, the prescaler is disabled.

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Bit	7	6	5	4	3	2	1	0	
Field		TRH							
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	F02H, F0AH								

Table 53. Timer 0–1 Reload High Byte Register (TxRH)

Table 54. Timer 0–1 Reload Low Byte Register (TxRL)

Bit	7	6	5	4	3	2	1	0		
Field		TRL								
RESET	1	1	1	1	1	1	1	1		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address				F03H,	F0BH					
Bit	Descriptio	n								
[7]										
[6]										
[5]										
[4]										
[3]										
[2]										
[1]										
[0]										

TRH and TRL—Timer Reload Register High and Low

These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit compare value.

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two bits to configure timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input capture event.

Table 57 Timer 0 1 Central Begister 0 (TyCTL 0)

Table 57. Timer 0–1 Control Register 0 (TXCTL0)										
Bit	7	6	5	4	3	2	1	0		
Field	TMODEHI	TICO	NFIG	Reserved		PWMD		INPCAP		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address				F06H,	F0EH					
Bit	Descript	ion								
[7] TMODEHI	Timer M This bit a the timer	Timer Mode High Bit This bit along with the TMODE field in TxCTL1 Register determines the operating mode of the timer. This is the most-significant bit of the Timer mode selection value.								
[6:5] TICONFIG	Timer In This field 0x = Time 10 = Time 11 = Time	 Timer Interrupt Configuration This field configures timer interrupt definition. 0x = Timer Interrupt occurs on all defined reload, compare and input events. 10 = Timer Interrupt only on defined input capture/deassertion events. 11 = Timer Interrupt only on defined reload/compare events. 								
[4]	Reserve This bit is	d s reserved a	and must be	programme	d to 0.					
[3:1] PWMD	PWMD— This field before th $000 = Nc$ $001 = 2c$ $010 = 4c$ $011 = 8c$ $100 = 16$ $101 = 32$ $110 = 64$ $111 = 125$	PWMD—PWM Delay value This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state. 000 = No delay. 001 = 2 cycles delay. 010 = 4 cycles delay. 011 = 8 cycles delay. 100 = 16 cycles delay. 101 = 32 cycles delay. 111 = 128 cycles delay.								
[0] INPCAP	Input Ca This bit ir 0 = Previ 1 = Previ	Input Capture Event This bit indicates if the most recent timer interrupt is caused by a Timer Input capture event. 0 = Previous timer interrupt is not a result of Timer Input capture event. 1 = Previous timer interrupt is a result of Timer Input capture event.								

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.



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Bit **Description (Continued)**

[6] COUNTER Mode

- TPOL If the timer is enabled the Timer Output signal is complemented after timer reload. (cont'd.)
 - 0 =Count occurs on the rising edge of the Timer Input signal.
 - 1 = Count occurs on the falling edge of the Timer Input signal.

PWM SINGLE OUTPUT Mode

- 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload.
- 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.

CAPTURE Mode

- 0 =Count is captured on the rising edge of the Timer Input signal.
- 1 = Count is captured on the falling edge of the Timer Input signal.

COMPARE Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload.

GATED Mode

- 0 = Timer counts when the Timer Input signal is High (1) and interrupts are generated on the falling edge of the Timer Input.
- 1 = Timer counts when the Timer Input signal is Low (0) and interrupts are generated on the rising edge of the Timer Input.

CAPTURE/COMPARE Mode

- 0 = Counting is started on the first rising edge of the Timer Input signal. The current count is captured on subsequent rising edges of the Timer Input signal.
- 1 = Counting is started on the first falling edge of the Timer Input signal. The current count is captured on subsequent falling edges of the Timer Input signal.

PWM DUAL OUTPUT Mode

- 0 = Timer Output is forced Low (0) and Timer Output Complement is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload. When enabled, the Timer Output Complement is forced Low (0) upon PWM count match and forced High (1) upon reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to High (1).
- 1 = Timer Output is forced High (1) and Timer Output Complement is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload. When enabled, the Timer Output Complement is forced High (1) upon PWM count match and forced Low (0) upon reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to Low (0).

CAPTURE RESTART Mode

- 0 = Count is captured on the rising edge of the Timer Input signal.
- 1 = Count is captured on the falling edge of the Timer Input signal.

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scheme is enabled, the UART Address Compare register holds the network address of the device.

MULTIPROCESSOR (9-bit) Mode Receive Interrupts

When MULTIPROCESSOR Mode is enabled, the UART only processes frames addressed to it. The determination of whether a frame of data is addressed to the UART can be made in hardware, software or some combination of the two, depending on the multiprocessor configuration bits. In general, the address compare feature reduces the load on the CPU, because it does not require access to the UART when it receives data directed to other devices on the multi-node network. The following three MULTIPROCESSOR modes are available in hardware:

- Interrupt on all address bytes
- Interrupt on matched address bytes and correctly framed data bytes
- Interrupt only on correctly framed data bytes

These modes are selected with MPMD[1:0] in the UART Control 1 Register. For all multiprocessor modes, bit MPEN of the UART Control 1 Register must be set to 1.

The first scheme is enabled by writing 01b to MPMD[1:0]. In this mode, all incoming address bytes cause an interrupt, while data bytes never cause an interrupt. The interrupt service routine must manually check the address byte that caused triggered the interrupt. If it matches the UART address, the software clears MPMD[0]. Each new incoming byte interrupts the CPU. The software is responsible for determining the end of the frame. It checks for the end-of-frame by reading the MPRX bit of the UART Status 1 Register for each incoming byte. If MPRX=1, a new frame has begun. If the address of this new frame is different from the UART's address, MPMD[0] must be set to 1 causing the UART interrupts to go inactive until the next address byte. If the new frame's address matches the UART's, the data in the new frame is processed as well.

The second scheme requires the following: set MPMD[1:0] to 10B and write the UART's address into the UART Address Compare register. This mode introduces additional hard-ware control, interrupting only on frames that match the UART's address. When an incoming address byte does not match the UART's address, it is ignored. All successive data bytes in this frame are also ignored. When a matching address byte occurs, an interrupt is issued and further interrupts now occur on each successive data byte. When the first data byte in the frame is read, the NEWFRM bit of the UART Status 1 Register is asserted. All successive data bytes have NEWFRM=0. When the next address byte occurs, the hardware compares it to the UART's address. If there is a match, the interrupts continues and the NEWFRM bit is set for the first byte of the new frame. If there is no match, the UART ignores all incoming bytes until the next address match.

The third scheme is enabled by setting MPMD[1:0] to 11b and by writing the UART's address into the UART Address Compare Register. This mode is identical to the second

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Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data Register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data Register before the Transmit shift register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following occurs:

• A data byte is received and is available in the UART Receive Data Register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data Register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

Note: In MULTIPROCESSOR Mode (MPEN = 1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received
- An overrun is detected
- A data framing error is detected

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error

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UART Address Compare Register

The UART Address Compare Register stores the multinode network address of the UART. When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare Register. Receive interrupts and RDA assertions only occur in the event of a match.

Bit	7	6	5	4	3	2	1	0			
Field		COMP_ADDR									
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address			•	F4	5H						

Bit	Description
[7:0]	Compare Address
COMP_ADDR	This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (Table 71 and Table 72) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Bit	7	6	5	4	3	2	1	0	
Field	BRH								
RESET	1	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address		F46H							

Table 71. UART Baud Rate High Byte Register (U0BRH)

Table 72.	UART	Baud	Rate	Low Byte	Register	(U0BRL)
-----------	------	------	------	----------	----------	---------

Bit	7	6	5	4	3	2	1	0
Field				BF	۶L			
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F47H							



Software Compensation Procedure

The value read from the ADC high and low byte registers are uncompensated. The user mode software must apply gain and offset correction to this uncompensated value for maximum accuracy. The following formula yields the compensated value:

 $ADC_{comp} = (ADC_{uncomp} - OFFCAL) + ((ADC_{uncomp} - OFFCAL)*GAINCAL)/2$

where GAINCAL is the gain calibration byte, OFFCAL is the offset calibration byte and ADC_{uncomp} is the uncompensated value read from the ADC. The OFFCAL value is in two's complement format, as are the compensated and uncompensated ADC values.

Note: The offset compensation is performed first, followed by the gain compensation. One bit of resolution is lost because of rounding on both the offset and gain computations. As a result the ADC registers read back 13 bits: 1 sign bit, two calibration bits lost to rounding and 10 data bits. Also note that in the second term, the multiplication must be performed before the division by 2¹⁶. Otherwise, the second term evaluates to zero incorrectly.

Caution: Although the ADC can be used without the gain and offset compensation, it does exhibit non-unity gain. Designing the ADC with sub-unity gain reduces noise across the ADC range but requires the ADC results to be scaled by a factor of 8/7.

ADC Control Register Definitions

The following sections define the ADC Control registers.

ADC Control Register 0

The ADC Control Register selects the analog input channel and initiates the analog-to-digital conversion.

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ADC Control/Status Register 1

The second ADC Control Register contains the voltage reference level selection bit.

Table 75. ADC Control/Status Register 1 (ADCCTL1)

Bit	7	6	5	4	3	2	1	0
Field	REFSELH				Reserved			
RESET	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F71H							
Bit	Description							
[7] REFSELH	 Voltage Reference Level Select High Bit In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this bit determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference. 00 = Internal Reference Disabled, reference comes from external pin. 01 = Internal Reference set to 1.0V. 10 = Internal Reference set to 2.0V (default). 							
[6:0]	[6:0] Reserved These bits are reserved and must be programmed to 0000000.							

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Table 80. Flash Code Protection Using the Flash Option Bits

FWP	Flash Code Protection Description
0	Programming and erasing disabled for all of Flash Program Memory. In user code program- ming, Page Erase, and Mass Erase are all disabled. Mass Erase is available through the On- Chip Debugger.
1	Programming, Page Erase, and Mass Erase are enabled for all of Flash Program Memory.

Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the same page previously stored there. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. For more details, see Figure 21.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

Sector-Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! XP devices are divided into maximum number of 8 sectors. A sector is 1/8 of the total Flash memory size unless this value is smaller than the page size – in which case, the sector and page sizes are equal. On Z8 Encore! F0823 Series devices, the sector size is varied according to the Flash memory configuration shown in <u>Table 79</u> on page 134.

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset, and any previously-written protection values are lost. User code must write this register in their initialization routine if they prefer to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Register with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register,

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These serial numbers are stored in the Flash information page (for more details, see the <u>Reading the Flash Information Page</u> section on page 148 and the <u>Serialization Data</u> section on page 154) and are unaffected by mass erasure of the device's Flash memory.

Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

The randomized lot identifier is a 32-byte binary value, stored in the flash information page (for more details, see the <u>Reading the Flash Information Page</u> section on page 148 and the <u>Randomized Lot Identifier</u> section on page 154) and is unaffected by mass erasure of the device's flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash Information Area.

; get value at info address 60 (FE60h) ldx FPS, #%80 ; enable access to flash info page ld R0, #%FE ld R1, #%60 ldc R2, @RR0 ; R2 now contains the calibration value

Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address (TRMADR) Register contains the target address for an access to the trim option bits.

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Table 87. Trim Bit Address Register (TRMADR)

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On-Chip Debugger Commands

The host communicates to the OCD by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of Z8 Encore! XP F0823 Series products. When this option is enabled, several of the OCD commands are disabled.

Table 101 is a summary of the OCD commands. Each OCD command is described in further detail in the pages that follow this table. <u>Table 102</u> on page 167 also indicates those commands that operate when the device is not in DEBUG Mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Debug Command	Command Byte	Enabled when not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	-
Reserved	01H	-	-
Read OCD Status Register	02H	Yes	-
Read Runtime Counter	03H	-	-
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	-
Write Program Counter	06H	-	Disabled.
Read Program Counter	07H	-	Disabled.
Write Register	08H	_	Only writes of the Flash Memory Con- trol registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Con- trol Register.
Read Register	09H	-	Disabled.
Write Program Memory	0AH	-	Disabled.
Read Program Memory	0BH	_	Disabled.
Write Data Memory	0CH	-	Yes.
Read Data Memory	0DH	-	-
Read Program Memory CRC	0EH	_	-
Reserved	0FH	-	-
Step Instruction	10H	-	Disabled.
Stuff Instruction	11H	-	Disabled.
Execute Instruction	12H	-	Disabled.
Reserved	13H–FFH	_	-

Table 101. OCD Commands

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In the following list of OCD Commands, data and commands sent from the host to the OCD are identified by 'DBG \leftarrow Command/Data'. Data sent from the OCD back to the host is identified by 'DBG \rightarrow Data'.

Read OCD Revision (00H). The Read OCD Revision command determines the version of the OCD. If OCD commands are added, removed, or changed, this revision number changes.

```
DBG \leftarrow 00H
DBG \rightarrow OCDRev[15:8] (Major revision number)
DBG \rightarrow OCDRev[7:0] (Minor revision number)
```

Read OCD Status Register (02H). The Read OCD Status Register command reads the OCDSTAT Register.

```
DBG \leftarrow 02H
DBG \rightarrow OCDSTAT[7:0]
```

Read Runtime Counter (03H). The Runtime Counter counts system clock cycles in between breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the Write Memory, Read Memory, Write Register, Read Register, Read Memory CRC, Step Instruction, Stuff Instruction, and Execute Instruction commands.

```
DBG \leftarrow 03H
DBG \rightarrow RuntimeCounter[15:8]
DBG \rightarrow RuntimeCounter[7:0]
```

Write OCD Control Register (04H). The Write OCD Control Register command writes the data that follows to the OCDCTL register. When the Flash Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of returning the device to normal operating mode is to reset the device.

```
DBG \leftarrow 04H
DBG \leftarrow OCDCTL[7:0]
```

Read OCD Control Register (05H). The Read OCD Control Register command reads the value of the OCDCTL register.

```
DBG \leftarrow 05H
DBG \rightarrow OCDCTL[7:0]
```

Write Program Counter (06H). The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, the Program Counter (PC) values are discarded.

```
DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]
```



DBG \leftarrow 0BH DBG \leftarrow Program Memory Address[15:8] DBG \leftarrow Program Memory Address[7:0] DBG \leftarrow Size[15:8] DBG \leftarrow Size[7:0] DBG \rightarrow 1-65536 data bytes

Write Data Memory (0CH). The Write Data Memory command writes data to Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option Bit is enabled, the data is discarded.

```
DBG \leftarrow 0CH
DBG \leftarrow Data Memory Address[15:8]
DBG \leftarrow Data Memory Address[7:0]
DBG \leftarrow Size[15:8]
DBG \leftarrow Size[7:0]
DBG \leftarrow 1-65536 data bytes
```

Read Data Memory (0DH). The Read Data Memory command reads from Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be read 1 to 65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode, this command returns FFH for the data.

```
DBG \leftarrow 0DH
DBG \leftarrow Data Memory Address[15:8]
DBG \leftarrow Data Memory Address[7:0]
DBG \leftarrow Size[15:8]
DBG \leftarrow Size[7:0]
DBG \rightarrow 1-65536 data bytes
```

Read Program Memory CRC (0EH). The Read Program Memory Cyclic Redundancy Check (CRC) command computes and returns the CRC of Program Memory using the 16bit CRC-CCITT polynomial. If the device is not in DEBUG Mode, this command returns FFFFH for the CRC value. Unlike most other OCD Read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads the Program Memory, calculates the CRC value, and returns the result. The delay is a function of the Program Memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Program Memory.

```
DBG \leftarrow 0EH
DBG \rightarrow CRC[15:8]
DBG \rightarrow CRC[7:0]
```

Step Instruction (10H). The Step Instruction steps one assembly instruction at the current Program Counter (PC) location. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

DBG ← 10H



Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a non-standard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency. The features of IPO include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53 MHz or 32.8 kHz (contains both a fast and a slow mode)
- Trimming possible through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53 MHz (fast mode) or 32.8 kHz (slow mode) is required. This trimming is done at +30°C and a supply voltage of 3.3 V, so accuracy of this operating point is optimal.

Power down this block for minimum system power. By default, the oscillator is configured through the Flash Option bits. However, the user code can override these trim values, as described in the <u>Trim Bit Address Space</u> section on page 151.

Select one of the two frequencies for the oscillator: 5.53MHz and 32.8kHz, using the OSCSEL bits in the <u>Oscillator Control</u> chapter on page 169.

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Figure 33 and Table 134 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.





|--|

		Delay (ns)		
Parameter	Abbreviation	Minimum	Maximum	
UART				
T ₁	DE assertion to TXD falling edge (start bit) delay	1 * X _{IN} period	1 bit time	
T ₂	End of Stop Bit(s) to DE deassertion delay (Tx data register is empty)	± 5		

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Packaging

Zilog's F0823 Series of MCUs includes the Z8F0113, Z8F0123, Z8F0213, Z8F0223, Z8F0413, Z8F0423, Z8F0813 and Z8F0823 devices, which are available in the following packages:

- 8-pin Plastic Dual Inline Package (PDIP)
- 8-Pin Quad Flat No-Lead Package (QFN)/MLF-S¹
- 20-pin Plastic Dual-Inline Package (PDIP)
- 20-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Small Shrink Outline Package (SSOP)
- 28-pin Plastic Dual-Inline Package (PDIP)
- 28-pin Small Outline Integrated Circuit Package (SOIC)
- 28-pin Small Shrink Outline Package (SSOP)

Current diagrams for each of these packages are published in Zilog's <u>Packaging Product</u> <u>Specification (PS0072)</u>, which is available free for download from the Zilog website.

^{1.} The footprint of the QFN)/MLF-S package is identical to that of the 8-pin SOIC package, but with a lower profile.