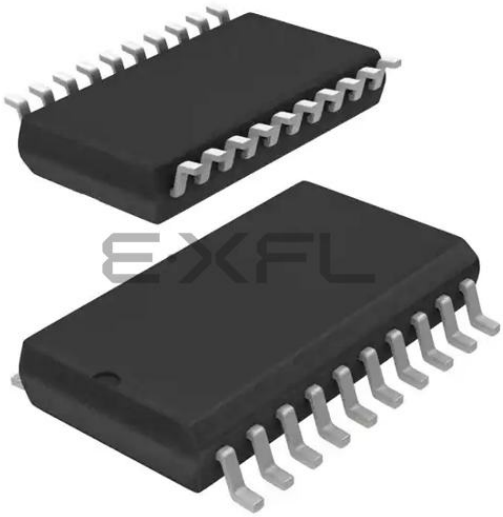

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 5MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0113sh005eg |

**Note:** *Analog input alternate functions (ANA) are not available on Z8F0x13 devices.

# Signal Descriptions

Table 3 lists the Z8 Encore! XP F0823 Series signals. To determine the signals available for the specific package styles, see **the** Pin Configurations **section on page 7**.

**Table 3. Signal Descriptions**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| **General-Purpose I/O Ports A–D** | | |
| PA[7:0] | I/O | Port A. These pins are used for general-purpose I/O. |
| PB[7:0][1] | I/O | Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC. |
| PC[7:0] | I/O | Port C. These pins are used for general-purpose I/O. |
| **UART Controllers** | | |
| TXD0 | O | Transmit Data. This signal is the transmit output from the UART and IrDA. |
| RXD0 | I | Receive Data. This signal is the receive input for the UART and IrDA. |
| $\overline{\text{CTS0}}$ | I | Clear To Send. This signal is the flow control input for the UART. |
| DE | O | Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART. |
| **Timers** | | |
| T0OUT/T1OUT | O | Timer Output 0–1. These signals are output from the timers. |
| $\overline{\text{T0OUT}}$/$\overline{\text{T1OUT}}$ | O | Timer Complement Output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode. |
| T0IN/T1IN | I | Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed $\overline{\text{T0OUT}}$ signals. |
| **Comparator** | | |
| CINP/CINN | I | Comparator Inputs. These signals are the positive and negative inputs to the comparator. |

Notes:
1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by $AV_{DD}$ and $AV_{SS}$.
2. The $AV_{DD}$ and $AV_{SS}$ signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 8-pin devices.

**Table 5. Pin Characteristics (8-Pin Devices)**

| Symbol Mnemonic | Direction | Reset Direction | Active Low or Active High | Tristate Output | Internal Pull-up or Pull-down | Schmitt-Trigger Input | Open Drain Output | 5V Tolerance |
|---|---|---|---|---|---|---|---|---|
| PA0/DBG | I/O | I (but can change during reset if key sequence detected) | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| PA1 | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| $\overline{\text{RESET}}$/PA2 | I/O | I/O (defaults to $\overline{\text{RESET}}$) | N/A | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes, unless pull-ups enabled |
| PA[5:3] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| VDD | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| VSS | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

**Table 8. Register File Address Map (Continued)**

| Address (Hex) | Register Description | Mnemonic | Reset (Hex) | Page No. |
|---|---|---|---|---|
| **LED Controller (cont'd)** | | | | |
| F84 | LED Drive Level Low Byte | LEDLVLL | 00 | 53 |
| F85 | Reserved | — | XX | |
| **Oscillator Control** | | | | |
| F86 | Oscillator Control | OSCCTL | A0 | 172 |
| F87–F8F | Reserved | — | XX | |
| **Comparator 0** | | | | |
| F90 | Comparator 0 Control | CMP0 | 14 | 133 |
| F91–FBF | Reserved | — | XX | |
| **Interrupt Controller** | | | | |
| FC0 | Interrupt Request 0 | IRQ0 | 00 | 59 |
| FC1 | IRQ0 Enable High Bit | IRQ0ENH | 00 | 62 |
| FC2 | IRQ0 Enable Low Bit | IRQ0ENL | 00 | 62 |
| FC3 | Interrupt Request 1 | IRQ1 | 00 | 60 |
| FC4 | IRQ1 Enable High Bit | IRQ1ENH | 00 | 64 |
| FC5 | IRQ1 Enable Low Bit | IRQ1ENL | 00 | 64 |
| FC6 | Interrupt Request 2 | IRQ2 | 00 | 61 |
| FC7 | IRQ2 Enable High Bit | IRQ2ENH | 00 | 65 |
| FC8 | IRQ2 Enable Low Bit | IRQ2ENL | 00 | 66 |
| FC9–FCC | Reserved | — | XX | |
| FCD | Interrupt Edge Select | IRQES | 00 | 67 |
| FCE | Shared Interrupt Select | IRQSS | 00 | 67 |
| FCF | Interrupt Control | IRQCTL | 00 | 68 |
| **GPIO Port A** | | | | |
| FD0 | Port A Address | PAADDR | 00 | 40 |
| FD1 | Port A Control | PACTL | 00 | 42 |
| FD2 | Port A Input Data | PAIN | XX | 43 |
| FD3 | Port A Output Data | PAOUT | 00 | 43 |
| **GPIO Port B** | | | | |
| FD4 | Port B Address | PBADDR | 00 | 40 |
| FD5 | Port B Control | PBCTL | 00 | 42 |

Note: XX=Undefined.

# Low-Power Modes

Z8 Encore! XP F0823 Series products contain power-saving features. The highest level of power reduction is provided by the STOP Mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT Mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in ACTIVE mode (defined as being in neither STOP nor HALT Mode).

## STOP Mode

Executing the eZ8 CPU's Stop instruction places the device into STOP Mode, powering down all peripherals except the Voltage Brown-Out detector, and the Watchdog Timer. These two blocks may also be disabled for additional power savings. In STOP Mode, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; $X_{IN}$ and $X_{OUT}$ (if previously enabled) are disabled, and PA0/PA1 revert to the states programmed by the GPIO registers
- System clock is stopped
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control Register
- If enabled, the Watchdog Timer logic continues to operate
- If enabled for operation in STOP Mode by the associated Flash Option Bit, the Voltage Brown-Out protection circuit continues to operate
- All other on-chip peripherals are idle

To minimize current in STOP Mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails ($V_{CC}$ or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP Mode using Stop Mode Recovery. For more information about Stop Mode Recovery, see the Reset and Stop Mode Recovery chapter on page 21.

## Port A–C Alternate Function Set 2 Subregisters

The Port A–C Alternate Function Set 2 Subregister (Table 29) is accessed through the Port A–C Control Register by writing 08H to the Port A–C Address Register. The Alternate Function Set 2 subregisters selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register is defined in Table 15 in the section the GPIO Alternate Functions section on page 34.

**Table 29. Port A–C Alternate Function Set 2 Subregisters (PxAFS2)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PAFS27 | PAFS26 | PAFS25 | PAFS24 | PAFS23 | PAFS22 | PAFS21 | PAFS20 |
| RESET | 00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device) | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | If 08H in Port A–C Address Register, accessible through the Port A–C Control Register | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>PAFS2x | **Port Alternate Function Set 2**<br>0 = Port Alternate Function selected as defined in Table 15 on page 33; also see the GPIO Alternate Functions section on page 34).<br>1 = Port Alternate Function selected as defined in Table 15. |

Note: x indicates the specific GPIO port pin number (7–0).

# Architecture

Figure 8 displays the interrupt controller block diagram.

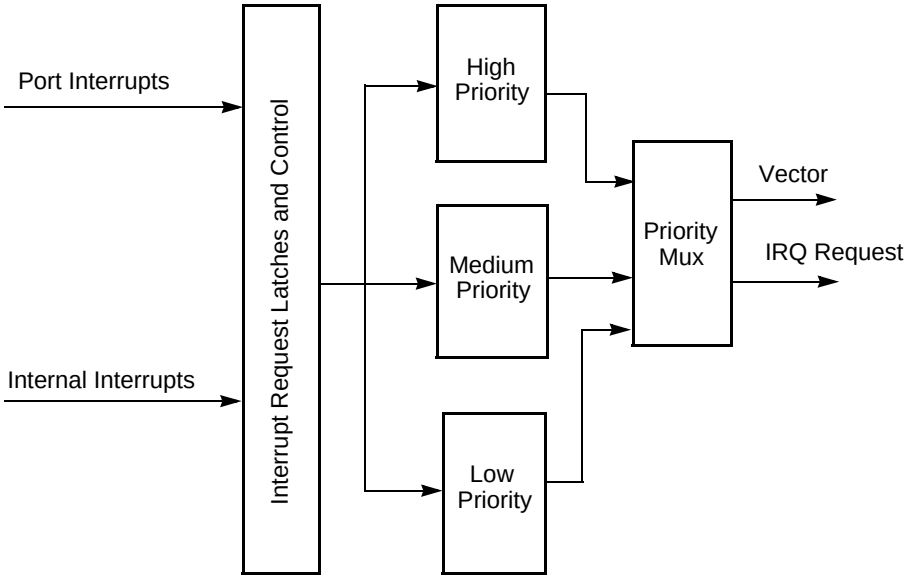


**Figure 8. Interrupt Controller Block Diagram**

# Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 56

Interrupt Vectors and Priority: see page 57

Interrupt Assertion: see page 57

Software Interrupt Assertion: see page 58

Watchdog Timer Interrupt Assertion: see page 58

## Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an Enable Interrupt (EI) instruction

## Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) register (Table 38) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

**Table 38. Interrupt Request 2 Register (IRQ2)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | PC3I | PC2I | PC1I | PC0I |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC6H | | | | | | | |

| Bit | Description |
|---|---|
| [7:4] | **Reserved**<br>These bits are reserved and must be programmed to 0000. |
| [3:0]<br>PCxI | **Port C Pin *x* Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port C pin *x*.<br>1 = An interrupt request from GPIO Port C pin *x* is awaiting service. |

Note: x indicates the specific GPIO Port C pin number (3–0).

## IRQ0 Enable High and Low Bit Registers

Table 39 describes the priority control for IRQ0. The IRQ0 Enable High and Low Bit registers (Table 40 and Table 41) form a priority-encoded enabling for interrupts in the Interrupt Request 0 Register. Priority is generated by setting bits in each register.

**Table 39. IRQ0 Enable and Priority Encoding**

| IRQ0ENH[*x*] | IRQ0ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Nominal |
| 1 | 1 | Level 3 | High |

Note: where *x* indicates the register bits from 0–7.

7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte register are placed in a holding register. A subsequent read from the Timer Low Byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte register returns the actual value in the counter.

## Timer Pin Signal Operation

Timer Output is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO Alternate Function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT mode. For this mode, there is no timer input available.

# Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0–1 High and Low Byte Registers: see page 83

Timer Reload High and Low Byte Registers: see page 84

Timer 0–1 PWM High and Low Byte Registers: see page 86

Timer 0–1 Control Registers: see page 86

## Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 51 and Table 52) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH

The window remains open until the count again reaches 8 (that is, 24 baud clock periods since the previous pulse was detected), giving the endec a sampling window of minus four baud rate clocks to plus eight baud rate clocks around the expected time of an incoming pulse. If an incoming pulse is detected inside this window this process is repeated. If the incoming data is a logical 1 (no pulse), the endec returns to the initial state and waits for the next falling edge. As each falling edge is detected, the endec clock counter is reset, resynchronizing the endec to the incoming signal, allowing the endec to tolerate jitter and baud rate errors in the incoming datastream. Resynchronizing the endec does not alter the operation of the UART, which ultimately receives the data. The UART is only synchronized to the incoming data stream when a Start bit is received.

## Infrared Encoder/Decoder Control Register Definitions

All infrared endec configuration and status information is set by the UART control registers as defined in the Universal Asynchronous Receiver/Transmitter chapter on page 97.

**Caution:** To prevent spurious signals during IrDA data transmission, set the IREN bit in the UART Control 1 Register to 1 to enable the endec before enabling the GPIO port alternate function for the corresponding pin.

| Bit | Description (Continued) |
|---|---|
| [3:0]<br>ANAIN | **Analog Input Select**<br>These bits select the analog input for conversion. Not all port pins in this list are available in all packages for Z8 Encore! XP F0823 Series. For information about the port pins available with each package style, see **the** Pin Description section on page 7. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.<br>For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.<br>**Single-Ended:**<br>0000 = ANA0.<br>0001 = ANA1.<br>0010 = ANA2.<br>0011 = ANA3.<br>0100 = ANA4.<br>0101 = ANA5.<br>0110 = ANA6.<br>0111 = ANA7.<br>1000 = Reserved.<br>1001 = Reserved.<br>1010 = Reserved.<br>1011 = Reserved.<br>1100 = Reserved.<br>1101 = Reserved.<br>1110 = Reserved.<br>1111 = Reserved. |

**Figure 20. Flash Memory Arrangement**

# Flash Information Area

The Flash information area is separate from program memory and is mapped to the address range FE00H to FFFFH. Not all these addresses are accessible. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.

# Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

Figure 21 displays a basic Flash Controller flow. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase, and Mass Erase) displayed in Figure 21.

# ADC Calibration Data

**Table 94. ADC Calibration Bits**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ADC_CAL | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 0060H–007DH | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0] ADC_CAL | **Analog-to-Digital Converter Calibration Values**<br>Contains factory-calibrated values for ADC gain and offset compensation. Each of the ten supported modes has one byte of offset calibration and two bytes of gain calibration. These values are read by the software to compensate ADC measurements as detailed in the Software Compensation Procedure section on page 126. The location of each calibration byte is provided in Table 95. |

**Table 95. ADC Calibration Data Location**

| Info Page Address | Memory Address | Compensation Usage | ADC Mode | Reference Type |
|---|---|---|---|---|
| 60 | FE60 | Offset | Single-Ended Unbuffered | Internal 2.0V |
| 08 | FE08 | Gain High Byte | Single-Ended Unbuffered | Internal 2.0V |
| 09 | FE09 | Gain Low Byte | Single-Ended Unbuffered | Internal 2.0V |
| 63 | FE63 | Offset | Single-Ended Unbuffered | Internal 1.0V |
| 0A | FE0A | Gain High Byte | Single-Ended Unbuffered | Internal 1.0V |
| 0B | FE0B | Gain Low Byte | Single-Ended Unbuffered | Internal 1.0V |
| 66 | FE66 | Offset | Single-Ended Unbuffered | External 2.0V |
| 0C | FE0C | Gain High Byte | Single-Ended Unbuffered | External 2.0V |
| 0D | FE0D | Gain Low Byte | Single-Ended Unbuffered | External 2.0V |

**Table 105. Oscillator Control Register (OSCCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | INTEN | Reserved | WDTEN | POFEN | WDFEN | SCKSEL | | |
| RESET | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F86H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>INTEN | **Internal Precision Oscillator Enable**<br>1 = Internal precision oscillator is enabled.<br>0 = Internal precision oscillator is disabled. |
| [6] | **Reserved**<br>This bit is reserved and must be programmed to 0 during writes and to 0 when read. |
| [5]<br>WDTEN | **Watchdog Timer Oscillator Enable**<br>1 = Watchdog Timer oscillator is enabled.<br>0 = Watchdog Timer oscillator is disabled. |
| [4]<br>POFEN | **Primary Oscillator Failure Detection Enable**<br>1 = Failure detection and recovery of primary oscillator is enabled.<br>0 = Failure detection and recovery of primary oscillator is disabled. |
| [3]<br>WDFEN | **Watchdog Timer Oscillator Failure Detection Enable**<br>1 = Failure detection of Watchdog Timer oscillator is enabled.<br>0 = Failure detection of Watchdog Timer oscillator is disabled. |
| [2:0]<br>SCKSEL | **System Clock Oscillator Select**<br>000 = Internal precision oscillator functions as system clock at 5.53 MHz.<br>001 = Internal precision oscillator functions as system clock at 32 kHz.<br>010 = Reserved.<br>011 = Watchdog Timer oscillator functions as system clock.<br>100 = External clock signal on PB3 functions as system clock.<br>101 = Reserved.<br>110 = Reserved.<br>111 = Reserved. |

# eZ8 CPU Instruction Classes

eZ8 CPU instructions are divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift

Tables 110 through 117 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction can be considered as a subset of more than one category. Within these tables, the source operand is identified as ‘src’, the destination operand is ‘dst’ and a condition code is ‘cc’.

**Table 110. Arithmetic Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| ADC | dst, src | Add with Carry |
| ADCX | dst, src | Add with Carry using Extended Addressing |
| ADD | dst, src | Add |
| ADDX | dst, src | Add using Extended Addressing |
| CP | dst, src | Compare |
| CPC | dst, src | Compare with Carry |
| CPCX | dst, src | Compare with Carry using Extended Addressing |
| CPX | dst, src | Compare using Extended Addressing |
| DA | dst | Decimal Adjust |
| DEC | dst | Decrement |
| DECW | dst | Decrement Word |
| INC | dst | Increment |
| INCW | dst | Increment Word |

**Table 128. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)**

| | | $V_{DD}$ = 3.0V to 3.6V<br>$T_A$ = 0°C to +70°C<br>(unless otherwise stated) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| | Signal Input Bandwidth | – | 10 | | kHz | As defined by –3 dB point |
| $R_S$ | Analog Source Impedance[4] | – | – | 10 | kW | In unbuffered mode |
| Zin | Input Impedance | – | 150 | | kW | In unbuffered mode at 20MHz[5] |
| Vin | Input Voltage Range | 0 | | $V_{DD}$ | V | Unbuffered Mode |

Notes:
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at $V_{DD}$ = 3.3 V and $T_A$ = +30°C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

**Table 129. Comparator Electrical Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $V_{OS}$ | Input DC Offset | | 5 | | mV | |
| $V_{CREF}$ | Programmable Internal Reference Voltage | | ±5 | | % | 20-/28-pin devices |
| | | | ±3 | | % | 8-pin devices |
| $T_{PROP}$ | Propagation Delay | | 200 | | ns | |
| $V_{HYS}$ | Input Hysteresis | | 4 | | mV | |
| $V_{IN}$ | Input Voltage Range | $V_{SS}$ | | $V_{DD}$–1 | V | |

## General Purpose I/O Port Input Data Sample Timing

Figure 29 displays a timing sequence for the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is

available to the eZ8 CPU on the second rising clock edge following the change of the port value.

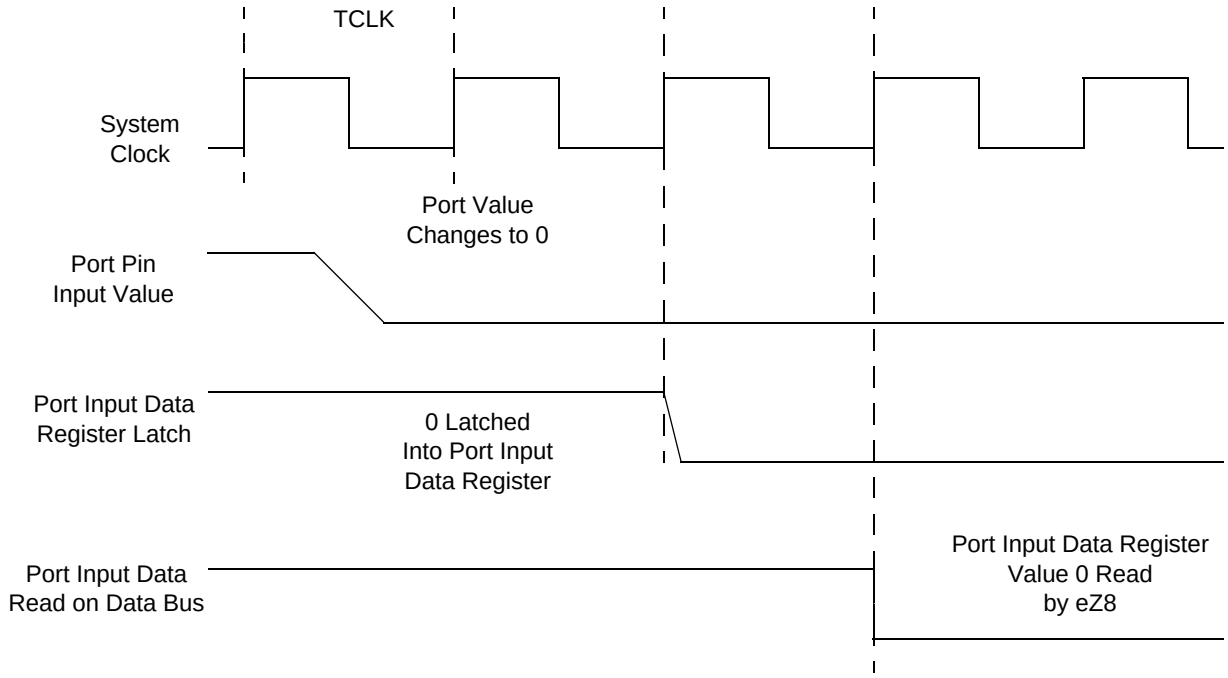


**Figure 29. Port Input Sample Timing**

**Table 130. GPIO Port Input Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| $T_{S\_PORT}$ | Port Input Transition to $X_{IN}$ Rise Setup Time (Not pictured) | 5 | – |
| $T_{H\_PORT}$ | $X_{IN}$ Rise to Port Input Transition Hold Time (Not pictured) | 0 | – |
| $T_{SMR}$ | GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources) | 1 µs | |

Figure 33 and Table 134 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.

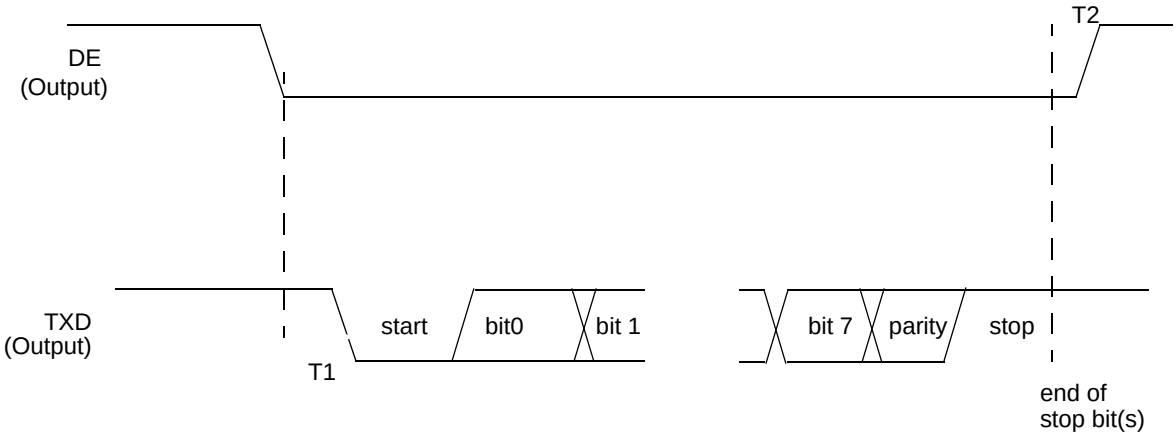


**Figure 33. UART Timing Without CTS**

**Table 134. UART Timing Without CTS**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| **UART** | | | |
| $T_1$ | DE assertion to TXD falling edge (start bit) delay | 1 * $X_{IN}$ period | 1 bit time |
| $T_2$ | End of Stop Bit(s) to DE deassertion delay (Tx data register is empty) | ± 5 | |

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 4 KB Flash** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0413PB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0413QB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0413SB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0413SH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0413HH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0413PH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0413SJ005SG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0413HJ005SG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0413PJ005SG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0413PB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0413QB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0413SB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0413SH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0413HH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0413PH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0413SJ005EG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0413HJ005EG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0413PJ005EG | 4 KB | 1 KB | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 1 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0123PB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0123QB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0123SB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0123SH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0123HH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0123PH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0123SJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0123HJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0123PJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0123PB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0123QB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0123SB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0123SH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0123HH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0123PH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0123SJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0123HJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0123PJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |