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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0123hh005sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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For correct operation, the LED anode must be connected to V_{DD} and the cathode must be connected to the GPIO pin. Using all Port C pins in LED Drive Mode with maximum current can result in excessive total current. For the maximum total current for the applicable package, see the Electrical Characteristics chapter on page 196.

Shared Reset Pin

On the 8-pin product versions, the reset pin is shared with PA2, but the pin is not limited to output-only when in GPIO Mode.

Caution: If PA2 on the 8-pin product is reconfigured as an input, ensure that no external stimulus 1 drives the pin Low during any reset sequence. Because PA2 returns to its RESET alternate function during system resets, driving it Low holds the chip in a reset state until the pin is released.

Shared Debug Pin

On the 8-pin version of this device only, the Debug pin shares function with the PA0 GPIO pin. This pin performs as a general purpose input pin on power-up, but the debug logic monitors this pin during the reset sequence to determine if the unlock sequence occurs. If the unlock sequence is present, the debug function is unlocked and the pin no longer functions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see the On-Chip Debugger chapter on page 156.

Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see the Oscillator Control Register Definitions section on page 171), the GPIO settings are overridden and PA0 and PA1 are disabled.

5V Tolerance

All six I/O pins on the 8-pin devices are 5V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than V_{DD} are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

Note: In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5V-tolerant, including PA[1:0], PB[5:0], and

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	3 0 (<i>)</i>
Port Register Mnemonic	Port Register Name
P <i>x</i> HDE	High Drive Enable.
P <i>x</i> SMRE	Stop Mode Recovery Source Enable.
P <i>x</i> PUE	Pull-up Enable.
PxAFS1	Alternate Function Set 1.
PxAFS2	Alternate Function Set 2.

Table 18. GPIO Port Registers and Subregisters (Continued)

Port A–C Address Registers

The Port A–C Address registers select the GPIO port functionality accessible through the Port A–C Control registers. The Port A–C Address and Control registers combine to provide access to all GPIO port controls (Table 19).

Table 19	. Port A-C	GPIO	Address	Registers	(PxADDR))
----------	------------	------	---------	-----------	----------	---

Bit	7	6	5	4	3	2	1	0
Field		PADDR[7:0]						
RESET		00H						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address		FD0H, FD4H, FD8H						

Bit	Description
[7:0]	Port Address
PADDR	The Port Address selects one of the subregisters accessible through the Port Control Register.
	See Table 20 for each subregister function.

Table 20. PADDR[7:0] Subregister Functions

PADDR[7:0]	Port Control Subregister Accessible Using the Port A–C Control Registers
00H	No function. Provides some protection against accidental Port reconfiguration.
01H	Data Direction.
02H	Alternate Function.
03H	Output Control (Open-Drain).
04H	High Drive Enable.

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Interrupt Controller

The interrupt controller on the Z8 Encore! XP F0823 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 unique interrupt vectors
 - 12 GPIO port pin interrupt sources (two are shared)
 - 8 on-chip peripheral interrupt sources (two are shared)
- Flexible GPIO interrupts
 - Eight selectable rising and falling edge GPIO interrupts
 - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the <u>eZ8 CPU Core User Manual (UM0128)</u> available for download at <u>www.zilog.com</u>.

Interrupt Vector Listing

Table 35 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

Note: Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

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Bit	Description (Continued)
[5] T0ENL	Timer 0 Interrupt Request Enable Low Bit
[4] U0RENL	UART 0 Receive Interrupt Request Enable Low Bit
[3] U0TENL	UART 0 Transmit Interrupt Request Enable Low Bit
[2:1]	Reserved These bits are reserved and must be programmed to 00.
[0] ADCENL	ADC Interrupt Request Enable Low Bit

IRQ1 Enable High and Low Bit Registers

Table 42 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers (Table 43 and Table 44) form a priority-encoded enabling for interrupts in the Interrupt Request 1 Register. Priority is generated by setting bits in each register.

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description		
0	0	Disabled	Disabled		
0	1	Level 1	Low		
1	0	Level 2	Nominal		
1	1	Level 3	High		
Note: x indicates register bits 0–7.					

Table 42. IRQ1 Enable and Priority Encoding

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7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte register are placed in a holding register. A subsequent read from the Timer Low Byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte register returns the actual value in the counter.

Timer Pin Signal Operation

Timer Output is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO Alternate Function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT mode. For this mode, there is no timer input available.

Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0-1 High and Low Byte Registers: see page 83

Timer Reload High and Low Byte Registers: see page 84

Timer 0-1 PWM High and Low Byte Registers: see page 86

Timer 0-1 Control Registers: see page 86

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 51 and Table 52) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH

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Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES TMODE					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H, F0FH							

Table 58. Timer 0–1 Control Register 1 (TxCTL1)

Bit	Description
[7]	Timer Enable
TEN	0 = Timer is disabled.
	1 = Timer enabled to count.
[6]	Timer Input/Output Polarity
TPOL	Operation of this bit is a function of the current operating mode of the timer.
	ONE-SHOT Mode
	When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload.
	CONTINUOUS Mode
	When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload.

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- Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin
- 6. Check the TDRE bit in the UART Status 0 Register to determine if the Transmit Data Register is empty (indicated by a 1). If empty, continue to <u>Step 7</u>. If the Transmit Data Register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data Register becomes available to receive new data.
- 7. Write the UART Control 1 Register to select the outgoing address bit.
- 8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
- 9. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
- 10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR Mode is enabled,.
- 11. To transmit additional bytes, return to <u>Step 5</u>.

Transmitting Data Using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data Register to accept new data for transmission. Observe the following steps to configure the UART for interrupt-driven data transmission:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
- 5. Write to the UART Control 1 Register to enable MULTIPROCESSOR (9-bit) Mode functions, if MULTIPROCESSOR Mode is appropriate.
- 6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.
- 7. Write to the UART Control 0 Register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission.
 - Enable parity, if appropriate and if MULTIPROCESSOR Mode is not enabled, and select either even or odd parity.

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Bit	Description (Continued)
[2] TDRE	 Transmitter Data Register Empty This bit indicates that the UART Transmit Data Register is empty and ready for additional data. Writing to the UART Transmit Data Register resets this bit. 0 = Do not write to the UART Transmit Data Register. 1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted.
[1] TXE	Transmitter Empty This bit indicates that the transmit shift register is empty and character transmission is finished. 0 = Data is currently transmitting. 1 = Transmission is complete.
[0] CTS	CTS Signal When this bit is read, it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low.

UART Status 1 Register

This register contains multiprocessor control and status bits.

Bit	7	6	5	4	3	2	1	0
Field			Rese	erved			NEWFRM	MPRX
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R
Address				F4	4H			

Bit	Description
[7:2]	Reserved These bits are reserved; R/W bits must be programmed to 000000 during writes and 000000 when read.
[1] NEWFRM	 New Frame A status bit denoting the start of a new frame. Reading the UART Receive Data Register resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame.
[0] MPRX	Multiprocessor Receive Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data Register resets this bit to 0.



Bit	Description
[7:5]	Reserved
	These bits are reserved and must be programmed to 111 during writes and to 111 when read.
[4]	State of Crystal Oscillator at Reset
XTLDIS	This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually.
	0 = The crystal oscillator is enabled during reset, resulting in longer reset timing.
	1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing.
	Caution: Programming the XTLDIS bit to zero on 8-pin versions of F0823 Series devices prevents any further communication via the debug pin due to the X_{IN} and DBG functions being shared on pin 2 of the 8-pin package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.
[3:0]	Reserved These bits are reserved and must be programmed to 1111 during writes and to 1111 when read.

Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 91 through 93.

			-	-	-			
Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0020H							
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.							

Table 91. Trim Options Bits at Address 0000H

Bit	Description
[7:0]	Reserved
	These bits are reserved. Altering this register may result in incorrect device operation.

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Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, # 2 of 2

DEBUG Mode

The operating characteristics of the devices in DEBUG Mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP Mode
- All enabled on-chip peripherals operate unless in STOP Mode
- Automatically exits HALT Mode
- Constantly refreshes the Watchdog Timer, if enabled.

Entering DEBUG Mode

The device enters DEBUG Mode following the operations below:

- The device enters DEBUG Mode after the eZ8 CPU executes a BRK (breakpoint) instruction
- If the DBG pin is held Low during the most recent clock cycle of System Reset, the part enters DEBUG Mode upon exiting System Reset

• Note: Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an autobaud sequence (see the <u>OCD Autobaud Detector/</u><u>Generator section on page 159</u>).

 If the PA2/RESET pin is held Low while a 32-bit key sequence is issued to the PA0/ DBG pin, the DBG feature is unlocked. After releasing PA2/RESET, it is pulled high. At this point, the PA0/DBG pin can be used to autobaud and cause the device to enter DEBUG Mode. For more details, see the OCD Unlock Sequence (8-Pin Devices Only) section on page 161.

Exiting DEBUG Mode

The device exits DEBUG Mode following any of these operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset
- Watchdog Timer reset
- Asserting the **RESET** pin Low to initiate a Reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a system reset

OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 Start bit, 8 data bits (least-significant bit first), and 1 Stop bit as displayed in Figure 25.

Figure 25. OCD Data Format

Note: When responding to a request for data, the OCD may commence transmitting immediately after receiving the stop bit of an incoming frame. Therefore, when sending the stop bit, the host must not actively drive the DBG pin High for more than 0.5 bit times. Zilog recommends that, if possible, the host drives the DBG pin using an open-drain output.

OCD Autobaud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the OCD contains an auto-baud detector/generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits Low (one Start bit plus 7 data

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Oscillator Control

Z8 Encore! XP F0823 Series devices uses three possible clocking schemes, each userselectable. These three schemes are:

- On-chip precision trimmed RC oscillator
- External clock drive
- On-chip low power Watchdog Timer oscillator

In addition, F0823 Series devices contain clock failure detection and recovery circuitry, which allow continued operation despite a failure of the primary oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures. A description of the specific operation of each oscillator is outlined elsewhere in this document.

System Clock Selection

The oscillator control block selects from the available clocks. Table 104 details each clock source and its usage.

Clock Source	Characteristics	Required Setup
Internal Precision RC Oscillator	 32.8kHz or 5.53MHz ± 4% accuracy when trimmed No external components required 	 Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator at either 5.53MHz or 32.8kHz
External Clock Drive	 0 to 20MHz Accuracy dependent on external clock source 	 Write GPIO registers to configure PB3 pin for external clock function Unlock and write OSCCTL to select external system clock Apply external clock signal to GPIO
Internal Watchdog Timer Oscillator	 10kHz nominal ± 40% accuracy; no external components required Very Low power consumption 	 Enable WDT if not enabled and wait until WDT Oscillator is operating. Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator

Table 104. Oscillator Configuration and Selection



eZ8 CPU Instruction Set

This chapter describes the following features of the eZ8 CPU instruction set: <u>Assembly Language Programming Introduction</u>: see page 174 <u>Assembly Language Syntax</u>: see page 175

eZ8 CPU Instruction Notation: see page 176

eZ8 CPU Instruction Classes: see page 178

eZ8 CPU Instruction Summary: see page 182

Assembly Language Programming Introduction

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (opcodes and operands) to represent the instructions themselves. The opcodes identify the instruction while the operands represent memory locations, registers, or immediate data values.

Each assembly language program consists of a series of symbolic commands called *statements*. Each statement can contain labels, operations, operands, and comments.

Labels are assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, the pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is detailed in the following example.



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		V _{DD} = 2.7V to 3.6V				
Symbol	Parameter	Typical ¹	Maximum ² Std Temp	Maximum ³ Ext Temp	Units	Conditions
I _{DD} Stop	Supply Current in STOP Mode	0.1	2	7.5	μA	No peripherals enabled. All pins driven to V_{DD} or V_{SS} .
I _{DD} Halt	Supply Current in HALT	35	55	65	μA	32kHz.
	Mode (with all peripher-	520	630	700	μA	5.5MHz.
I _{DD}	Supply Current in	2.8	4.5	4.8	mA	32kHz.
	ACTIVE Mode (with all peripherals disabled)	4.5	5.2	5.2	mA	5.5MHz.
	-					
I _{DD} WDT	Watchdog Timer Sup- ply Current	0.9	1.0	1.1	μA	
I _{DD} IPO	Internal Precision Oscil- lator Supply Current	350	500	550	μA	
I _{DD} VBO	Voltage Brown-Out Sup- ply Current	50			μA	For 20-/28-pin devices (VBO only). ⁴
	-					For 8-pin devices. ⁴
I _{DD} ADC	Analog-to-Digital Con-	2.8	3.1	3.2	mA	32kHz.
	verter Supply Current (with External Refer- ence)	3.1	3.6	3.7	mΑ	5.5MHz.
		3.3	3.7	3.8	mA	10MHz.
	, _	3.7	4.2	4.3	mA	20MHz.
I _{DD} ADCRef	ADC Internal Refer- ence Supply Current	0			μA	See Note 4.
I _{DD} CMP	Comparator supply Cur- rent	150	180	190	μA	See Note 4.
I _{DD} BG	Band Gap Supply Cur-	320	480	500	μA	For 20-/28-pin devices.
	rent					For 8-pin devices.

Table 122. Power Consumption

Notes:

1. Typical conditions are defined as $V_{DD} = 3.3 \text{ V}$ and $+30^{\circ}\text{C}$. 2. Standard temperature is defined as $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

3. Extended temperature is defined as $T_A = -40^{\circ}$ C to +105°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

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On-Chip Debugger Timing

Figure 31 and Table 132 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 ns maximum rise and fall time.



Figure 31	On-Chin	Debugger	Timina
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		Dela	/ (ns)	
Parameter	Abbreviation	Minimum	Maximum	
DBG				
T ₁	X _{IN} Rise to DBG Valid Delay	_	15	
T ₂	X _{IN} Rise to DBG Output Hold Time	2	-	
T ₃	DBG to X _{IN} Rise Input Setup Time	5	-	
T ₄	DBG to X _{IN} Rise Input Hold Time	5	_	

Table 132. On-Chip Debugger Timing

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UART Timing

Figure 32 and Table 133 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the transmit data register has been loaded with data prior to CTS assertion.



Figure 32. UART Timing With CTS

		Dela	y (ns)
Parameter	Abbreviation	Minimum	Maximum
UART			
T ₁	CTS Fall to DE output delay	2 * X _{IN} period	2 * X _{IN} period + 1 bit time
T ₂	DE assertion to TXD falling edge (start bit) delay	±	: 5
T ₃	End of Stop Bit(s) to DE deassertion delay	±	: 5

Tahlo	133	IIART	Timina	With	CTS
lable	133.	UARI	ruuuy	VVILII	613

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Number			nes	upts	t Timers M	t A/D Channels	F with IrDA	ription
Part I	Flash	RAM	/0 Li	nterr	16-Bi //PW	10-Bi	UARI	Desc
Z8 Encore! XP F0823	Series v	with 4	– KB Fla	 ash, 10)-Bit An	àlog-t	o-Digi	ital Converter
Standard Temperature: 0°C to 70°C								
Z8F0423PB005SG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005SG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005SG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005SG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005SG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005SG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005SG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005SG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005SG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: –40°C to 105°C								
Z8F0423PB005EG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005EG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005EG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005EG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005EG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005EG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005EG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005EG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005EG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)



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