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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	22
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0123sj005sg

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OCD Status Register	168
Oscillator Control	169
Operation	169
System Clock Selection	169
Clock Failure Detection and Recovery	170
Oscillator Control Register Definitions	171
Internal Precision Oscillator	173
Operation	173
eZ8 CPU Instruction Set	174
Assembly Language Programming Introduction	174
Assembly Language Syntax	175
eZ8 CPU Instruction Notation	176
eZ8 CPU Instruction Classes	178
eZ8 CPU Instruction Summary	182
Opcode Maps	192
Electrical Characteristics	196
Absolute Maximum Ratings	196
DC Characteristics	197
AC Characteristics	200
On-Chip Peripheral AC and DC Electrical Characteristics	201
General Purpose I/O Port Input Data Sample Timing	204
General Purpose I/O Port Output Timing	206
On-Chip Debugger Timing	207
UART Timing	208
Packaging	210
Ordering Information	211
Part Number Suffix Designations	220
Index	221
Customer Support	230

- 2.7V to 3.6V operating voltage
- Up to thirteen 5V-tolerant input pins
- 8-, 20-, and 28-pin packages
- 0°C to +70°C and –40°C to +105°C for operating temperature ranges

Part Selection Guide

Table 1 lists the basic features and package styles available for each device within the Z8 Encore! XP® F0823 Series product line.

Table 1. F0823 Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	I/O	ADC Inputs	Packages
Z8F0823	8	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0813	8	1024	6–24	0	8-, 20-, and 28-pins
Z8F0423	4	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0413	4	1024	6–24	0	8-, 20-, and 28-pins
Z8F0223	2	512	6–22	4–8	8-, 20-, and 28-pins
Z8F0213	2	512	6–24	0	8-, 20-, and 28-pins
Z8F0123	1	256	6–22	4–8	8-, 20-, and 28-pins
Z8F0113	1	256	6–24	0	8-, 20-, and 28-pins

On-Chip Debugger

F0823 Series products feature an integrated On-Chip Debugger. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code. A single-pin interface provides communication to the OCD.

► **Note:** *Analog input alternate functions (ANA) are not available on Z8F0x13 devices.

Signal Descriptions

Table 3 lists the Z8 Encore! XP F0823 Series signals. To determine the signals available for the specific package styles, see the [Pin Configurations](#) section on page 7.

Table 3. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A–D		
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[7:0] ¹	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
UART Controllers		
TXD0	O	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	I	Clear To Send. This signal is the flow control input for the UART.
DE	O	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT/T1OUT	O	Timer Output 0–1. These signals are output from the timers.
T0OUT/T1OUT	O	Timer Complement Output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed T0OUT signals.
Comparator		
CINP/CINN	I	Comparator Inputs. These signals are the positive and negative inputs to the comparator.

Notes:

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS}.
2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Bit	Description (Continued)
[4] EXT	External Reset Indicator If this bit is set to 1, a Reset initiated by the external <u>RESET</u> pin occurred. A Power-On Reset or a Stop Mode Recovery from a change in an input pin resets this bit. Reading this register resets this bit. For POR/Stop Mode Recover event values, please see Table 13.
[3:0]	Reserved These bits are reserved and must be programmed to 0000 when read.

Table 13. POR Indicator Values

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using WDT time-out	0	0	1	0
Reset using the OCD (OCTCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using WDT time-out	0	1	1	0

PC[2:0]. All other signal pins are 5 V-tolerant, and can safely handle inputs higher than V_{DD} even with the pull-ups enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see the [Oscillator Control Register Definitions](#) section on page 171) such that the external oscillator is selected as the system clock. For 8-pin devices, use PA1 instead of PB3.

GPIO Interrupts

Many of the GPIO port pins are used as interrupt sources. Some port pins are configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). For more information about interrupts using the GPIO pins, see the [Interrupt Controller](#) chapter on page 54.

GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data, and output data. Table 18 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

Table 18. GPIO Port Registers and Subregisters

Port Register Mnemonic	Port Register Name
PxADDR	Port A–C Address Register (Selects subregisters).
PxCTL	Port A–C Control Register (Provides access to subregisters).
PxIN	Port A–C Input Data Register.
PxOUT	Port A–C Output Data Register.
Port Subregister Mnemonic	Port Register Name
PxDD	Data Direction.
PxAF	Alternate Function.
PxOC	Output Control (Open-Drain).

Table 43. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7VENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Bit	Description
[7] PA7VENH	Port A Bit[7] Interrupt Request Enable High Bit
[6] PA6CENH	Port A Bit[7] or Comparator Interrupt Request Enable High Bit
[5:0] PAxENH	Port A Bit[x] Interrupt Request Enable High Bit For selection of Port A as the interrupt source, see the Shared Interrupt Select Register section on page 67.

Note: x indicates the specific GPIO Port A pin number (5–0).

Table 44. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7VENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Bit	Description
[7] PA7VENL	Port A Bit[7] Interrupt Request Enable Low Bit
[6] PA6CENL	Port A Bit[7] or Comparator Interrupt Request Enable Low Bit
[5:0] PAxENL	Port A Bit[x] Interrupt Request Enable Low Bit

Note: x indicates the specific GPIO Port A pin number (5–0).

IRQ2 Enable High and Low Bit Registers

Table 45 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers (Table 46 and Table 47) form a priority encoded enabling for interrupts in the Interrupt Request 2 register. Priority is generated by setting bits in each register.

Table 45. IRQ2 Enable and Priority Encoding

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: where x indicates the register bits from 0–7.

Table 46. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC7H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3] C3ENH	Port C3 Interrupt Request Enable High Bit
[2] C2ENH	Port C2 Interrupt Request Enable High Bit
[1] C1ENH	Port C1 Interrupt Request Enable High Bit
[0] C0ENH	Port C0 Interrupt Request Enable High Bit

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first PWM time-out period. If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

PWM Dual Output Mode

In PWM DUAL OUTPUT Mode, the timer outputs a PWM output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from the TxL reads the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

Table 51. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H							

Table 52. Timer 0–1 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

Bit	Description
[7:0]	Timer High and Low Bytes
TH, TL	These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 53 and Table 54) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte register occurs, the temporary holding register value is written to the Timer High Byte register. This operation allows simultaneous updates of the 16-bit Timer reload value. In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit compare value.

ADC Calibration Data

Table 94. ADC Calibration Bits

Bit	7	6	5	4	3	2	1	0
Field	ADC_CAL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0060H–007DH							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] ADC_CAL	Analog-to-Digital Converter Calibration Values Contains factory-calibrated values for ADC gain and offset compensation. Each of the ten supported modes has one byte of offset calibration and two bytes of gain calibration. These values are read by the software to compensate ADC measurements as detailed in the Software Compensation Procedure section on page 126. The location of each calibration byte is provided in Table 95.

Table 95. ADC Calibration Data Location

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
60	FE60	Offset	Single-Ended Unbuffered	Internal 2.0V
08	FE08	Gain High Byte	Single-Ended Unbuffered	Internal 2.0V
09	FE09	Gain Low Byte	Single-Ended Unbuffered	Internal 2.0V
63	FE63	Offset	Single-Ended Unbuffered	Internal 1.0V
0A	FE0A	Gain High Byte	Single-Ended Unbuffered	Internal 1.0V
0B	FE0B	Gain Low Byte	Single-Ended Unbuffered	Internal 1.0V
66	FE66	Offset	Single-Ended Unbuffered	External 2.0V
0C	FE0C	Gain High Byte	Single-Ended Unbuffered	External 2.0V
0D	FE0D	Gain Low Byte	Single-Ended Unbuffered	External 2.0V

OCD Status Register

The OCD Status Register reports status information about the current state of the debugger and the system.

Table 103. OCD Status Register (OCDSTAT)

Bit	7	6	5	4	3	2	1	0
Field	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Description
[7] DBG	Debug Status 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	HALT Mode 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	Flash Read Protect Option Bit Enable 0 = FRP bit enabled to allow disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	Reserved These bits are reserved and must be 00000 when read.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
DA dst	$\text{dst} \leftarrow \text{DA}(\text{dst})$	R		40	*	*	*	X	–	–	2	2
		IR		41							2	3
DEC dst	$\text{dst} \leftarrow \text{dst} - 1$	R		30	–	*	*	*	–	–	2	2
		IR		31							2	3
DECW dst	$\text{dst} \leftarrow \text{dst} - 1$	RR		80	–	*	*	*	–	–	2	5
		IRR		81							2	6
DI	$\text{IRQCTL}[7] \leftarrow 0$			8F	–	–	–	–	–	–	1	2
DJNZ dst, RA	$\text{dst} \leftarrow \text{dst} - 1$ if $\text{dst} \neq 0$ $\text{PC} \leftarrow \text{PC} + \text{X}$	r		0A-FA	–	–	–	–	–	–	2	3
EI	$\text{IRQCTL}[7] \leftarrow 1$			9F	–	–	–	–	–	–	1	2
HALT	HALT Mode			7F	–	–	–	–	–	–	1	2
INC dst	$\text{dst} \leftarrow \text{dst} + 1$	R		20	–	*	*	–	–	–	2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	$\text{dst} \leftarrow \text{dst} + 1$	RR		A0	–	*	*	*	–	–	2	5
		IRR		A1							2	6
IRET	$\text{FLAGS} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 1$ $\text{PC} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 2$ $\text{IRQCTL}[7] \leftarrow 1$			BF	*	*	*	*	*	*	1	5
JP dst	$\text{PC} \leftarrow \text{dst}$	DA		8D	–	–	–	–	–	–	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true $\text{PC} \leftarrow \text{dst}$	DA		0D-FD	–	–	–	–	–	–	3	2
JR dst	$\text{PC} \leftarrow \text{PC} + \text{X}$	DA		8B	–	–	–	–	–	–	2	2
JR cc, dst	if cc is true $\text{PC} \leftarrow \text{PC} + \text{X}$	DA		0B-FB	–	–	–	–	–	–	2	2

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LD dst, rc	dst ← src	r	IM	0C-FC	–	–	–	–	–	–	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	lr	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	4
		R	IM	E6							3	2
		IR	IM	E7							3	3
		lr	r	F3							2	3
		IR	R	F5							3	3
LDC dst, src	dst ← src	r	lrr	C2	–	–	–	–	–	–	2	5
		lr	lrr	C5							2	9
		lrr	r	D2							2	5
LDCI dst, src	dst ← src r ← r + 1 rr ← rr + 1	lr	lrr	C3	–	–	–	–	–	–	2	9
		lrr	lr	D3							2	9
LDE dst, src	dst ← src	r	lrr	82	–	–	–	–	–	–	2	5
		lrr	r	92							2	5
LDEI dst, src	dst ← src r ← r + 1 rr ← rr + 1	lr	lrr	83	–	–	–	–	–	–	2	9
		lrr	lr	93							2	9
LDWX dst, src	dst ← src	ER	ER	1FE8	–	–	–	–	–	–	5	4

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	1.1 BRK	2.2 SRP IM	2.3 ADD r1,r2	2.4 ADD r1,lr2	3.3 ADD R2,R1	3.4 ADD IR2,R1	3.3 ADD R1,IM	3.4 ADD IR1,IM	4.3 ADDX ER2,ER1	4.3 ADDX IM,ER1	2.3 DJNZ r1,X	2.2 JR cc,X	2.2 LD r1,IM	3.2 JP cc,DA	1.2 INC r1	1.2 NOP
	1	2.2 RLC R1	2.3 RLC IR1	2.3 ADC r1,r2	2.4 ADC r1,lr2	3.3 ADC R2,R1	3.4 ADC IR2,R1	3.3 ADC R1,IM	3.4 ADC IR1,IM	4.3 ADCX ER2,ER1	4.3 ADCX IM,ER1	↓	↓	↓	↓	↓	See 2nd Opcode Map
	2	2.2 INC R1	2.3 INC IR1	2.3 SUB r1,r2	2.4 SUB r1,lr2	3.3 SUB R2,R1	3.4 SUB IR2,R1	3.3 SUB R1,IM	3.4 SUB IR1,IM	4.3 SUBX ER2,ER1	4.3 SUBX IM,ER1						1
	3	2.2 DEC R1	2.3 DEC IR1	2.3 SBC r1,r2	2.4 SBC r1,lr2	3.3 SBC R2,R1	3.4 SBC IR2,R1	3.3 SBC R1,IM	3.4 SBC IR1,IM	4.3 SBCX ER2,ER1	4.3 SBCX IM,ER1						
	4	2.2 DA R1	2.3 DA IR1	2.3 OR r1,r2	2.4 OR r1,lr2	3.3 OR R2,R1	3.4 OR IR2,R1	3.3 OR R1,IM	3.4 OR IR1,IM	4.3 ORX ER2,ER1	4.3 ORX IM,ER1						
	5	2.2 POP R1	2.3 POP IR1	2.3 AND r1,r2	2.4 AND r1,lr2	3.3 AND R2,R1	3.4 AND IR2,R1	3.3 AND R1,IM	3.4 AND IR1,IM	4.3 ANDX ER2,ER1	4.3 ANDX IM,ER1						1.2 WDT
	6	2.2 COM R1	2.3 COM IR1	2.3 TCM r1,r2	2.4 TCM r1,lr2	3.3 TCM R2,R1	3.4 TCM IR2,R1	3.3 TCM R1,IM	3.4 TCM IR1,IM	4.3 TCMX ER2,ER1	4.3 TCMX IM,ER1						1.2 STOP
	7	2.2 PUSH R2	2.3 PUSH IR2	2.3 TM r1,r2	2.4 TM r1,lr2	3.3 TM R2,R1	3.4 TM IR2,R1	3.3 TM R1,IM	3.4 TM IR1,IM	4.3 TMX ER2,ER1	4.3 TMX IM,ER1						1.2 HALT
	8	2.5 DECW RR1	2.6 DECW IRR1	2.5 LDE r1,lr2	2.9 LDEI lr1,lr2	3.2 LDX r1,ER2	3.3 LDX lr1,ER2	3.4 LDX IRR2,R1	3.4 LDX IRR2,IR1	3.4 LDX r1,rr2,X	3.4 LDX rr1,rr2,X						1.2 DI
	9	2.2 RL R1	2.3 RL IR1	2.5 LDE r2,lr1	2.9 LDEI lr2,lr1	3.2 LDX r2,ER1	3.3 LDX lr2,ER1	3.4 LDX R2,IRR1	3.5 LDX IR2,IRR1	3.3 LEA r1,r2,X	3.5 LEA rr1,rr2,X						1.2 EI
	A	2.5 INCW RR1	2.6 INCW IRR1	2.3 CP r1,r2	2.4 CP r1,lr2	3.3 CP R2,R1	3.4 CP IR2,R1	3.3 CP R1,IM	3.4 CP IR1,IM	4.3 CPX ER2,ER1	4.3 CPX IM,ER1						1.4 RET
	B	2.2 CLR R1	2.3 CLR IR1	2.3 XOR r1,r2	2.4 XOR r1,lr2	3.3 XOR R2,R1	3.4 XOR IR2,R1	3.3 XOR R1,IM	3.4 XOR IR1,IM	4.3 XORX ER2,ER1	4.3 XORX IM,ER1						1.5 IRET
	C	2.2 RRC R1	2.3 RRC IR1	2.5 LDC r1,lr2	2.9 LDCI lr1,lr2	2.3 JP IRR1	2.9 LDC lr1,lr2		3.4 LD r1,r2,X	3.2 PUSHX ER2							1.2 RCF
	D	2.2 SRA R1	2.3 SRA IR1	2.5 LDC r2,lr1	2.9 LDCI lr2,lr1	2.6 CALL IRR1	2.2 BSWAP R1	3.3 CALL DA	3.4 LD r2,r1,X	3.2 POPX ER1							1.2 SCF
	E	2.2 RR R1	2.3 RR IR1	2.2 BIT p,b,r1	2.3 LD r1,lr2	3.2 LD R2,R1	3.3 LD IR2,R1	3.2 LD R1,IM	3.3 LD IR1,IM	4.2 LDX ER2,ER1	4.2 LDX IM,ER1						1.2 CCF
	F	2.2 SWAP R1	2.3 SWAP IR1	2.6 TRAP Vector	2.3 LD lr1,r2	2.8 MULT RR1	3.3 LD R2,IR1	3.3 BTJ p,b,r1,X	3.4 BTJ p,b,lr1,X								

Figure 27. First Opcode Map

Table 126. Flash Memory Electrical Characteristics and Timing

$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)					
Parameter	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Time	100	–	–	ns	
Flash Byte Program Time	20	–	40	μs	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance	10,000	–	–	cycles	Program/erase cycles

Table 127. Watchdog Timer Electrical Characteristics and Timing

V _{DD} = 2.7V to 3.6V T _A = −40°C to +105°C (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F _{WDT}	WDT Oscillator Frequency		10		kHz	
F _{WDT}	WDT Oscillator Error			±50	%	
T _{WDT-CAL}	WDT Calibrated Timeout	0.98	1	1.02	s	V _{DD} = 3.3 V; T _A = 30°C
		0.70	1	1.30	s	V _{DD} = 2.7V to 3.6V T _A = 0°C to 70°C
		0.50	1	1.50	s	V _{DD} = 2.7V to 3.6V T _A = −40°C to +105°C

Ordering Information

Order your F0823 Series products from Zilog using the part numbers shown in Table 135. For more information about ordering, please consult your local Zilog sales office. The [Sales Location](#) page on the Zilog website lists all regional offices.

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 8 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0°C to 70°C								
Z8F0823PB005SG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005SG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005SG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005SG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005SG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005SG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005SG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005SG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005SG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: -40°C to 105°C								
Z8F0823PB005EG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005EG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005EG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005EG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005EG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005EG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005EG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005EG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005EG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0°C to 70°C								
Z8F0423PB005SG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005SG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005SG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005SG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005SG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005SG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005SG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005SG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005SG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: -40°C to 105°C								
Z8F0423PB005EG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005EG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005EG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005EG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005EG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005EG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005EG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005EG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005EG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package

Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

Example. Part number Z8F0423SH005SG is an 8-bit 20MHz Flash MCU with 4KB of Program Memory and equipped with 6–22 I/O lines and 4–8 ADC channels in a 20-pin SOIC package, operating within a 0°C to +70°C temperature range and built using lead-free solder.

