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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	16
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0223ph005sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Note: *Analog input alternate functions (ANA) are not available on Z8F0x13 devices.

Signal Descriptions

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Table 3 lists the Z8 Encore! XP F0823 Series signals. To determine the signals available for the specific package styles, see the Pin Configurations section on page 7.

Signal Mnemonic	I/O	Description				
General-Purpose I/O Ports A–D						
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.				
PB[7:0] ¹	I/O	Port B. These pins are used for general-purpose I/O. PB6 and PB7 are available only in those devices without an ADC.				
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.				
UART Controllers						
TXD0	0	Transmit Data. This signal is the transmit output from the UART and IrDA.				
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.				
CTS0	Ι	Clear To Send. This signal is the flow control input for the UART.				
DE	0	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 Register. The DE signal can be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.				
Timers						
T0OUT/T1OUT	0	Timer Output 0–1. These signals are output from the timers.				
T0OUT/T1OUT	0	Timer Complement Output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.				
T0IN/T1IN	Ι	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed T0OUT signals.				
Comparator						
CINP/CINN	Ι	Comparator Inputs. These signals are the positive and negative inputs to the comparator.				
Notes:						

Table 3. Signal Descriptions

1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS} .

2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

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Signal Mnemonic	I/O	Description
COUT	0	Comparator Output. This is the output of the comparator.
Analog		
ANA[7:0]	I	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	Ι	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD. Caution: The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V _{DD}	I	Digital Power Supply.
AV _{DD} ²	I	Analog Power Supply.
V _{SS}	I	Digital Ground.
AV _{SS}	I	Analog Ground.
Notes: 1. PB6 and PB7 are	only ava	ailable in 28-pin packages without ADC. In 28-pin packages with ADC, they are

Table 3. Signal Descriptions (Continued)

replaced by AV_{DD} and AV_{SS}.
The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.



clock and reset signals, the required reset duration can be as short as three clock periods and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the RESET input pin is asserted Low, the Z8 Encore! XP F0823 Series devices remain in the Reset state. If the RESET pin is held Low beyond the System Reset timeout, the device exits the Reset state on the system clock rising edge following RESET pin deassertion. Following a System Reset initiated by the external RESET pin, the EXT status bit in the WDT Control (WDTCTL) register is set to 1.

External Reset Indicator

During System Reset or when enabled by the GPIO logic (see **the** <u>Port A–C Control Registers</u> **section on page 42**), the RESET pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows an Z8 Encore! XP F0823 Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO, or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the $\overrightarrow{\text{RESET}}$ pin Low. The $\overrightarrow{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 9 has elapsed.

On-Chip Debugger Initiated Reset

A POR is initiated using the On-Chip Debugger by setting the RST bit in the OCD Control Register. The OCD block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the System Reset. Following the System Reset, the POR bit in the Reset Status (RSTSTAT) Register is set.

Stop Mode Recovery

The device enters into STOP Mode when eZ8 CPU executes a STOP instruction. For more details about STOP Mode, see **the** Low-Power Modes **section on page 30**. During Stop Mode Recovery, the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay also included the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control Register (WDTCTL) and the Oscillator Control Register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required or IPO disabling is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

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The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the STOP bit in the Watchdog Timer Control Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The section following the table provides more detailed information about each of the Stop Mode Recovery sources.

Operating Mode	Stop Mode Recovery Source	Action	
STOP Mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery	
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)	
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery	
	Assertion of external RESET Pin	System Reset	
	Debug Pin driven Low	System Reset	

Table 11. Stop Mode Recovery Sources and Resulting Action

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Watchdog Timer Control Register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and Z8 Encore! XP F0823 Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins can be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

Note: The SMR pulses shorter than specified does not trigger a recovery. When this happens, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1.

Caution: In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or without initiating an interrupt (if enabled for that pin).

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PA0 and PA6 contain two different timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the timer mode. For more details, see the <u>Timers</u> chapter on page 69.

Caution: For pins with multiple alternate functions, Zilog recommends writing to the AFS1 and AFS2 subregisters before enabling the alternate function via the AF Subregister. This prevents spurious transitions through unwanted alternate function modes.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Select Register AFS1	Alternate Function Select Register AFS2
Port A	PA0	TOIN	Timer 0 Input	AFS1[0]: 0	AFS2[0]: 0
		Reserved		AFS1[0]: 0	AFS2[0]: 1
		Reserved		AFS1[0]: 1	AFS2[0]: 0
		T0OUT	Timer 0 Output Complement	AFS1[0]: 1	AFS2[0]: 1
	PA1	T0OUT	Timer 0 Output	AFS1[1]: 0	AFS2[1]: 0
		Reserved		AFS1[1]: 0	AFS2[1]: 1
		CLKIN	External Clock Input	AFS1[1]: 1	AFS2[1]: 0
		Analog Functions*	ADC Analog Input/V _{REF}	AFS1[1]: 1	AFS2[1]: 1
	PA2	DE0	UART 0 Driver Enable	AFS1[2]: 0	AFS2[2]: 0
		RESET	External Reset	AFS1[2]: 0	AFS2[2]: 1
		T1OUT	Timer 1 Output	AFS1[2]: 1	AFS2[2]: 0
		Reserved		AFS1[2]: 1	AFS2[2]: 1
	PA3	CTS0	UART 0 Clear to Send	AFS1[3]: 0	AFS2[3]: 0
		COUT	Comparator Output	AFS1[3]: 0	AFS2[3]: 1
		T1IN	Timer 1 Input	AFS1[3]: 1	AFS2[3]: 0
		Analog Functions*	ADC Analog Input	AFS1[3]: 1	AFS2[3]: 1
	PA4	RXD0	UART 0 Receive Data	AFS1[4]: 0	AFS2[4]: 0
		Reserved		AFS1[4]: 0	AFS2[4]: 1
		Reserved		AFS1[4]: 1	AFS2[4]: 0
		Analog Functions*	ADC/Comparator Input (N)	AFS1[4]: 1	AFS2[4]: 1
	PA5	TXD0	UART 0 Transmit Data	AFS1[5]: 0	AFS2[5]: 0
		T1OUT	Timer 1 Output Complement	AFS1[5]: 0	AFS2[5]: 1
		Reserved		AFS1[5]: 1	AFS2[5]: 0
		Analog Functions*	ADC/Comparator Input (P)	AFS1[5]: 1	AFS2[5]: 1

Table 16. Port Alternate Function Mapping (8-Pin Parts)

Note: *Analog Functions include ADC inputs, ADC reference and comparator inputs. Also, alternate function selection as described in the Port A–C Alternate Function Subregisters section on page 43 must be enabled.

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PC[2:0]. All other signal pins are 5V-tolerant, and can safely handle inputs higher than V_{DD} even with the pull-ups enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see the <u>Oscillator Control Register Definitions</u> section on page 171) such that the external oscillator is selected as the system clock. For 8-pin devices, use PA1 instead of PB3.

GPIO Interrupts

Many of the GPIO port pins are used as interrupt sources. Some port pins are configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). For more information about interrupts using the GPIO pins, see the <u>Interrupt Controller</u> chapter on page 54.

GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data, and output data. Table 18 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

Port Register	
Mnemonic	Port Register Name
P <i>x</i> ADDR	Port A–C Address Register (Selects subregisters).
P <i>x</i> CTL	Port A–C Control Register (Provides access to subregisters).
PxIN	Port A–C Input Data Register.
P <i>x</i> OUT	Port A–C Output Data Register.
Port Subregister	
Mnemonic	Port Register Name
P <i>x</i> DD	Data Direction.
P <i>x</i> AF	Alternate Function.
P <i>x</i> OC	Output Control (Open-Drain).

Table 18. GPIO Port Registers and Subregisters

LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 33). These two bits select between four programmable drive levels. Each pin is individually programmable.

Bit	7	6	5	4	3	2	1	0
Field		LEDLVLH[7:0]						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address		F83H						

Table 33. LED Drive Level High Register (LEDLVLH)

Bit	Description
[7:0]	LED Level High Bit
LEDLVLH	{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C
	pin.
	00 = 3mA.
	01= 7mA.
	10= 13mA.
	11= 20mA.

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PWM Output High Time Ratio (%) = $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by:

PWM Output High Time Ratio (%) = $\frac{PWM Value}{Reload Value} \times 100$

CAPTURE Mode

In CAPTURE Mode, the current timer count value is recorded when the appropriate external Timer Input transition occurs. The capture count value is written to the Timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the capture occurs on a rising edge or a falling edge of the Timer Input signal. When the capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in TxCTL1 Register is set to indicate the timer interrupt is because of an input capture event.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting. The INPCAP bit in TxCTL1 Register clears indicating the timer interrupt is not because of an input capture event.

Observe the following steps to configure a timer for CAPTURE Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for CAPTURE Mode
 - Set the prescale value
 - Set the capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a capture or a reload event. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a reload.
- 5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both

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input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL1 Register.

- 6. Configure the associated GPIO port pin for the Timer Input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

Capture Elapsed Time (s) = (Capture Value – Start Value) × Prescale System Clock Frequency (Hz)

CAPTURE RESTART Mode

In CAPTURE RESTART Mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The capture count value is written to the Timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the capture occurs on a rising edge or a falling edge of the Timer Input signal. When the capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 Register is set to indicate the timer interrupt is because of an input capture event.

If no capture event occurs, the timer counts up to the 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 Register is cleared to indicate the timer interrupt is not caused by an input capture event.

Observe the following steps to configure a timer for CAPTURE RESTART Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for CAPTURE RESTART Mode; setting the mode also involves writing to TMODEHI bit in TxCTL1 Register
 - Set the prescale value
 - Set the capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.

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Table 61. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET		00H						
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF1H							
Note: R/W	ote: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.							

Bit	Description
[7:0]	WDT Reload Upper Byte
WDTU	Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 62. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0		
Field	WDTH									
RESET	04H									
R/W	R/W*									
Address	FF2H									
Note: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.										

Bit	Description
[7:0]	WDT Reload High Byte
WDTH	Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 63. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0		
Field	WDTL									
RESET	00H									
R/W	R/W*									
Address	FF3H									
Note: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.										

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Bit	Description (Continued)				
[2] TDRE	Transmitter Data Register EmptyThis bit indicates that the UART Transmit Data Register is empty and ready for additional data.Writing to the UART Transmit Data Register resets this bit.0 = Do not write to the UART Transmit Data Register.1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted.				
[1] TXE	Transmitter Empty This bit indicates that the transmit shift register is empty and character transmission is finished. 0 = Data is currently transmitting. 1 = Transmission is complete.				
[0] CTS	CTS Signal When this bit is read, it returns the level of the $\overline{\text{CTS}}$ signal. This signal is active Low.				

UART Status 1 Register

This register contains multiprocessor control and status bits.

Bit	7	6	5	4	3	2	1	0		
Field		NEWFRM	MPRX							
RESET	0	0	0	0	0	0	0	0		
R/W	R	R	R	R	R/W	R/W	R	R		
Address	F44H									

Bit	Description						
[7:2]	Reserved These bits are reserved; R/W bits must be programmed to 000000 during writes and 000000 when read.						
[1] NEWFRM	 New Frame A status bit denoting the start of a new frame. Reading the UART Receive Data Register resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame. 						
[0] MPRX	Multiprocessor Receive Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data Register resets this bit to 0.						

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UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 registers (Table 68 and Table 69) configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

Bit	7	6	5	4	3	2	1	0			
Field	TEN	REN	CTSE	PEN	PSEL	SBRK	LBEN				
RESET	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address	F42H										
Bit	Description										
[7] TEN	Transmit Enable \overline{CTC} signal										

Table 68. UART Control 0 Register (U0CTL0)

DI	Description
[7] TEN	Transmit Enable This bit enables or disables the transmitter. The enable is also controlled by the CTS signal and the CTSE bit. If the CTS signal is low and the CTSE bit is 1, the transmitter is enabled. 0 = Transmitter disabled. 1 = Transmitter enabled.
[6] REN	Receive EnableThis bit enables or disables the receiver.0 = Receiver disabled.1 = Receiver enabled.
[5] CTSE	CTSE — CTS Enable 0 = The CTS signal has no effect on the transmitter. 1 = The UART recognizes the CTS signal as an enable control from the transmitter.
[4] PEN	 Parity Enable This bit enables or disables parity. Even or odd is determined by the PSEL bit. 0 = Parity is disabled. 1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit .
[3] PSEL	 Parity Select 0 = Even parity is transmitted and expected on all received data. 1 = Odd parity is transmitted and expected on all received data.
[2] SBRK	 Send Break This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. 0 = No break is sent. 1 = Forces a break condition by setting the output of the transmitter to zero.

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- CEN resets to 0 to indicate the conversion is complete
- 6. If the ADC remains idle for 160 consecutive system clock cycles, it is automatically powered-down.

Continuous Conversion

When configured for continuous conversion, the ADC continuously performs an analogto-digital conversion on the selected analog input. Each new data value over-writes the previous value stored in the ADC Data registers. An interrupt is generated after each conversion.

Caution: In CONTINUOUS Mode, ADC updates are limited by the input signal bandwidth of the ADC and the latency of the ADC and its digital filter. Step changes at the input are not detected at the next output from the ADC. The response of the ADC (in all modes) is limited by the input signal bandwidth and the latency.

Observe the following steps for setting up the ADC and initiating continuous conversion:

- 1. Enable the acceptable analog input by configuring the general-purpose I/O pins for alternate function. This action disables the digital input and output driver.
- 2. Write the ADC Control/Status Register 1 to configure the ADC:
 - Write the REFSELH bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in the ADC Control/Status Register 1.
- 3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control Register can be written simultaneously:
 - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
 - Set CONT to 1 to select continuous conversion.
 - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
 - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELL bit is contained in ADC Control Register 0.
 - Set CEN to 1 to start the conversions.

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Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
LDX dst, src	dst ← src	r	ER	84	-	_	-	-	_	_	3	2
		lr	ER	85	-						3	3
		R	IRR	86	-						3	4
		IR	IRR	87	-						3	5
		r	X(rr)	88	-						3	4
		X(rr)	r	89	-						3	4
		ER	r	94	-						3	2
		ER	lr	95	-						3	3
		IRR	R	96	-						3	4
		IRR	IR	97	-						3	5
		ER	ER	E8	-						4	2
		ER	IM	E9	-						4	2
LEA dst, X(src)	$dst \gets src + X$	r	X(r)	98	_	_	_	_	_	_	3	3
		rr	X(rr)	99	-						3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	-	-	_	-	_	_	2	8
NOP	No operation			0F	-	_	_	_	_	_	1	2
OR dst, src	$dst \gets dst \ OR \ src$	r	r	42	_	*	*	0	_	_	2	3
		r	lr	43	-						2	4
		R	R	44	-						3	3
		R	IR	45	-						3	4
		R	IM	46	-						3	3
		IR	IM	47	-						3	4
ORX dst, src	$dst \gets dst \ OR \ src$	ER	ER	48	-	*	*	0	_	_	4	3
		ER	IM	49	-						4	3
POP dst	dst ← @SP	R		50	_	_	_	_	_	_	2	2
	$SP \leftarrow SP + 1$	IR		51	-						2	3

Table 118. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Z8 Encore! XP[®] F0823 Series Product Specification

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Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the F0823 Series of products, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

Absolute Maximum Ratings

Stresses greater than those listed in Table 120 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		220	mW	
Maximum current into V _{DD} or out of V _{SS}		60	mA	
20-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		430	mW	
Maximum current into V _{DD} or out of V _{SS}		120	mA	
28-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		450	mW	
Maximum current into V _{DD} or out of V _{SS}		125	mA	

Table 120.	Absolute	Maximum	Ratings
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Notes: Operating temperature is specified in DC Characteristics.

This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.

2. This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).



		T _A = -40°C to +105°C (unless otherwise specified)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
I _{LED}	Controlled Current Drive	1.8	3	4.5	mA	{AFS2,AFS1} = {0,0}.
		2.8	7	10.5	mA	${AFS2,AFS1} = {0,1}.$
		7.8	13	19.5	mA	${AFS2,AFS1} = {1,0}.$
		12	20	30	mA	${AFS2,AFS1} = {1,1}.$
C _{PAD}	GPIO Port Pad Capacitance	-	8.0 ²	-	pF	
C _{XIN}	X _{IN} Pad Capaci- tance	-	8.0 ²	-	pF	
C _{XOUT}	X _{OUT} Pad Capaci- tance	-	9.5 ²	-	pF	
I _{PU}	Weak Pull-up Cur- rent	30	100	350	μA	V _{DD} = 3.0V–3.6V.
V _{RAM}	RAM Data Reten- tion Voltage	TBD			V	Voltage at which RAM retains static values; no reading or writing is allowed.

Table 121. DC Characteristics (Continued)

Notes:

1. This condition excludes all pins that have on-chip pull-ups, when driven Low.

2. These values are provided for design guidance only and are not tested in production.



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