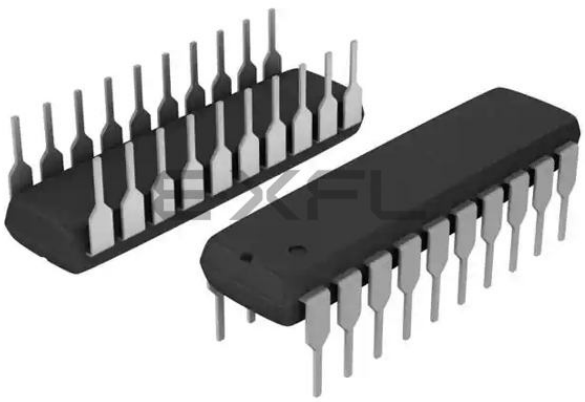

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 5MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0413ph005eg |

# Table of Contents

The eZ8 CPU fetches the Reset vector at Program Memory addresses `0002H` and `0003H` and loads that value into the Program Counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the STOP bit in the Watchdog Timer Control Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The section following the table provides more detailed information about each of the Stop Mode Recovery sources.

**Table 11. Stop Mode Recovery Sources and Resulting Action**

| Operating Mode | Stop Mode Recovery Source | Action |
|---|---|---|
| STOP Mode | Watchdog Timer time-out when configured for Reset | Stop Mode Recovery |
| | Watchdog Timer time-out when configured for interrupt | Stop Mode Recovery followed by interrupt (if interrupts are enabled) |
| | Data transition on any GPIO port pin enabled as a Stop Mode Recovery source | Stop Mode Recovery |
| | Assertion of external $\overline{\text{RESET}}$ Pin | System Reset |
| | Debug Pin driven Low | System Reset |

## Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Watchdog Timer Control Register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and Z8 Encore! XP F0823 Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

## Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins can be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

**Note:** The SMR pulses shorter than specified does not trigger a recovery. When this happens, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1.

**!** **Caution:** In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or without initiating an interrupt (if enabled for that pin).

**Note:** This register is only reset during a Power-On Reset sequence. Other System Reset events do not affect it.

**Table 14. Power Control Register 0 (PWRCTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | Reserved | | VBO | Reserved | ADC | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F80H | | | | | | | |

| Bit | Description |
|---|---|
| [7] | **Reserved**<br>This bit is reserved and must be programmed to 1. |
| [6:5] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [4]<br>VBO | **Voltage Brown-Out Detector Disable**<br>This bit and the VBO_AO Flash option bit must both enable the VBO for the VBO to be active.<br>0 = VBO enabled.<br>1 = VBO disabled. |
| [3] | **Reserved**<br>This bit is reserved and must be programmed to 0. |
| [2]<br>ADC | **Analog-to-Digital Converter Disable**<br>0 = Analog-to-Digital Converter enabled.<br>1 = Analog-to-Digital Converter disabled. |
| [1]<br>COMP | **Comparator Disable**<br>0 = Comparator is enabled.<br>1 = Comparator is disabled. |
| [0] | **Reserved**<br>This bit is reserved and must be programmed to 0. |

| Bit | Description (Continued) |
|---|---|
| [5]<br>T0ENL | **Timer 0 Interrupt Request Enable Low Bit** |
| [4]<br>U0RENL | **UART 0 Receive Interrupt Request Enable Low Bit** |
| [3]<br>U0TENL | **UART 0 Transmit Interrupt Request Enable Low Bit** |
| [2:1] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [0]<br>ADCENL | **ADC Interrupt Request Enable Low Bit** |

## IRQ1 Enable High and Low Bit Registers

Table 42 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers (Table 43 and Table 44) form a priority-encoded enabling for interrupts in the Interrupt Request 1 Register. Priority is generated by setting bits in each register.

**Table 42. IRQ1 Enable and Priority Encoding**

| IRQ1ENH[*x*] | IRQ1ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Nominal |
| 1 | 1 | Level 3 | High |

Note: *x* indicates register bits 0–7.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer reload. If it is appropriate to have the Timer Output make a state change at a One-Shot time-out (rather than a single cycle pulse), first set the TPOL bit in the Timer Control Register to the start value before enabling ONE-SHOT Mode. After starting the timer, set `TPOL` to the opposite bit value.

Observe the following steps to configure a timer for ONE-SHOT Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for ONE-SHOT Mode
   - Set the prescale value
   - Set the initial output level (High or Low) if using the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In ONE-SHOT Mode, the system clock always provides the timer input. The timer period is computed via the following equation:

$$\text{ONE-SHOT Mode Time-Out Period (s)} = \frac{(\text{Reload Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## CONTINUOUS Mode

In CONTINUOUS Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for CONTINUOUS Mode and to initiate the count:

enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for COUNTER Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer.
   - Configure the timer for COUNTER Mode.
   - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER Mode. After the first timer reload in COUNTER Mode, counting always begins at the reset value of `0001H`. In COUNTER Mode the Timer High and Low Byte registers must be written with the value `0001H`.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control Register to enable the timer.

In COUNTER Mode, the number of timer input transitions since the timer start is computed via the following equation:

$$\text{COUNTER Mode Timer Input Transitions} = \text{Current Count Value} - \text{Start Value}$$

## COMPARATOR COUNTER Mode

In COMPARATOR COUNTER Mode, the timer counts input transitions from the analog comparator output. The `TPOL` bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPARATOR COUNTER Mode, the prescaler is disabled.

> **!** **Caution:** The frequency of the comparator output signal must not exceed one-fourth the system clock frequency.

After reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for COMPARATOR COUNTER Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer.
   - Configure the timer for COMPARATOR COUNTER Mode.
   - Select either the rising edge or falling edge of the comparator output signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
2. Write to the Timer High and Low Byte registers to set the starting count value. This action only affects the first pass in COMPARATOR COUNTER Mode. After the first timer reload in COMPARATOR COUNTER Mode, counting always begins at the reset value of `0001H`. Generally, in COMPARATOR COUNTER Mode the Timer High and Low Byte registers must be written with the value `0001H`.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
6. Write to the Timer Control Register to enable the timer.

In COMPARATOR COUNTER Mode, the number of comparator output transitions since the timer start is computed via the following equation:

$$\text{Comparator Output Transitions} = \text{Current Count Value} - \text{Start Value}$$

1. Checks the UART Status 0 Register to determine the source of the interrupt - error, break, or received data.
2. Reads the data from the UART Receive Data Register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) Mode, further actions may be required depending on the MULTIPROCESSOR Mode bits MPMD[1:0].
3. Clears the UART Receiver interrupt in the applicable Interrupt Request register.
4. Executes the `IRET` instruction to return from the interrupt-service routine and await more data.

## Clear To Send ($\overline{\text{CTS}}$) Operation

The CTS pin, if enabled by the CTSE bit of the UART Control 0 Register, performs flow control on the outgoing transmit datastream. The Clear To Send ($\overline{\text{CTS}}$) input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert $\overline{\text{CTS}}$ at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this action is typically performed during Stop Bit transmission. If $\overline{\text{CTS}}$ deasserts in the middle of a character transmission, the current character is sent completely.

## MULTIPROCESSOR (9-Bit) Mode

The UART has a MULTIPROCESSOR (9-bit) Mode that uses an extra ($9^{th}$) bit for selective communication when a number of processors share a common UART bus. In MULTIPROCESSOR Mode (also referred to as 9-bit mode), the multiprocessor bit (`MP`) is transmitted immediately following the 8-bits of data and immediately preceding the Stop bit(s) as displayed in Figure 13. The character format is given below:

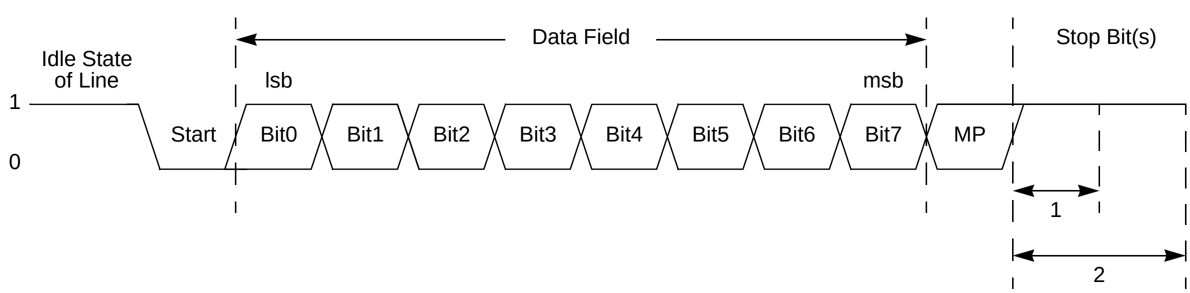


**Figure 13. UART Asynchronous MULTIPROCESSOR Mode Data Format**

In MULTIPROCESSOR (9-bit) Mode, the parity bit location ($9^{th}$ bit) becomes the Multiprocessor control bit. The UART Control 1 and Status 1 registers provide MULTIPROCESSOR (9-bit) Mode control and status information. If an automatic address matching

## UART Address Compare Register

The UART Address Compare Register stores the multinode network address of the UART. When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare Register. Receive interrupts and RDA assertions only occur in the event of a match.

**Table 70. UART Address Compare Register (U0ADDR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | COMP_ADDR | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F45H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>COMP_ADDR | **Compare Address**<br>This 8-bit value is compared to incoming address bytes. |

## UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (Table 71 and Table 72) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

**Table 71. UART Baud Rate High Byte Register (U0BRH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BRH | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F46H | | | | | | | |

**Table 72. UART Baud Rate Low Byte Register (U0BRL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BRL | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F47H | | | | | | | |

# Comparator Control Register Definition

The Comparator Control Register (CMPCTL) configures the comparator inputs and sets the value of the internal voltage reference.

**Table 78. Comparator Control Register (CMP0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | INPSEL | INNSEL | REFLVL | | | | Reserved | |
| RESET | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F90H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>INPSEL | **Signal Select for Positive Input**<br>0 = GPIO pin used as positive comparator input.<br>1 = temperature sensor used as positive comparator input. |
| [6]<br>INNSEL | **Signal Select for Negative Input**<br>0 = internal reference disabled, GPIO pin used as negative comparator input.<br>1 = internal reference enabled as negative comparator input. |
| [5:2]<br>REFLVL | **Internal Reference Voltage Level**<br>0000 = 0.0V.<br>0001 = 0.2V.<br>0010 = 0.4V.<br>0011 = 0.6V.<br>0100 = 0.8V.<br>0101 = 1.0V (Default).<br>0110 = 1.2V.<br>0111 = 1.4V.<br>1000 = 1.6V.<br>1001 = 1.8V.<br>1010–1111 = Reserved.<br>**Note:** This reference is independent of the ADC voltage reference. |
| [1:0] | **Reserved**<br>These bits are reserved; R/W bits must be programmed to 00 during writes and to 00 when read. |

**Table 81. Flash Control Register (FCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FCMD | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | W | W | W | W | W | W | W | W |
| Address | FF8H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>FCMD | **Flash Command**<br>73H = First unlock command.<br>8CH = Second unlock command.<br>95H = Page Erase command (must be third command in sequence to initiate Page Erase).<br>63H = Mass Erase command (must be third command in sequence to initiate Mass Erase).<br>5EH = Enable Flash Sector Protect Register Access. |

**Table 99. Randomized Lot ID Locations**

| Info Page Address | Memory Address | Usage |
|---|---|---|
| 3C | FE3C | Randomized Lot ID Byte 31 (most significant) |
| 3D | FE3D | Randomized Lot ID Byte 30 |
| 3E | FE3E | Randomized Lot ID Byte 29 |
| 3F | FE3F | Randomized Lot ID Byte 28 |
| 58 | FE58 | Randomized Lot ID Byte 27 |
| 59 | FE59 | Randomized Lot ID Byte 26 |
| 5A | FE5A | Randomized Lot ID Byte 25 |
| 5B | FE5B | Randomized Lot ID Byte 24 |
| 5C | FE5C | Randomized Lot ID Byte 23 |
| 5D | FE5D | Randomized Lot ID Byte 22 |
| 5E | FE5E | Randomized Lot ID Byte 21 |
| 5F | FE5F | Randomized Lot ID Byte 20 |
| 61 | FE61 | Randomized Lot ID Byte 19 |
| 62 | FE62 | Randomized Lot ID Byte 18 |
| 64 | FE64 | Randomized Lot ID Byte 17 |
| 65 | FE65 | Randomized Lot ID Byte 16 |
| 67 | FE67 | Randomized Lot ID Byte 15 |
| 68 | FE68 | Randomized Lot ID Byte 14 |
| 6A | FE6A | Randomized Lot ID Byte 13 |
| 6B | FE6B | Randomized Lot ID Byte 12 |
| 6D | FE6D | Randomized Lot ID Byte 11 |
| 6E | FE6E | Randomized Lot ID Byte 10 |
| 70 | FE70 | Randomized Lot ID Byte 9 |
| 71 | FE71 | Randomized Lot ID Byte 8 |
| 73 | FE73 | Randomized Lot ID Byte 7 |
| 74 | FE74 | Randomized Lot ID Byte 6 |
| 76 | FE76 | Randomized Lot ID Byte 5 |
| 77 | FE77 | Randomized Lot ID Byte 4 |
| 79 | FE79 | Randomized Lot ID Byte 3 |
| 7A | FE7A | Randomized Lot ID Byte 2 |
| 7C | FE7C | Randomized Lot ID Byte 1 |
| 7D | FE7D | Randomized Lot ID Byte 0 (least significant) |

**Table 108. Notational Shorthand (Continued)**

| Notation | Description | Operand | Range |
|---|---|---|---|
| RA | Relative Address | X | X represents an index in the range of +127 to –128 which is an offset relative to the address of the next instruction |
| rr | Working Register Pair | RRp | p = 0, 2, 4, 6, 8, 10, 12, or 14. |
| RR | Register Pair | Reg | Reg. represents an even number in the range of 00H to FEH. |
| Vector | Vector Address | Vector | Vector represents a number in the range of 00H to FFH. |
| X | Indexed | #Index | The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to –128 range. |

Table 109 lists additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.

**Table 109. Additional Symbols**

| Symbol | Definition |
|---|---|
| dst | Destination Operand |
| src | Source Operand |
| @ | Indirect Address Prefix |
| SP | Stack Pointer |
| PC | Program Counter |
| FLAGS | Flags Register |
| RP | Register Pointer |
| # | Immediate Operand Prefix |
| B | Binary Number Suffix |
| % | Hexadecimal Number Prefix |
| H | Hexadecimal Number Suffix |

Assignment of a value is indicated by an arrow, as shown in the following example.

dst ← dst + src

This example indicates that the source data is added to the destination data; the result is stored in the destination location.

**Table 110. Arithmetic Instructions (Continued)**

| Mnemonic | Operands | Instruction |
|---|---|---|
| MULT | dst | Multiply |
| SBC | dst, src | Subtract with Carry |
| SBCX | dst, src | Subtract with Carry using Extended Addressing |
| SUB | dst, src | Subtract |
| SUBX | dst, src | Subtract using Extended Addressing |

**Table 111. Bit Manipulation Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| BCLR | bit, dst | Bit Clear |
| BIT | p, bit, dst | Bit Set or Clear |
| BSET | bit, dst | Bit Set |
| BSWAP | dst | Bit Swap |
| CCF | — | Complement Carry Flag |
| RCF | — | Reset Carry Flag |
| SCF | — | Set Carry Flag |
| TCM | dst, src | Test Complement Under Mask |
| TCMX | dst, src | Test Complement Under Mask using Extended Addressing |
| TM | dst, src | Test Under Mask |
| TMX | dst, src | Test Under Mask using Extended Addressing |

**Table 112. Block Transfer Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| LDCI | dst, src | Load Constant to/from Program Memory and Auto-Increment Addresses |
| LDEI | dst, src | Load External Data to/from Data Memory and Auto-Increment Addresses |

**Table 128. Analog-to-Digital Converter Electrical Characteristics and Timing**

| | | $V_{DD}$ = 3.0V to 3.6V<br>$T_A$ = 0°C to +70°C<br>(unless otherwise stated) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| | Resolution | 10 | | – | bits | |
| | Differential Nonlinearity (DNL) | –1.0 | – | 1.0 | LSB[3] | External $V_{REF}$ = 2.0V; $R_S \leftarrow$ 3.0 kΩ |
| | Integral Nonlinearity (INL) | –3.0 | – | 3.0 | LSB[3] | External $V_{REF}$ = 2.0V; $R_S \leftarrow$ 3.0 kΩ |
| | Offset Error with Calibration | | ±1 | | LSB[3] | |
| | Absolute Accuracy with Calibration | | ±3 | | LSB[3] | |
| $V_{REF}$ | Internal Reference Voltage | 1.0<br>2.0 | 1.1<br>2.2 | 1.2<br>2.4 | V | REFSEL=01<br>REFSEL=10 |
| $V_{REF}$ | Internal Reference Variation with Temperature | | ±1.0 | | % | Temperature variation with $V_{DD}$ = 3.0 |
| $V_{REF}$ | Internal Reference Voltage Variation with $V_{DD}$ | | ±0.5 | | % | Supply voltage variation with $T_A$ = 30°C |
| $R_{REFOUT}$ | Reference Buffer Output Impedance | | 850 | | W | When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1) |
| | Single-Shot Conversion Time | – | 5129 | – | System clock cycles | All measurements but temperature sensor |
| | | | 10258 | | | Temperature sensor measurement |
| | Continuous Conversion Time | – | 256 | – | System clock cycles | All measurements but temperature sensor |
| | | | 512 | | | Temperature sensor measurement |

Notes:
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at $V_{DD}$ = 3.3 V and $T_A$ = +30°C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

available to the eZ8 CPU on the second rising clock edge following the change of the port value.

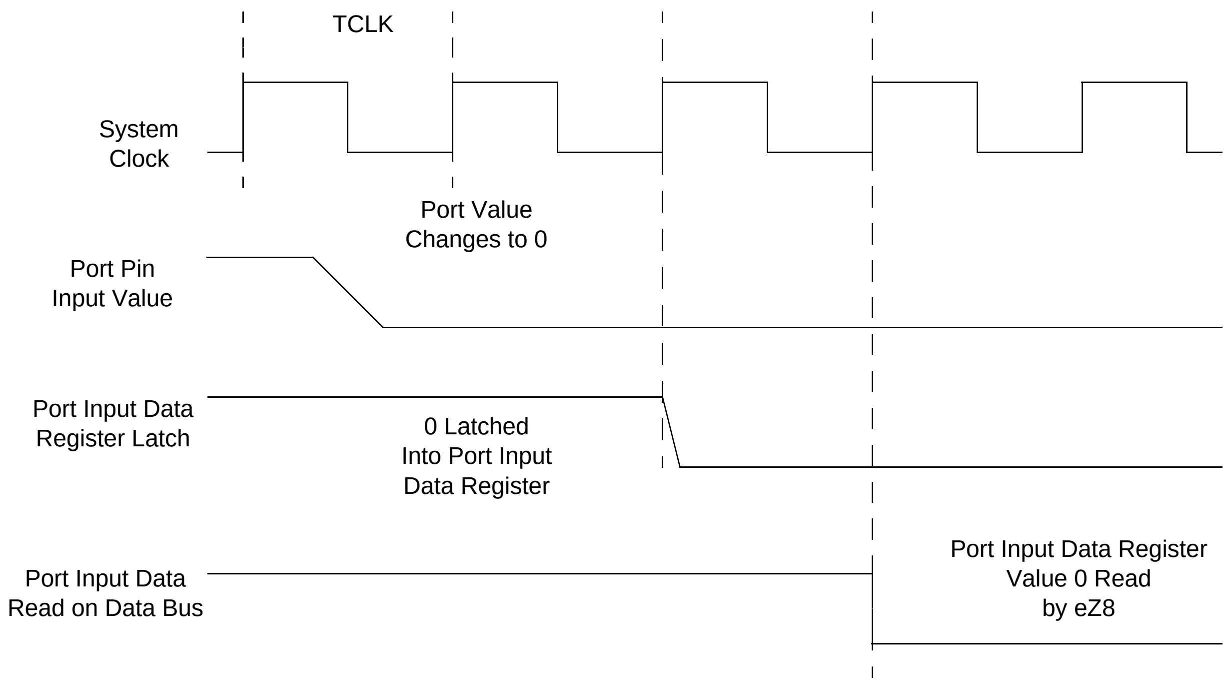


**Figure 29. Port Input Sample Timing**

**Table 130. GPIO Port Input Timing**

| Parameter | Abbreviation | Delay (ns) | |
|---|---|---|---|
| | | **Minimum** | **Maximum** |
| $T_{S\_PORT}$ | Port Input Transition to $X_{IN}$ Rise Setup Time (Not pictured) | 5 | – |
| $T_{H\_PORT}$ | $X_{IN}$ Rise to Port Input Transition Hold Time (Not pictured) | 0 | – |
| $T_{SMR}$ | GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources) | 1 µs | |

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0423PB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0423QB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0423SB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0423SH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0423HH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0423PH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0423SJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0423HJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0423PJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0423PB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0423QB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0423SB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0423SH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0423HH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0423PH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0423SJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0423HJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0423PJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |

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