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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0413sb005eg">https://www.e-xfl.com/product-detail/zilog/z8f0413sb005eg</a>



Figure 30. GPIO Port Output Timing ..... 206

Figure 31. On-Chip Debugger Timing ..... 207

Figure 32. UART Timing With CTS ..... 208

Figure 33. UART Timing Without CTS ..... 209

## Port A–C Alternate Function Set 1 Subregisters

The Port A–C Alternate Function Set1 Subregister (Table 28) is accessed through the Port A–C Control Register by writing 07H to the Port A–C Address Register. The Alternate Function Set 1 subregisters selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register are defined in “**GPIO Alternate Functions**” on page 34.

► **Note:** Alternate function selection on port pins must also be enabled as described in the Port A–C Alternate Function Subregisters section on page 43.

**Table 28. Port A–C Alternate Function Set 1 Subregisters (PAFS1x)**

Bit	7	6	5	4	3	2	1	0
Field	PAFS17	PAFS16	PAFS15	PAFS14	PAFS13	PAFS12	PAFS11	PAFS10
RESET	00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device)							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 07H in Port A–C Address Register, accessible through the Port A–C Control Register							

Bit	Description
[7:0]	<b>Port Alternate Function Set to 1</b>
PAFS1x	0 = Port Alternate Function selected as defined in Table 15 (see the <u>GPIO Alternate Functions</u> section on page 34). 1 = Port Alternate Function selected as defined in Table 15 (see the <u>GPIO Alternate Functions</u> section on page 34).

Note: x indicates the specific GPIO port pin number (7–0).

Table 40. IRQ0 Enable High Bit Register (IRQ0ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENH	T0ENH	U0RENH	U0TENH	Reserved		ADCENH
RESET	0	0	0	0	0	0		0
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Address	FC1H							

Bit	Description
[7]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[6] T1ENH	<b>Timer 1 Interrupt Request Enable High Bit</b>
[5] T0ENH	<b>Timer 0 Interrupt Request Enable High Bit</b>
[4] U0RENH	<b>UART 0 Receive Interrupt Request Enable High Bit</b>
[3] U0TENH	<b>UART 0 Transmit Interrupt Request Enable High Bit</b>
[2:1]	<b>Reserved</b> These bits are reserved and must be programmed to 00.
[0] ADCENH	<b>ADC Interrupt Request Enable High Bit</b>

Table 41. IRQ0 Enable Low Bit Register (IRQ0ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENL	T0ENL	U0RENL	U0TENL	Reserved		ADCENL
RESET	0	0	0	0	0	0		0
R/W	R	R/W	R/W	R/W	R/W	R		R/W
Address	FC2H							

Bit	Description
[7]	<b>Reserved</b> This bit is reserved and must be programmed to 0 when read.
[6] T1ENL	<b>Timer 1 Interrupt Request Enable Low Bit</b>



1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for CONTINUOUS Mode
  - Set the prescale value
  - If using the Timer Output alternate function, set the initial output level (High or Low)
2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is computed via the following equation:

$$\text{CONTINUOUS Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

### **COUNTER Mode**

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER Mode, the prescaler is disabled.

---

**! Caution:** The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.

---

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is

5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. Write to the Timer Control Register to enable the timer.
7. Assert the Timer Input signal to initiate the counting.

### **CAPTURE/COMPARE Mode**

In CAPTURE/COMPARE Mode, the timer begins counting on the first external Timer Input transition. The acceptable transition (rising edge or falling edge) is set by the TPOL bit in the Timer Control Register. The timer input is the system clock.

Every subsequent acceptable transition (after the first) of the Timer Input signal captures the current count value. The capture value is written to the Timer PWM High and Low Byte registers. When the capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H, and counting resumes. The INPCAP bit in TxCTL1 Register is set to indicate the timer interrupt is caused by an input capture event.

If no capture event occurs, the timer counts up to the 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL1 Register is cleared to indicate the timer interrupt is not because of an input capture event.

Observe the following steps to configure a timer for CAPTURE/COMPARE Mode and initiating the count:

1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for CAPTURE/COMPARE Mode
  - Set the prescale value
  - Set the capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the compare value.
4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL1 Register.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. Write to the Timer Control Register to enable the timer.

## **WDT Reset in NORMAL Operation**

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Watchdog Timer Control Register is set to 1. For more information about System Reset, see **the Reset and Stop Mode Recovery** chapter on page 21.

## **WDT Reset in STOP Mode**

If configured to generate a Reset when a time-out occurs and the device is in STOP Mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Watchdog Timer Control Register are set to 1 following WDT time-out in STOP Mode. For more information, see **the Reset and Stop Mode Recovery** chapter on page 21.

## **Watchdog Timer Reload Unlock Sequence**

Writing the unlock sequence to the Watchdog Timer Control Register (WDTCTL) address unlocks the three Watchdog Timer Reload Byte Registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the Reload registers. The following sequence is required to unlock the Watchdog Timer Reload Byte Registers (WDTU, WDTH, and WDTL) for write access.

1. Write 55H to the Watchdog Timer Control Register (WDTCTL).
2. Write AAH to the Watchdog Timer Control Register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte register (WDTU).
4. Write the Watchdog Timer Reload High Byte register (WDTH).
5. Write the Watchdog Timer Reload Low Byte register (WDTL).

All three Watchdog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## **Watchdog Timer Control Register Definitions**

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 94

Watchdog Timer Reload Upper Byte Register (WDTU): see page 95

## UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 registers (Table 68 and Table 69) configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

**Table 68. UART Control 0 Register (U0CTL0)**

Bit	7	6	5	4	3	2	1	0
Field	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F42H							

Bit	Description
[7] TEN	<b>Transmit Enable</b> This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is low and the CTSE bit is 1, the transmitter is enabled. 0 = Transmitter disabled. 1 = Transmitter enabled.
[6] REN	<b>Receive Enable</b> This bit enables or disables the receiver. 0 = Receiver disabled. 1 = Receiver enabled.
[5] CTSE	<b>CTSE—CTS Enable</b> 0 = The $\overline{\text{CTS}}$ signal has no effect on the transmitter. 1 = The UART recognizes the CTS signal as an enable control from the transmitter.
[4] PEN	<b>Parity Enable</b> This bit enables or disables parity. Even or odd is determined by the PSEL bit. 0 = Parity is disabled. 1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit .
[3] PSEL	<b>Parity Select</b> 0 = Even parity is transmitted and expected on all received data. 1 = Odd parity is transmitted and expected on all received data.
[2] SBRK	<b>Send Break</b> This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. 0 = No break is sent. 1 = Forces a break condition by setting the output of the transmitter to zero.

Bit	Description (Continued)
[1] STOP	<b>Stop Bit Select</b> 0 = The transmitter sends one stop bit. 1 = The transmitter sends two stop bits.
[0] LBEN	<b>Loop Back Enable</b> 0 = Normal operation. 1 = All transmitted data is looped back to the receiver.

Table 69. UART Control 1 Register (U0CTL1)

Bit	7	6	5	4	3	2	1	0
Field	MPMD[1]	MPEN	MPMD[0]	MPBT	DEPOL	BRGCTL	RDAIRQ	IREN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F43H							

Bit	Description
[7,5] MPMD[1:0]	<b>MULTIPROCESSOR Mode</b> If MULTIPROCESSOR (9-bit) Mode is enabled. 00 = The UART generates an interrupt request on all received bytes (data and address). 01 = The UART generates an interrupt request only on received address bytes. 10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs. 11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register.
[6] MPEN	<b>MULTIPROCESSOR (9-bit) Enable</b> This bit is used to enable MULTIPROCESSOR (9-bit) Mode. 0 = Disable MULTIPROCESSOR (9-bit) Mode. 1 = Enable MULTIPROCESSOR (9-bit) Mode.
[4] MPBT	<b>Multiprocessor Bit Transmit</b> This bit is applicable only when MULTIPROCESSOR (9-bit) Mode is enabled. The 9th bit is used by the receiving device to determine if the data byte contains address or data information. 0 = Send a 0 in the multiprocessor bit location of the data stream (data byte). 1 = Send a 1 in the multiprocessor bit location of the data stream (address byte).
[3] DEPOL	<b>Driver Enable Polarity</b> 0 = DE signal is Active High. 1 = DE signal is Active Low.

4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
  - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation
  - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete
5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
  - Writes the 11-bit two's complement result to {ADCD\_H[7:0], ADCD\_L[7:5]}
  - An interrupt request to the Interrupt Controller denoting conversion complete
6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

## **Interrupts**

The ADC is able to interrupt the CPU whenever a conversion has been completed and the ADC is enabled.

When the ADC is disabled, an interrupt is not asserted; however, an interrupt pending when the ADC is disabled is not cleared.

## **Calibration and Compensation**

Z8 Encore! XP F0823 Series ADC can be factory calibrated for offset error and gain error, with the compensation data stored in Flash memory. Alternatively, user code can perform its own calibration, storing the values into Flash themselves.

### **Factory Calibration**

Devices that have been factory calibrated contain nine bytes of calibration data in the Flash option bit space. This data consists of three bytes for each reference type. For a list of input modes for which calibration data exists, see the [Zilog Calibration Data](#) section on page 152. There is 1 byte for offset, and there are 2 bytes for gain correction.

### **User Calibration**

If you have precision references available, its own external calibration can be performed, storing the values into Flash themselves.

## ADC Data High Byte Register

The ADC Data High Byte Register contains the upper eight bits of the ADC output. The output is an 11-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

**Table 76. ADC Data High Byte Register (ADCD\_H)**

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	F72H							

Bit	Description
[7:0]	<b>ADC Data High Byte</b>
ADCDH	This byte contains the upper eight bits of the ADC output. These bits are not valid during a single-shot conversion. During a continuous conversion, the most recent conversion output is held in this register. These bits are undefined after a Reset.

**Table 99. Randomized Lot ID Locations**

<b>Info Page Address</b>	<b>Memory Address</b>	<b>Usage</b>
3C	FE3C	Randomized Lot ID Byte 31 (most significant)
3D	FE3D	Randomized Lot ID Byte 30
3E	FE3E	Randomized Lot ID Byte 29
3F	FE3F	Randomized Lot ID Byte 28
58	FE58	Randomized Lot ID Byte 27
59	FE59	Randomized Lot ID Byte 26
5A	FE5A	Randomized Lot ID Byte 25
5B	FE5B	Randomized Lot ID Byte 24
5C	FE5C	Randomized Lot ID Byte 23
5D	FE5D	Randomized Lot ID Byte 22
5E	FE5E	Randomized Lot ID Byte 21
5F	FE5F	Randomized Lot ID Byte 20
61	FE61	Randomized Lot ID Byte 19
62	FE62	Randomized Lot ID Byte 18
64	FE64	Randomized Lot ID Byte 17
65	FE65	Randomized Lot ID Byte 16
67	FE67	Randomized Lot ID Byte 15
68	FE68	Randomized Lot ID Byte 14
6A	FE6A	Randomized Lot ID Byte 13
6B	FE6B	Randomized Lot ID Byte 12
6D	FE6D	Randomized Lot ID Byte 11
6E	FE6E	Randomized Lot ID Byte 10
70	FE70	Randomized Lot ID Byte 9
71	FE71	Randomized Lot ID Byte 8
73	FE73	Randomized Lot ID Byte 7
74	FE74	Randomized Lot ID Byte 6
76	FE76	Randomized Lot ID Byte 5
77	FE77	Randomized Lot ID Byte 4
79	FE79	Randomized Lot ID Byte 3
7A	FE7A	Randomized Lot ID Byte 2
7C	FE7C	Randomized Lot ID Byte 1
7D	FE7D	Randomized Lot ID Byte 0 (least significant)



## Operation

The following section describes the operation of the OCD.

### OCD Interface

The OCD uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, in that transmit and receive cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface from the F0823 Series products to the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figure 23 and Figure 24. The recommended method is the buffered implementation depicted in Figure 24. The DBG pin has an internal pull-up resistor which is sufficient for some applications (for more details about the pull-up current, see the [Electrical Characteristics](#) chapter on page 196). For OCD operation at higher data rates or in noisy systems, Zilog recommends an external pull-up resistor.

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**! Caution:** For operation of the OCD, all power pins ( $V_{DD}$  and  $AV_{DD}$ ) must be supplied with power, and all ground pins ( $V_{SS}$  and  $AV_{SS}$ ) must be properly grounded. The DBG pin is open-drain and may require an external pull-up resistor to ensure proper operation.

---

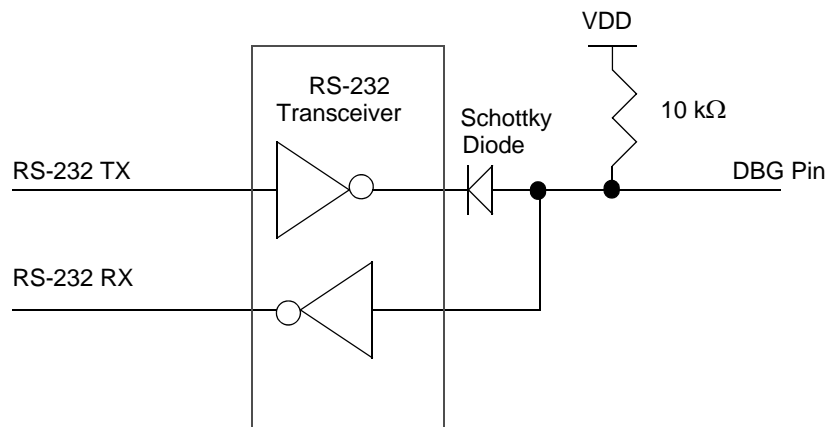


Figure 23. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, # 1 of 2

**Read Program Counter (07H).** The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, this command returns FFFFH.

```
DBG ← 07H
DBG → ProgramCounter[15:8]
DBG → ProgramCounter[7:0]
```

**Write Register (08H).** The Write Register command writes data to the Register File. Data can be written 1–256 bytes at a time (256 bytes can be written by setting size to 0). If the device is not in DEBUG Mode, the address and data values are discarded. If the Flash Read Protect Option bit is enabled, only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

```
DBG ← 08H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG ← 1-256 data bytes
```

**Read Register (09H).** The Read Register command reads data from the Register File. Data can be read 1–256 bytes at a time (256 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, this command returns FFH for all the data values.

```
DBG ← 09H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG → 1-256 data bytes
```

**Write Program Memory (0AH).** The Write Program Memory command writes data to Program Memory. This command is equivalent to the LDC and LDCT instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. If the device is not in DEBUG Mode or if the Flash Read Protect Option bit is enabled, the data is discarded.

```
DBG ← 0AH
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1-65536 data bytes
```

**Read Program Memory (0BH).** The Read Program Memory command reads data from Program Memory. This command is equivalent to the LDC and LDCT instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash Read Protect Option Bit is enabled, this command returns FFH for the data.

**Table 119. Opcode Map Abbreviations**

<b>Abbreviation</b>	<b>Description</b>	<b>Abbreviation</b>	<b>Description</b>
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

# Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the F0823 Series of products, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

## Absolute Maximum Ratings

Stresses greater than those listed in Table 120 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages ( $V_{DD}$  or  $V_{SS}$ ).

**Table 120. Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	−40	+105	°C	
Storage temperature	−65	+150	°C	
Voltage on any pin with respect to $V_{SS}$	−0.3	+5.5	V	1
	−0.3	+3.9	V	2
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	−0.3	+3.6	V	
Maximum current on input and/or inactive output pin	−5	+5	μA	
Maximum output current from active output pin	−25	+25	mA	
<b>8-pin Packages Maximum Ratings at 0°C to 70°C</b>				
Total power dissipation		220	mW	
Maximum current into $V_{DD}$ or out of $V_{SS}$		60	mA	
<b>20-pin Packages Maximum Ratings at 0°C to 70°C</b>				
Total power dissipation		430	mW	
Maximum current into $V_{DD}$ or out of $V_{SS}$		120	mA	
<b>28-pin Packages Maximum Ratings at 0°C to 70°C</b>				
Total power dissipation		450	mW	
Maximum current into $V_{DD}$ or out of $V_{SS}$		125	mA	

Notes: Operating temperature is specified in DC Characteristics.

1. This voltage applies to all pins except the following:  $V_{DD}$ ,  $AV_{DD}$ , pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but  $V_{DD}$ .
2. This voltage applies to pins on the 20/28 pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

## AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50 pF on all outputs.

**Table 123. AC Characteristics**

$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)					
Symbol	Parameter	Minimum	Maximum	Units	Conditions
F <sub>SYSCLK</sub>	System Clock Frequency	–	20.0*	MHz	Read-only from Flash memory.
		0.032768	20.0 <sup>1</sup>	MHz	Program or erasure of the Flash memory.
T <sub>XIN</sub>	System Clock Period	50	–	ns	T <sub>CLK</sub> = 1/F <sub>SYSCLK</sub> .
T <sub>XINH</sub>	System Clock High Time	20	30	ns	T <sub>CLK</sub> = 50ns.
T <sub>XINL</sub>	System Clock Low Time	20	30	ns	T <sub>CLK</sub> = 50ns.
T <sub>XINR</sub>	System Clock Rise Time	–	3	ns	T <sub>CLK</sub> = 50ns.
T <sub>XINF</sub>	System Clock Fall Time	–	3	ns	T <sub>CLK</sub> = 50ns.
Note: *System Clock Frequency is limited by the Internal Precision Oscillator on the Z8 Encore! XP F0823 Series. See Table 124 on page 200.					

**Table 124. Internal Precision Oscillator Electrical Characteristics**

$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F <sub>IPO</sub>	Internal Precision Oscillator Frequency (High Speed)		5.53		MHz	V <sub>DD</sub> = 3.3V T <sub>A</sub> = 30°C
F <sub>IPO</sub>	Internal Precision Oscillator Frequency (Low Speed)		32.7		kHz	V <sub>DD</sub> = 3.3V T <sub>A</sub> = 30°C
F <sub>IPO</sub>	Internal Precision Oscillator Error		±1	±4	%	
T <sub>IPOST</sub>	Internal Precision Oscillator Startup Time		3		μs	

## On-Chip Peripheral AC and DC Electrical Characteristics

Table 125 tabulates the electrical characteristics of the POR and VBO blocks.

**Table 125. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing**

Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$			Units	Conditions
		Minimum	Typical*	Maximum		
$V_{\text{POR}}$	Power-On Reset Voltage Threshold	2.20	2.45	2.70	V	$V_{\text{DD}} = V_{\text{POR}}$
$V_{\text{VBO}}$	Voltage Brown-Out Reset Voltage Threshold	2.15	2.40	2.65	V	$V_{\text{DD}} = V_{\text{VBO}}$
	$V_{\text{POR}}$ to $V_{\text{VBO}}$ hysteresis		50	75	mV	
	Starting $V_{\text{DD}}$ voltage to ensure valid Power-On Reset.	—	$V_{\text{SS}}$	—	V	
$T_{\text{ANA}}$	Power-On Reset Analog Delay	—	70	—	$\mu\text{s}$	$V_{\text{DD}} > V_{\text{POR}}$ ; $T_{\text{POR}}$ Digital Reset delay follows $T_{\text{ANA}}$
$T_{\text{POR}}$	Power-On Reset Digital Delay		16		$\mu\text{s}$	66 Internal Precision Oscillator cycles + IPO startup time ( $T_{\text{IPOST}}$ )
$T_{\text{SMR}}$	Stop Mode Recovery		16		$\mu\text{s}$	66 Internal Precision Oscillator cycles
$T_{\text{VBO}}$	Voltage Brown-Out Pulse Rejection Period	—	10	—	$\mu\text{s}$	Period of time in which $V_{\text{DD}} < V_{\text{VBO}}$ without generating a Reset.
$T_{\text{RAMP}}$	Time for $V_{\text{DD}}$ to transition from $V_{\text{SS}}$ to $V_{\text{POR}}$ to ensure valid Reset	0.10	—	100	ms	
$T_{\text{SMP}}$	Stop Mode Recovery pin pulse rejection period		20		ns	For any SMR pin or for the Reset pin when it is asserted in STOP Mode.

Note: \*Data in the typical column is from characterization at 3.3 V and 30°C. These values are provided for design guidance only and are not tested in production.

**Table 126. Flash Memory Electrical Characteristics and Timing**

$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)					
Parameter	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Time	100	–	–	ns	
Flash Byte Program Time	20	–	40	$\mu s$	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance	10,000	–	–	cycles	Program/erase cycles

**Table 127. Watchdog Timer Electrical Characteristics and Timing**

V <sub>DD</sub> = 2.7V to 3.6V T <sub>A</sub> = −40°C to +105°C (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F <sub>WDT</sub>	WDT Oscillator Frequency		10		kHz	
F <sub>WDT</sub>	WDT Oscillator Error			±50	%	
T <sub>WDT-CAL</sub>	WDT Calibrated Timeout	0.98	1	1.02	s	V <sub>DD</sub> = 3.3 V; T <sub>A</sub> = 30°C
		0.70	1	1.30	s	V <sub>DD</sub> = 2.7V to 3.6V T <sub>A</sub> = 0°C to 70°C
		0.50	1	1.50	s	V <sub>DD</sub> = 2.7V to 3.6V T <sub>A</sub> = −40°C to +105°C

General Purpose I/O Port Output Timing

Figure 30 and Table 131 provide timing information for GPIO Port pins.

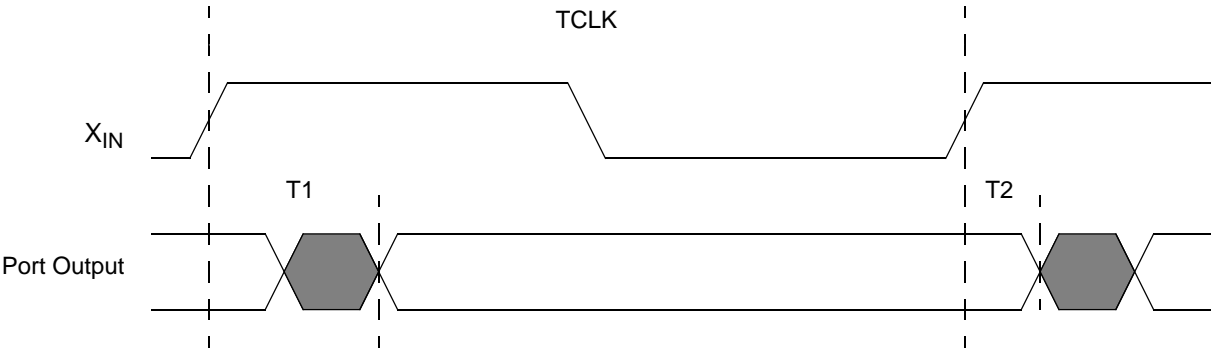


Figure 30. GPIO Port Output Timing

Table 131. GPIO Port Output Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
GPIO Port pins			
T <sub>1</sub>	X <sub>IN</sub> Rise to Port Output Valid Delay	–	15
T <sub>2</sub>	X <sub>IN</sub> Rise to Port Output Hold Time	2	–



## Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

**Example.** Part number Z8F0423SH005SG is an 8-bit 20MHz Flash MCU with 4KB of Program Memory and equipped with 6–22 I/O lines and 4–8 ADC channels in a 20-pin SOIC package, operating within a 0°C to +70°C temperature range and built using lead-free solder.

