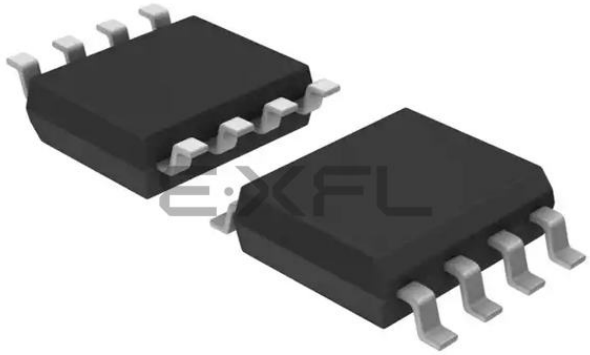

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0413sb005sg

- 2.7V to 3.6V operating voltage
- Up to thirteen 5V-tolerant input pins
- 8-, 20-, and 28-pin packages
- 0°C to +70°C and –40°C to +105°C for operating temperature ranges

Part Selection Guide

Table 1 lists the basic features and package styles available for each device within the Z8 Encore! XP® F0823 Series product line.

Table 1. F0823 Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	I/O	ADC Inputs	Packages
Z8F0823	8	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0813	8	1024	6–24	0	8-, 20-, and 28-pins
Z8F0423	4	1024	6–22	4–8	8-, 20-, and 28-pins
Z8F0413	4	1024	6–24	0	8-, 20-, and 28-pins
Z8F0223	2	512	6–22	4–8	8-, 20-, and 28-pins
Z8F0213	2	512	6–24	0	8-, 20-, and 28-pins
Z8F0123	1	256	6–22	4–8	8-, 20-, and 28-pins
Z8F0113	1	256	6–24	0	8-, 20-, and 28-pins

Architecture

Figure 7 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.

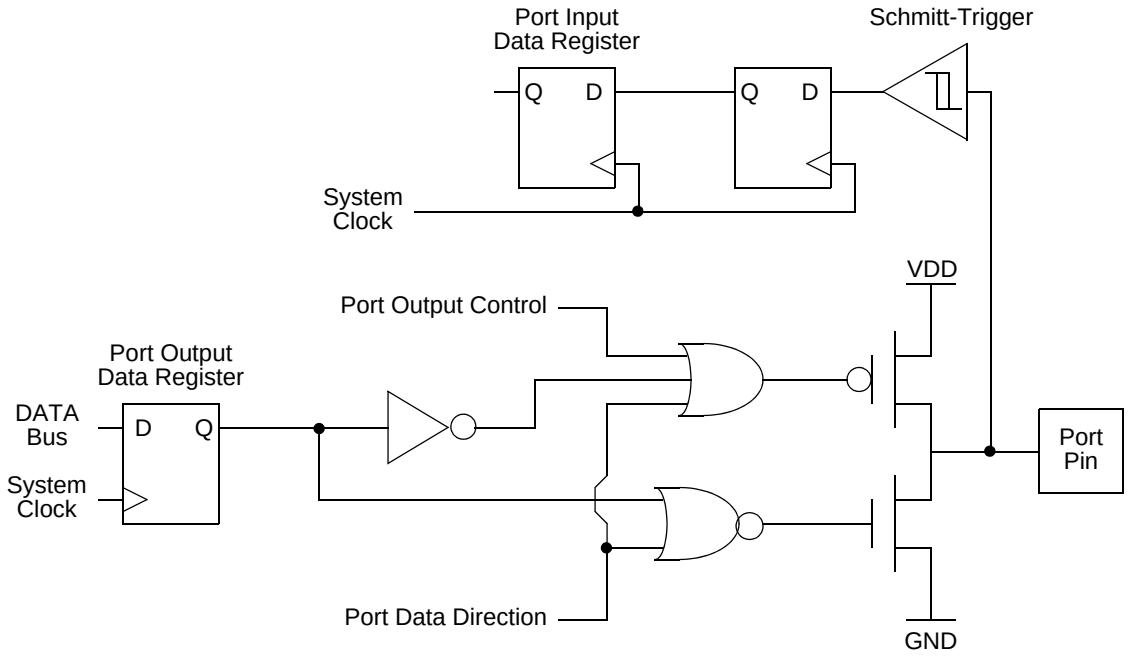


Figure 7. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins are used for general-purpose I/O and access to on-chip peripheral functions such as the timers and serial communication devices. The port A–D Alternate Function subregisters configure these pins for either GPIO or alternate function operation. When a pin is configured for alternate function, control of the port pin direction (input/output) is passed from the Port A–D Data Direction registers to the alternate function assigned to this pin. Tables 16 and 17 list the alternate functions possible with each port pin for 8-pin and non-8-pin parts, respectively. The alternate function associated at a pin is defined through Alternate Function Sets subregisters AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, those pins function as input and output for the crystal oscillator.

- Execution of an Return from Interrupt (IRET) instruction
- Writing a 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a Trap instruction
- Illegal Instruction Trap
- Primary Oscillator Fail Trap
- Watchdog Timer Oscillator Fail Trap

Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all interrupts are enabled with identical interrupt priority (for example, all as Level 2 interrupts), the interrupt priority is assigned from highest to lowest as specified in Table 35 on page 55. Level 3 interrupts are always assigned higher priority than Level 2 interrupts which, in turn, always are assigned higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2 or Level 3), priority is assigned as specified in Table 35. Reset, Watchdog Timer interrupt (if enabled), Primary Oscillator Fail Trap, Watchdog Timer Oscillator Fail Trap, and Illegal Instruction Trap always have highest (Level 3) priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.

! **Caution:** Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) register (Table 49) determines the source of the PADxS interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Table 49. Shared Interrupt Select Register (IRQSS)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PA6CS	Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCEH							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] PA6CS	**PA6/Comparator Selection** 0 = PA6 is used for the interrupt for PA6CS interrupt request. 1 = The comparator is used as an interrupt for PA6CS interrupt requests.
[5:0]	**Reserved** These bits are reserved and must be programmed to 000000.

– Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin

6. Check the TDRE bit in the UART Status 0 Register to determine if the Transmit Data Register is empty (indicated by a 1). If empty, continue to Step 7. If the Transmit Data Register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data Register becomes available to receive new data.
7. Write the UART Control 1 Register to select the outgoing address bit.
8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
9. Write the data byte to the UART Transmit Data Register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR Mode is enabled,.
11. To transmit additional bytes, return to Step 5.

Transmitting Data Using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data Register to accept new data for transmission. Observe the following steps to configure the UART for interrupt-driven data transmission:

1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
5. Write to the UART Control 1 Register to enable MULTIPROCESSOR (9-bit) Mode functions, if MULTIPROCESSOR Mode is appropriate.
6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.
7. Write to the UART Control 0 Register to:
   – Set the transmit enable bit (TEN) to enable the UART for data transmission.
   – Enable parity, if appropriate and if MULTIPROCESSOR Mode is not enabled, and select either even or odd parity.

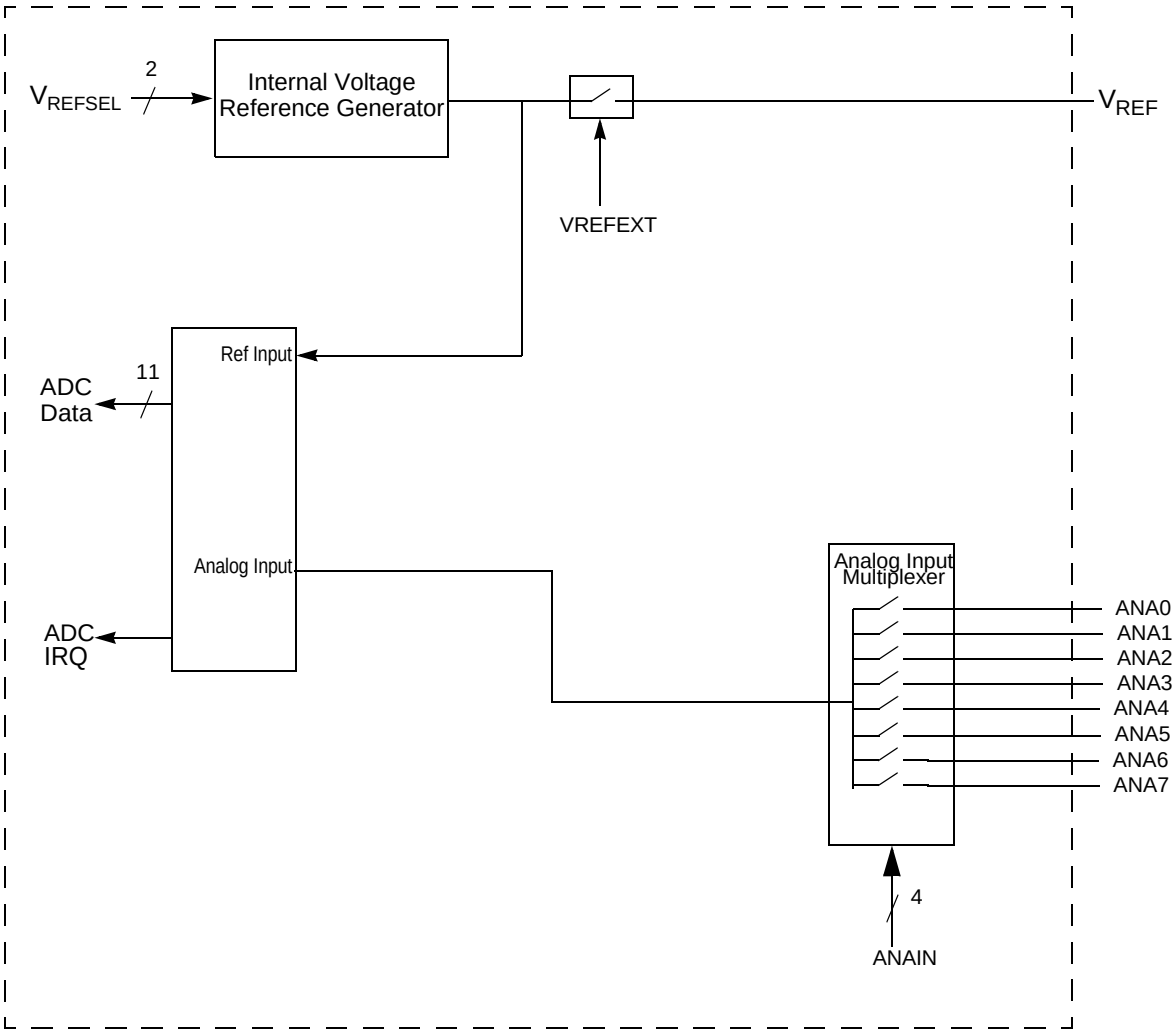


Figure 19. Analog-to-Digital Converter Block Diagram

Operation

The output of the ADC is an 11-bit, signed, two's-complement digital value. The output generally ranges from 0 to +1023, but offset errors can cause small negative values.

The ADC registers return 13 bits of data, but the two LSBs are intended for compensation use only. When the compensation routine is performed on the 13 bit raw ADC value, two bits of resolution are lost because of a rounding error. As a result, the final value is an 11-bit number.

ADC Control/Status Register 1

The second ADC Control Register contains the voltage reference level selection bit.

Table 75. ADC Control/Status Register 1 (ADCCTL1)

Bit	7	6	5	4	3	2	1	0
Field	REFSELH	Reserved						
RESET	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F71H							

Bit	Description
[7] REFSELH	**Voltage Reference Level Select High Bit** In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this bit determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference. 00 = Internal Reference Disabled, reference comes from external pin. 01 = Internal Reference set to 1.0V. 10 = Internal Reference set to 2.0V (default).
[6:0]	**Reserved** These bits are reserved and must be programmed to 0000000.

Bit	Description
[7:5]	**Reserved** These bits are reserved and must be programmed to 111 during writes and to 111 when read.
[4] XTLDIS	**State of Crystal Oscillator at Reset** This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually. 0 = The crystal oscillator is enabled during reset, resulting in longer reset timing. 1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing. **Caution:** Programming the XTLDIS bit to zero on 8-pin versions of F0823 Series devices prevents any further communication via the debug pin due to the X_{IN} and DBG functions being shared on pin 2 of the 8-pin package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.
[3:0]	**Reserved** These bits are reserved and must be programmed to 1111 during writes and to 1111 when read.

Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 91 through 93.

Table 91. Trim Options Bits at Address 0000H

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0020H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	**Reserved** These bits are reserved. Altering this register may result in incorrect device operation.

bits), framed between High bits. The auto-baud detector measures this period and sets the OCD baud rate generator accordingly.

The auto-baud detector/generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by eight. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by four, but this theoretical maximum is possible only for low noise designs with clean signals. Table 100 lists minimum and recommended maximum baud rates for sample crystal frequencies.

Table 100. OCD Baud-Rate Limits

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (kbps)	Recommended Standard PC Baud Rate (bps)	Minimum Baud Rate (kbps)
5.5296	1382.4	691,200	1.08
0.032768 (32kHz)	4.096	2400	0.064

If the OCD receives a Serial Break (nine or more continuous bits Low) the auto-baud detector/generator resets. Reconfigure the auto-baud detector/generator by sending 80H.

OCD Serial Errors

The OCD detects any of the following error conditions on the DBG pin:

- Serial Break (a minimum of nine continuous bits Low)
- Framing Error (received Stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a four character long Serial Break back to the host, and resets the auto-baud detector/generator. A Framing Error or Transmit Collision may be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to the F0823 Series devices or when recovering from an error. A Serial Break from the host resets the auto-baud generator/detector but does not reset the OCD Control Register. A Serial Break leaves the device in DEBUG Mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns High. Because of the open-drain nature of the DBG pin, the host sends a Serial Break to the OCD even if the OCD is transmitting a character.

Stuff Instruction (11H). The Stuff command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

Execute Instruction (12H). The Execute command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.

```
DBG ← 12H
DBG ← 1–5 byte opcode
```

On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

OCD Control Register

The OCD Control Register controls the state of the OCD. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It also resets Z8 Encore! XP F0823 Series device.

A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
BTJNZ bit, src, dst	if src[bit] = 1 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
BTJZ bit, src, dst	if src[bit] = 0 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
CALL dst	SP ← SP –2 @SP ← PC PC ← dst	IRR		D4	–	–	–	–	–	–	2	6
		DA		D6							3	3
CCF	C ← ~C			EF	*	–	–	–	–	–-	1	2
CLR dst	dst ← 00H	R		B0	–	–	–	–	–	–	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	–	*	*	0	–	–	2	2
		IR		61							2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	–	–	2	3
		r	Ir	A3							2	4
		R	R	A4							3	3
		R	IR	A5							3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	–	–	3	3
		r	Ir	1F A3							3	4
		R	R	1F A4							4	3
		R	IR	1F A5							4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	–	–	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	–	–	4	3
		ER	IM	A9							4	3

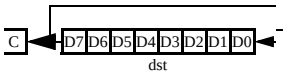
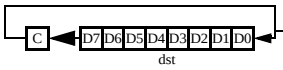
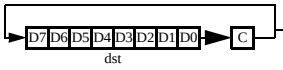
Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
LDX dst, src	dst ← src	r	ER	84	–	–	–	–	–	–	3	2
		Ir	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	Ir	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	dst ← src + X	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	–	–	–	–	–	–	3	2
RCF	C ← 0			CF	0	–	–	–	–	–	1	2
RET	PC ← @SP SP ← SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	–	–	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	–	–	2	2
		IR		C1							2	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

DC Characteristics

Table 121 lists the DC characteristics of the Z8 Encore! XP F0823 Series products. All voltages are referenced to V_{SS}, the primary system ground.

Table 121. DC Characteristics

		T_A = –40°C to +105°C (unless otherwise specified)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
V_{DD}	Supply Voltage	2.7	–	3.6	V	
V_{IL1}	Low Level Input Voltage	–0.3	–	0.3*V_{DD}	V	
V_{IH1}	High Level Input Voltage	0.7*V_{DD}	–	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.
V_{IH2}	High Level Input Voltage	0.7*V_{DD}	–	V_{DD}+0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.
V_{OL1}	Low Level Output Voltage	–	–	0.4	V	I_{OL} = 2mA; V_{DD} = 3.0V High Output Drive disabled.
V_{OH1}	High Level Output Voltage	2.4	–	–	V	I_{OH} = –2mA; V_{DD} = 3.0V High Output Drive disabled.
V_{OL2}	Low Level Output Voltage	–	–	0.6	V	I_{OL} = 20mA; V_{DD} = 3.3 V High Output Drive enabled.
V_{OH2}	High Level Output Voltage	2.4	–	–	V	I_{OH} = –20mA; V_{DD} = 3.3 V High Output Drive enabled.
I_{IH}	Input Leakage Current	–	±0.002	±5	µA	V_{IN} = V_{DD} V_{DD} = 3.3 V
I_{IL}	Input Leakage Current	–	±0.007	±5	µA	V_{IN} = V_{SS} V_{DD} = 3.3 V
I_{TL}	Tristate Leakage Current	–	–	±5	µA	

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.

Table 126. Flash Memory Electrical Characteristics and Timing

	V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C (unless otherwise stated)				
Parameter	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
Flash Byte Read Time	100	–	–	ns	
Flash Byte Program Time	20	–	40	µs	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance	10,000	–	–	cycles	Program/erase cycles

Table 127. Watchdog Timer Electrical Characteristics and Timing

		V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
F_{WDT}	WDT Oscillator Frequency		10		kHz	
F_{WDT}	WDT Oscillator Error			±50	%	
$T_{WDT-CAL}$	WDT Calibrated Timeout	0.98	1	1.02	s	V_{DD} = 3.3 V; T_A = 30°C
		0.70	1	1.30	s	V_{DD} = 2.7V to 3.6V T_A = 0°C to 70°C
		0.50	1	1.50	s	V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C

Table 128. Analog-to-Digital Converter Electrical Characteristics and Timing

		V_{DD} = 3.0V to 3.6V T_A = 0°C to +70°C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
	Resolution	10		–	bits	
	Differential Nonlinearity (DNL)	–1.0	–	1.0	LSB[3]	External V_{REF} = 2.0V; $R_S \leftarrow$ 3.0 kΩ
	Integral Nonlinearity (INL)	–3.0	–	3.0	LSB[3]	External V_{REF} = 2.0V; $R_S \leftarrow$ 3.0 kΩ
	Offset Error with Calibration		±1		LSB[3]	
	Absolute Accuracy with Calibration		±3		LSB[3]	
V_{REF}	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
V_{REF}	Internal Reference Variation with Temperature		±1.0		%	Temperature variation with V_{DD} = 3.0
V_{REF}	Internal Reference Voltage Variation with V_{DD}		±0.5		%	Supply voltage variation with T_A = 30°C
R_{REFOUT}	Reference Buffer Output Impedance		850		W	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement
	Continuous Conversion Time	–	256	–	System clock cycles	All measurements but temperature sensor
			512			Temperature sensor measurement

Notes:
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at V_{DD} = 3.3 V and T_A = +30°C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

Table 128. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD} = 3.0V to 3.6V T_A = 0°C to +70°C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
	Signal Input Bandwidth	–	10		kHz	As defined by –3 dB point
R_S	Analog Source Impedance[4]	–	–	10	kW	In unbuffered mode
Zin	Input Impedance	–	150		kW	In unbuffered mode at 20MHz[5]
Vin	Input Voltage Range	0		V_{DD}	V	Unbuffered Mode

Notes:
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at V_{DD} = 3.3 V and T_A = +30°C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

Table 129. Comparator Electrical Characteristics

		V_{DD} = 2.7V to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
V_{OS}	Input DC Offset		5		mV	
V_{CREF}	Programmable Internal Reference Voltage		±5		%	20-/28-pin devices
			±3		%	8-pin devices
T_{PROP}	Propagation Delay		200		ns	
V_{HYS}	Input Hysteresis		4		mV	
V_{IN}	Input Voltage Range	V_{SS}		V_{DD}–1	V	

General Purpose I/O Port Input Data Sample Timing

Figure 29 displays a timing sequence for the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is

General Purpose I/O Port Output Timing

Figure 30 and Table 131 provide timing information for GPIO Port pins.

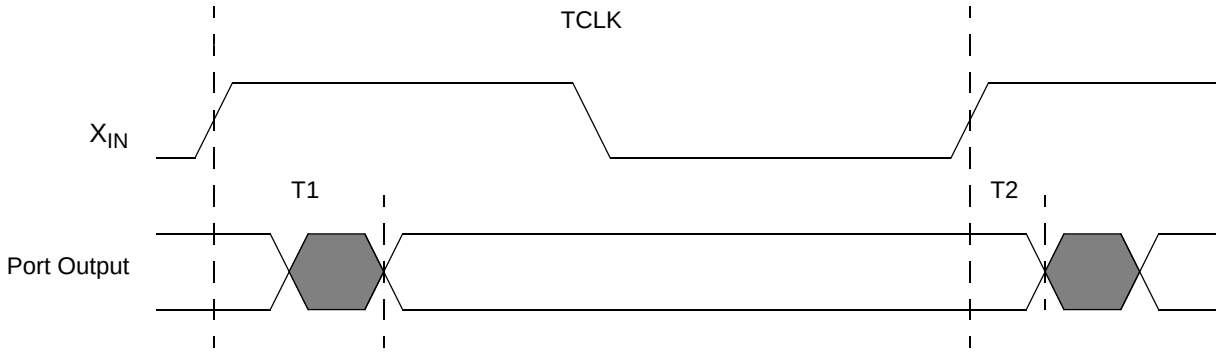


Figure 30. GPIO Port Output Timing

Table 131. GPIO Port Output Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
GPIO Port pins			
T_1	X_{IN} Rise to Port Output Valid Delay	–	15
T_2	X_{IN} Rise to Port Output Hold Time	2	–

Ordering Information

Order your F0823 Series products from Zilog using the part numbers shown in Table 135. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 8 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0°C to 70°C								
Z8F0823PB005SG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005SG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005SG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005SG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005SG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005SG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005SG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005SG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005SG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: –40°C to 105°C								
Z8F0823PB005EG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005EG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005EG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005EG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005EG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005EG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005EG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005EG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005EG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0°C to 70°C								
Z8F0423PB005SG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005SG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005SG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005SG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005SG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005SG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005SG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005SG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005SG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: –40°C to 105°C								
Z8F0423PB005EG	4 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0423QB005EG	4 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0423SB005EG	4 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0423SH005EG	4 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0423HH005EG	4 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0423PH005EG	4 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0423SJ005EG	4 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0423HJ005EG	4 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0423PJ005EG	4 KB	1 KB	22	18	2	8	1	PDIP 28-pin package