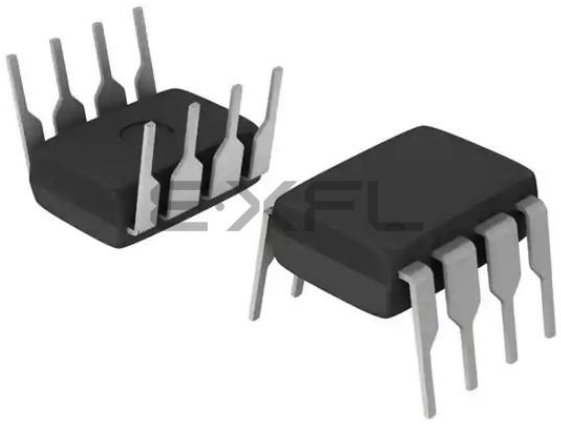

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 5MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 6 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0423pb005eg |

**Table 3. Signal Descriptions (Continued)**

| Signal Mnemonic | I/O | Description |
|---|---|---|
| COUT | O | Comparator Output. This is the output of the comparator. |
| **Analog** | | |
| ANA[7:0] | I | Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier. |
| VREF | I/O | Analog-to-Digital Converter reference voltage input. |
| **Clock Input** | | |
| CLKIN | I | Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock. |
| **LED Drivers** | | |
| LED | O | Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block. |
| **On-Chip Debugger** | | |
| DBG | I/O | Debug. This signal is the control and data input and output to and from the OCD.<br>**Caution:** The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation. |
| **Reset** | | |
| $\overline{\text{RESET}}$ | I/O | RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor. |
| **Power Supply** | | |
| $V_{DD}$ | I | Digital Power Supply. |
| $AV_{DD}$[2] | I | Analog Power Supply. |
| $V_{SS}$ | I | Digital Ground. |
| $AV_{SS}$ | I | Analog Ground. |

Notes:
1. PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by $AV_{DD}$ and $AV_{SS}$.
2. The $AV_{DD}$ and $AV_{SS}$ signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

**Note:** This register is only reset during a Power-On Reset sequence. Other System Reset events do not affect it.

**Table 14. Power Control Register 0 (PWRCTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | Reserved | | VBO | Reserved | ADC | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F80H | | | | | | | |

| Bit | Description |
|---|---|
| [7] | **Reserved**<br>This bit is reserved and must be programmed to 1. |
| [6:5] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [4]<br>VBO | **Voltage Brown-Out Detector Disable**<br>This bit and the VBO_AO Flash option bit must both enable the VBO for the VBO to be active.<br>0 = VBO enabled.<br>1 = VBO disabled. |
| [3] | **Reserved**<br>This bit is reserved and must be programmed to 0. |
| [2]<br>ADC | **Analog-to-Digital Converter Disable**<br>0 = Analog-to-Digital Converter enabled.<br>1 = Analog-to-Digital Converter disabled. |
| [1]<br>COMP | **Comparator Disable**<br>0 = Comparator is enabled.<br>1 = Comparator is disabled. |
| [0] | **Reserved**<br>This bit is reserved and must be programmed to 0. |

PA0 and PA6 contain two different timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the timer mode. For more details, see the Timers chapter on page 69.

**Caution:** For pins with multiple alternate functions, Zilog recommends writing to the AFS1 and AFS2 subregisters before enabling the alternate function via the AF Subregister. This prevents spurious transitions through unwanted alternate function modes.

**Table 16. Port Alternate Function Mapping (8-Pin Parts)**

| Port | Pin | Mnemonic | Alternate Function Description | Alternate Function Select Register AFS1 | Alternate Function Select Register AFS2 |
|---|---|---|---|---|---|
| **Port A** | PA0 | T0IN | Timer 0 Input | AFS1[0]: 0 | AFS2[0]: 0 |
| | | Reserved | | AFS1[0]: 0 | AFS2[0]: 1 |
| | | Reserved | | AFS1[0]: 1 | AFS2[0]: 0 |
| | | T0OUT | Timer 0 Output Complement | AFS1[0]: 1 | AFS2[0]: 1 |
| | PA1 | T0OUT | Timer 0 Output | AFS1[1]: 0 | AFS2[1]: 0 |
| | | Reserved | | AFS1[1]: 0 | AFS2[1]: 1 |
| | | CLKIN | External Clock Input | AFS1[1]: 1 | AFS2[1]: 0 |
| | | Analog Functions* | ADC Analog Input/$V_{REF}$ | AFS1[1]: 1 | AFS2[1]: 1 |
| | PA2 | $\overline{DE0}$ | UART 0 Driver Enable | AFS1[2]: 0 | AFS2[2]: 0 |
| | | RESET | External Reset | AFS1[2]: 0 | AFS2[2]: 1 |
| | | T1OUT | Timer 1 Output | AFS1[2]: 1 | AFS2[2]: 0 |
| | | Reserved | | AFS1[2]: 1 | AFS2[2]: 1 |
| | PA3 | $\overline{CTS0}$ | UART 0 Clear to Send | AFS1[3]: 0 | AFS2[3]: 0 |
| | | COUT | Comparator Output | AFS1[3]: 0 | AFS2[3]: 1 |
| | | T1IN | Timer 1 Input | AFS1[3]: 1 | AFS2[3]: 0 |
| | | Analog Functions* | ADC Analog Input | AFS1[3]: 1 | AFS2[3]: 1 |
| | PA4 | RXD0 | UART 0 Receive Data | AFS1[4]: 0 | AFS2[4]: 0 |
| | | Reserved | | AFS1[4]: 0 | AFS2[4]: 1 |
| | | Reserved | | AFS1[4]: 1 | AFS2[4]: 0 |
| | | Analog Functions* | ADC/Comparator Input (N) | AFS1[4]: 1 | AFS2[4]: 1 |
| | PA5 | TXD0 | UART 0 Transmit Data | AFS1[5]: 0 | AFS2[5]: 0 |
| | | T1OUT | Timer 1 Output Complement | AFS1[5]: 0 | AFS2[5]: 1 |
| | | Reserved | | AFS1[5]: 1 | AFS2[5]: 0 |
| | | Analog Functions* | ADC/Comparator Input (P) | AFS1[5]: 1 | AFS2[5]: 1 |

Note: *Analog Functions include ADC inputs, ADC reference and comparator inputs. Also, alternate function selection as described in the Port A–C Alternate Function Subregisters section on page 43 must be enabled.

For correct operation, the LED anode must be connected to $V_{DD}$ and the cathode must be connected to the GPIO pin. Using all Port C pins in LED Drive Mode with maximum current can result in excessive total current. For the maximum total current for the applicable package, see the Electrical Characteristics chapter on page 196.

## Shared Reset Pin

On the 8-pin product versions, the reset pin is shared with PA2, but the pin is not limited to output-only when in GPIO Mode.

**Caution:** If PA2 on the 8-pin product is reconfigured as an input, ensure that no external stimulus drives the pin Low during any reset sequence. Because PA2 returns to its RESET alternate function during system resets, driving it Low holds the chip in a reset state until the pin is released.

## Shared Debug Pin

On the 8-pin version of this device only, the Debug pin shares function with the PA0 GPIO pin. This pin performs as a general purpose input pin on power-up, but the debug logic monitors this pin during the reset sequence to determine if the unlock sequence occurs. If the unlock sequence is present, the debug function is unlocked and the pin no longer functions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see the On-Chip Debugger chapter on page 156.

## Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see the Oscillator Control Register Definitions section on page 171), the GPIO settings are overridden and PA0 and PA1 are disabled.

## 5V Tolerance

All six I/O pins on the 8-pin devices are 5V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than $V_{DD}$ are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

**Note:** In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5V-tolerant, including PA[1:0], PB[5:0], and

**Table 18. GPIO Port Registers and Subregisters (Continued)**

| Port Register Mnemonic | Port Register Name |
|---|---|
| P*x*HDE | High Drive Enable. |
| P*x*SMRE | Stop Mode Recovery Source Enable. |
| P*x*PUE | Pull-up Enable. |
| PxAFS1 | Alternate Function Set 1. |
| PxAFS2 | Alternate Function Set 2. |

## Port A–C Address Registers

The Port A–C Address registers select the GPIO port functionality accessible through the Port A–C Control registers. The Port A–C Address and Control registers combine to provide access to all GPIO port controls (Table 19).

**Table 19. Port A–C GPIO Address Registers (P*x*ADDR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PADDR[7:0] | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FD0H, FD4H, FD8H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] PADDR | **Port Address**<br>The Port Address selects one of the subregisters accessible through the Port Control Register. See Table 20 for each subregister function. |

**Table 20. PADDR[7:0] Subregister Functions**

| PADDR[7:0] | Port Control Subregister Accessible Using the Port A–C Control Registers |
|---|---|
| 00H | No function. Provides some protection against accidental Port reconfiguration. |
| 01H | Data Direction. |
| 02H | Alternate Function. |
| 03H | Output Control (Open-Drain). |
| 04H | High Drive Enable. |

| Bit | Description (Continued) |
|---|---|
| [4]<br>U0RXI | **UART 0 Receiver Interrupt Request**<br>0 = No interrupt request is pending for the UART 0 receiver.<br>1 = An interrupt request from the UART 0 receiver is awaiting service. |
| [3]<br>U0TXI | **UART 0 Transmitter Interrupt Request**<br>0 = No interrupt request is pending for the UART 0 transmitter.<br>1 = An interrupt request from the UART 0 transmitter is awaiting service. |
| [2:1] | **Reserved**<br>These bits are reserved and must be programmed to 00. |
| [0]<br>ADCI | **ADC Interrupt Request**<br>0 = No interrupt request is pending for the ADC.<br>1 = An interrupt request from the ADC is awaiting service. |

## Interrupt Request 1 Register

The Interrupt Request 1 (IRQ1) register (Table 37) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ1 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU reads the Interrupt Request 1 Register to determine if any interrupt requests are pending.

**Table 37. Interrupt Request 1 Register (IRQ1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PA7VI | PA6CI | PA5I | PA4I | PA3I | PA2I | PA1I | PA0I |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC3H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>PA7VI | **Port A7 Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port A.<br>1 = An interrupt request from GPIO Port A. |
| [6]<br>PA6CI | **Port A6 or Comparator Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port A or Comparator.<br>1 = An interrupt request from GPIO Port A or Comparator. |
| [5:0]<br>PAxI | **Port A Pin *x* Interrupt Request**<br>0 = No interrupt request is pending for GPIO Port A pin *x*.<br>1 = An interrupt request from GPIO Port A pin *x* is awaiting service. |

Note: x indicates the specific GPIO Port pin number (0–5).

## IRQ2 Enable High and Low Bit Registers

Table 45 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers (Table 46 and Table 47) form a priority encoded enabling for interrupts in the Interrupt Request 2 register. Priority is generated by setting bits in each register.

**Table 45. IRQ2 Enable and Priority Encoding**

| IRQ2ENH[*x*] | IRQ2ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Nominal |
| 1 | 1 | Level 3 | High |

Note: where *x* indicates the register bits from 0–7.

**Table 46. IRQ2 Enable High Bit Register (IRQ2ENH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | C3ENH | C2ENH | C1ENH | C0ENH |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC7H | | | | | | | |

| Bit | Description |
|---|---|
| [7:4] | **Reserved**<br>These bits are reserved and must be programmed to 0000. |
| [3]<br>C3ENH | **Port C3 Interrupt Request Enable High Bit** |
| [2]<br>C2ENH | **Port C2 Interrupt Request Enable High Bit** |
| [1]<br>C1ENH | **Port C1 Interrupt Request Enable High Bit** |
| [0]<br>C0ENH | **Port C0 Interrupt Request Enable High Bit** |

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first PWM time-out period. If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

## PWM Dual Output Mode

In PWM DUAL OUTPUT Mode, the timer outputs a PWM output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

## Watchdog Timer Refresh

When first enabled, the WDT is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the down counter to be reloaded with the WDT reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When Z8 Encore! XP F0823 Series devices are operating in DEBUG Mode (using the OCD), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

## Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT_RES Flash Option Bit determines the time-out response of the Watchdog Timer. For information about programming of the WDT_RES Flash Option Bit, see **the** Flash Option Bits chapter on page 146.

### WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watchdog Timer Control Register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

The Reset Status Register (see the Reset Status Register section on page 28) must be read before clearing the WDT interrupt. This read clears the WDT time-out Flag and prevents further WDT interrupts for immediately occurring.

### WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and F0823 Series are in STOP Mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watchdog Timer Control Register are set to 1 following a WDT time-out in STOP Mode. For more information about Stop Mode Recovery, see **the** Reset and Stop Mode Recovery chapter on page 21.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

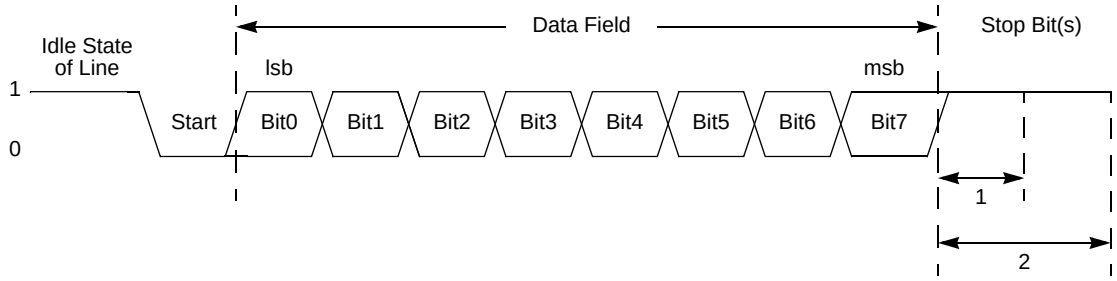


**Figure 11. UART Asynchronous Data Format without Parity**

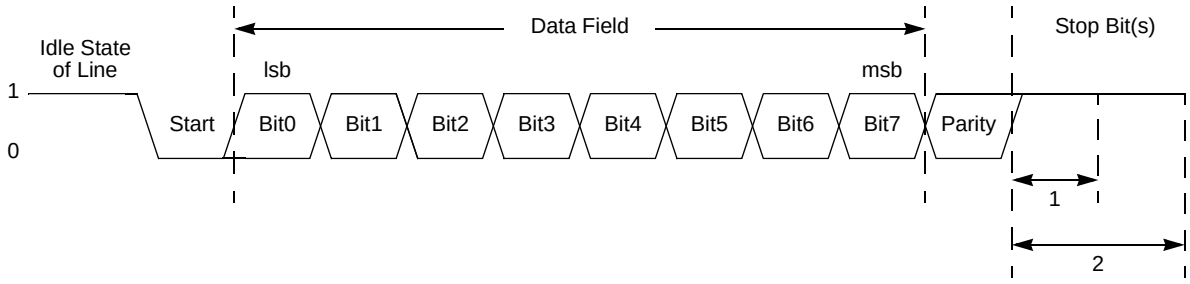


**Figure 12. UART Asynchronous Data Format with Parity**

## Transmitting Data Using the Polled Method

Observe the following steps to transmit data using the polled method of operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Write to the UART Control 1 Register, if MULTIPROCESSOR Mode is appropriate, to enable MULTIPROCESSOR (9-bit) Mode functions.
4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR Mode.
5. Write to the UART Control 0 Register to:
   - Set the transmit enable bit (TEN) to enable the UART for data transmission
   - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR Mode is not enabled, and select either even or odd parity (PSEL)

## Receiving IrDA Data

Data received from the infrared transceiver using the IR_RXD signal through the RXD pin is decoded by the infrared endec and passed to the UART. The UART's baud rate clock is used by the infrared endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 18 displays data reception. When the infrared endec is enabled, the UART's RXD signal is internal to the Z8 Encore! XP F0823 Series products while the IR_RXD signal is received through the RXD pin.

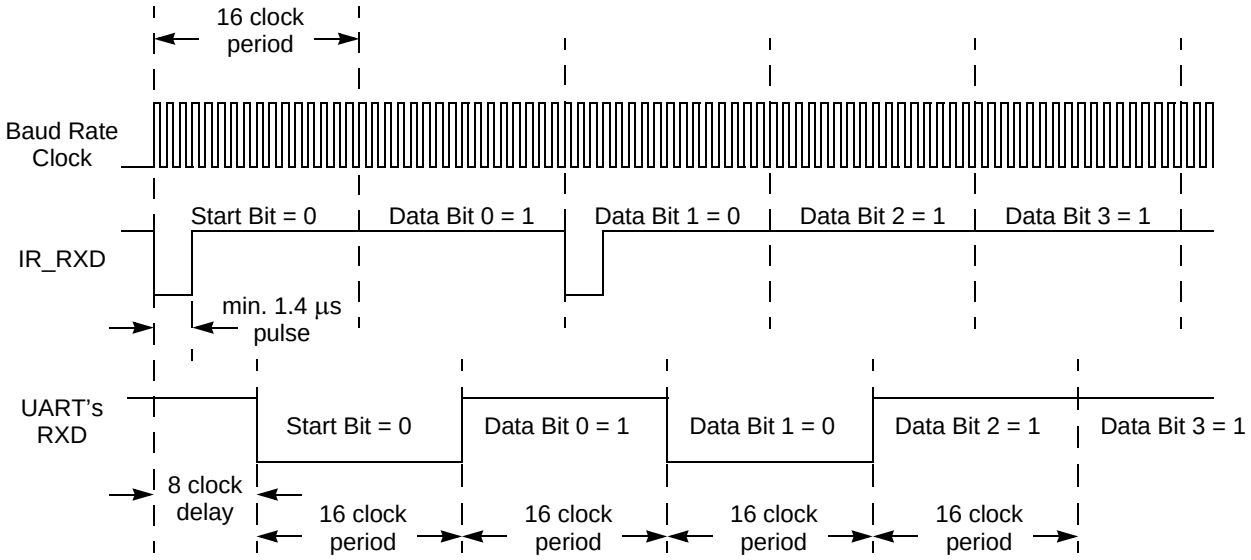


**Figure 18. IrDA Data Reception**

### Infrared Data Reception

**Caution:** The system clock frequency must be at least 1.0MHz to ensure proper reception of the 1.4µs minimum width pulses allowed by the IrDA standard.

### Endec Receiver Synchronization

The IrDA receiver uses a local baud rate clock counter (0 to 15 clock periods) to generate an input stream for the UART and to create a sampling window for detection of incoming pulses. The generated UART input (UART RXD) is delayed by 8 baud rate clock periods with respect to the incoming IrDA data stream. When a falling edge in the input data stream is detected, the endec counter is reset. When the count reaches a value of 8, the UART RXD value is updated to reflect the value of the decoded data. When the count reaches 12 baud clock periods, the sampling window for the next incoming pulse opens.

## ADC Control/Status Register 1

The second ADC Control Register contains the voltage reference level selection bit.

**Table 75. ADC Control/Status Register 1 (ADCCTL1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | REFSELH | Reserved | | | | | | |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F71H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>REFSELH | **Voltage Reference Level Select High Bit**<br>In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this bit determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference.<br>00 = Internal Reference Disabled, reference comes from external pin.<br>01 = Internal Reference set to 1.0V.<br>10 = Internal Reference set to 2.0V (default). |
| [6:0] | **Reserved**<br>These bits are reserved and must be programmed to 0000000. |

These serial numbers are stored in the Flash information page (for more details, see the Reading the Flash Information Page section on page 148 and the Serialization Data section on page 154) and are unaffected by mass erasure of the device's Flash memory.

### Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

The randomized lot identifier is a 32-byte binary value, stored in the flash information page (for more details, see the Reading the Flash Information Page section on page 148 and the Randomized Lot Identifier section on page 154) and is unaffected by mass erasure of the device's flash memory.

## Reading the Flash Information Page

The following code example shows how to read data from the Flash Information Area.

```
; get value at info address 60 (FE60h)
ldx FPS, #%80 ; enable access to flash info page
ld R0, #%FE
ld R1, #%60
ldc R2, @RR0 ; R2 now contains the calibration value
```

# Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

## Trim Bit Address Register

The Trim Bit Address (TRMADR) Register contains the target address for an access to the trim option bits.

**Table 87. Trim Bit Address Register (TRMADR)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRMADR: Trim Bit Address (00H to 1FH) | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF6H | | | | | | | |

## Serialization Data

**Table 96. Serial Number at 001C–001F (S_NUM)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | S_NUM | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Information Page Memory 001C–001F | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7:0]<br>S_NUM | **Serial Number Byte**<br>The serial number is a unique four-byte binary value; see Table 97. |

**Table 97. Serialization Data Locations**

| Info Page Address | Memory Address | Usage |
|---|---|---|
| 1C | FE1C | Serial Number Byte 3 (most significant). |
| 1D | FE1D | Serial Number Byte 2. |
| 1E | FE1E | Serial Number Byte 1. |
| 1F | FE1F | Serial Number Byte 0 (least significant). |

## Randomized Lot Identifier

**Table 98. Lot Identification Number (RAND_LOT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RAND_LOT | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Interspersed throughout Information Page Memory | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

| Bit | Description |
|---|---|
| [7]<br>RAND_LOT | **Randomized Lot ID**<br>The randomized lot ID is a 32-byte binary value that changes for each production lot; see Table 99. |

# eZ8 CPU Instruction Classes

eZ8 CPU instructions are divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift

Tables 110 through 117 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction can be considered as a subset of more than one category. Within these tables, the source operand is identified as ‘src’, the destination operand is ‘dst’ and a condition code is ‘cc’.

**Table 110. Arithmetic Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| ADC | dst, src | Add with Carry |
| ADCX | dst, src | Add with Carry using Extended Addressing |
| ADD | dst, src | Add |
| ADDX | dst, src | Add using Extended Addressing |
| CP | dst, src | Compare |
| CPC | dst, src | Compare with Carry |
| CPCX | dst, src | Compare with Carry using Extended Addressing |
| CPX | dst, src | Compare using Extended Addressing |
| DA | dst | Decimal Adjust |
| DEC | dst | Decrement |
| DECW | dst | Decrement Word |
| INC | dst | Increment |
| INCW | dst | Increment Word |

# On-Chip Peripheral AC and DC Electrical Characteristics

Table 125 tabulates the electrical characteristics of the POR and VBO blocks.

**Table 125. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing**

| | | $T_A$ = –40°C to +105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical*** | **Maximum** | **Units** | **Conditions** |
| $V_{POR}$ | Power-On Reset Voltage Threshold | 2.20 | 2.45 | 2.70 | V | $V_{DD} = V_{POR}$ |
| $V_{VBO}$ | Voltage Brown-Out Reset Voltage Threshold | 2.15 | 2.40 | 2.65 | V | $V_{DD} = V_{VBO}$ |
| | $V_{POR}$ to $V_{VBO}$ hysteresis | | 50 | 75 | mV | |
| | Starting $V_{DD}$ voltage to ensure valid Power-On Reset. | – | $V_{SS}$ | – | V | |
| $T_{ANA}$ | Power-On Reset Analog Delay | – | 70 | – | µs | $V_{DD} > V_{POR}$; $T_{POR}$ Digital Reset delay follows $T_{ANA}$ |
| $T_{POR}$ | Power-On Reset Digital Delay | | 16 | | µs | 66 Internal Precision Oscillator cycles + IPO startup time ($T_{IPOST}$) |
| $T_{SMR}$ | Stop Mode Recovery | | 16 | | µs | 66 Internal Precision Oscillator cycles |
| $T_{VBO}$ | Voltage Brown-Out Pulse Rejection Period | – | 10 | – | µs | Period of time in which $V_{DD} < V_{VBO}$ without generating a Reset. |
| $T_{RAMP}$ | Time for $V_{DD}$ to transition from $V_{SS}$ to $V_{POR}$ to ensure valid Reset | 0.10 | – | 100 | ms | |
| $T_{SMP}$ | Stop Mode Recovery pin pulse rejection period | | 20 | | ns | For any SMR pin or for the Reset pin when it is asserted in STOP Mode. |

Note: *Data in the typical column is from characterization at 3.3 V and 30°C. These values are provided for design guidance only and are not tested in production.

**Table 128. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)**

| | | $V_{DD}$ = 3.0V to 3.6V<br>$T_A$ = 0°C to +70°C<br>(unless otherwise stated) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| | Signal Input Bandwidth | – | 10 | | kHz | As defined by –3 dB point |
| $R_S$ | Analog Source Impedance[4] | – | – | 10 | kW | In unbuffered mode |
| Zin | Input Impedance | – | 150 | | kW | In unbuffered mode at 20MHz[5] |
| Vin | Input Voltage Range | 0 | | $V_{DD}$ | V | Unbuffered Mode |

Notes:
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at $V_{DD}$ = 3.3 V and $T_A$ = +30°C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

**Table 129. Comparator Electrical Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $V_{OS}$ | Input DC Offset | | 5 | | mV | |
| $V_{CREF}$ | Programmable Internal Reference Voltage | | ±5 | | % | 20-/28-pin devices |
| | | | ±3 | | % | 8-pin devices |
| $T_{PROP}$ | Propagation Delay | | 200 | | ns | |
| $V_{HYS}$ | Input Hysteresis | | 4 | | mV | |
| $V_{IN}$ | Input Voltage Range | $V_{SS}$ | | $V_{DD}$–1 | V | |

## General Purpose I/O Port Input Data Sample Timing

Figure 29 displays a timing sequence for the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0423PB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0423QB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0423SB005SG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0423SH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0423HH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0423PH005SG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0423SJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0423HJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0423PJ005SG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0423PB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0423QB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0423SB005EG | 4 KB | 1 KB | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0423SH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0423HH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0423PH005EG | 4 KB | 1 KB | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0423SJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0423HJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0423PJ005EG | 4 KB | 1 KB | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 1 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0123PB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0123QB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0123SB005SG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0123SH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0123HH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0123PH005SG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0123SJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0123HJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0123PJ005SG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0123PB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | PDIP 8-pin package |
| Z8F0123QB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | QFN 8-pin package |
| Z8F0123SB005EG | 1 KB | 256 B | 6 | 12 | 2 | 4 | 1 | SOIC 8-pin package |
| Z8F0123SH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SOIC 20-pin package |
| Z8F0123HH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | SSOP 20-pin package |
| Z8F0123PH005EG | 1 KB | 256 B | 16 | 18 | 2 | 7 | 1 | PDIP 20-pin package |
| Z8F0123SJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SOIC 28-pin package |
| Z8F0123HJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | SSOP 28-pin package |
| Z8F0123PJ005EG | 1 KB | 256 B | 22 | 18 | 2 | 8 | 1 | PDIP 28-pin package |

**Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Description |
|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP F0823 Series with 1 KB Flash** | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | |
| Z8F0113PB005SG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0113QB005SG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0113SB005SG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0113SH005SG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0113HH005SG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0113PH005SG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0113SJ005SG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0113HJ005SG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0113PJ005SG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | |
| Z8F0113PB005EG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | PDIP 8-pin package |
| Z8F0113QB005EG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | QFN 8-pin package |
| Z8F0113SB005EG | 1 KB | 256 B | 6 | 12 | 2 | 0 | 1 | SOIC 8-pin package |
| Z8F0113SH005EG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | SOIC 20-pin package |
| Z8F0113HH005EG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | SSOP 20-pin package |
| Z8F0113PH005EG | 1 KB | 256 B | 16 | 18 | 2 | 0 | 1 | PDIP 20-pin package |
| Z8F0113SJ005EG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | SOIC 28-pin package |
| Z8F0113HJ005EG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | SSOP 28-pin package |
| Z8F0113PJ005EG | 1 KB | 256 B | 24 | 18 | 2 | 0 | 1 | PDIP 28-pin package |