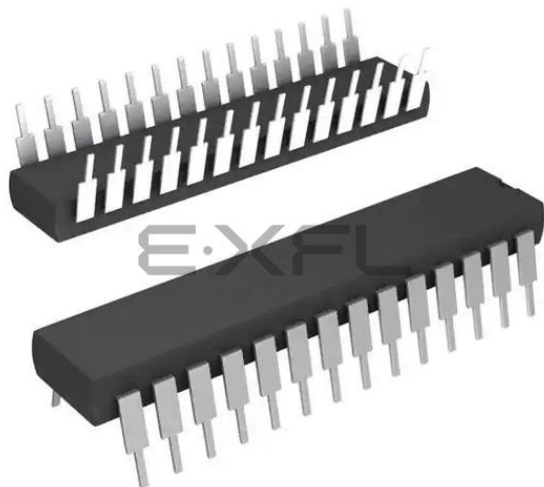




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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0813pj005sg

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Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 8-pin devices.

Table 5. Pin Characteristics (8-Pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull- down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
PA1	I/O	I	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
RESET/PA2	I/O	I/O (defaults to RESET)	N/A	Yes	Program- mable for PA2; always on for RESET	Yes	Programma- ble for PA2; always on for RESET	Yes, unless pull-ups enabled
PA[5:3]	I/O	I	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
VDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
VSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
LED Controller (cont'd)				
F84	LED Drive Level Low Byte	LEDLVLL	00	<u>53</u>
F85	Reserved	—	XX	
Oscillator Control				
F86	Oscillator Control	OSCCTL	A0	<u>172</u>
F87–F8F	Reserved	—	XX	
Comparator 0				
F90	Comparator 0 Control	CMP0	14	<u>133</u>
F91–FBF	Reserved	—	XX	
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	<u>59</u>
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	<u>62</u>
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	<u>62</u>
FC3	Interrupt Request 1	IRQ1	00	<u>60</u>
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	<u>64</u>
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	<u>64</u>
FC6	Interrupt Request 2	IRQ2	00	<u>61</u>
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	<u>65</u>
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	<u>66</u>
FC9–FCC	Reserved	—	XX	
FCD	Interrupt Edge Select	IRQES	00	<u>67</u>
FCE	Shared Interrupt Select	IRQSS	00	<u>67</u>
FCF	Interrupt Control	IRQCTL	00	<u>68</u>
GPIO Port A				
FD0	Port A Address	PAADDR	00	<u>40</u>
FD1	Port A Control	PACTL	00	<u>42</u>
FD2	Port A Input Data	PAIN	XX	<u>43</u>
FD3	Port A Output Data	PAOUT	00	<u>43</u>
GPIO Port B				
FD4	Port B Address	PBADDR	00	<u>40</u>
FD5	Port B Control	PBCTL	00	<u>42</u>

Note: XX=Undefined.

Table 18. GPIO Port Registers and Subregisters (Continued)

Port Register Mnemonic	Port Register Name
PxHDE	High Drive Enable.
PxSMRE	Stop Mode Recovery Source Enable.
PxPUE	Pull-up Enable.
PxAFS1	Alternate Function Set 1.
PxAFS2	Alternate Function Set 2.

Port A–C Address Registers

The Port A–C Address registers select the GPIO port functionality accessible through the Port A–C Control registers. The Port A–C Address and Control registers combine to provide access to all GPIO port controls (Table 19).

Table 19. Port A–C GPIO Address Registers (PxADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD0H, FD4H, FD8H							

Bit	Description
[7:0] PADDR	Port Address The Port Address selects one of the subregisters accessible through the Port Control Register. See Table 20 for each subregister function.

Table 20. PADDR[7:0] Subregister Functions

PADDR[7:0]	Port Control Subregister Accessible Using the Port A–C Control Registers
00H	No function. Provides some protection against accidental Port reconfiguration.
01H	Data Direction.
02H	Alternate Function.
03H	Output Control (Open-Drain).
04H	High Drive Enable.

Port A–C Input Data Registers

Reading from the Port A–C Input Data registers (Table 30) returns the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Table 30. Port A–C Input Data Registers (PxIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD2H, FD6H, FDAH							

Bit	Description
[7:0] PxIN	Port Input Data Sampled data from the corresponding port pin input. 0 = Input data is logical 0 (Low). 1 = Input data is logical 1 (High).

Note: x indicates the specific GPIO port pin number (7–0).

Timers

Z8 Encore! XP F0823 Series products contain up to two 16-bit reloadable timers that are used for timing, event counting or generation of PWM signals. The timers' features include:

- 16-bit reload counter
- Programmable prescaler with prescale values from 1 to 128
- PWM output generation
- Capture and compare capability
- External input pin for timer input, clock gating, or capture signal; external input pin signal frequency is limited to a maximum of one-fourth the system clock frequency
- Timer output pin
- Timer interrupt

In addition to the timers described in this chapter, the baud rate generator of the UART (if unused) also provides basic timing functionality. For information about using the baud rate generator as an additional timer, see the Universal Asynchronous Receiver/Transmitter chapter on page 97.

Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which can place Z8 Encore! XP F0823 Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

Operation

The WDT is a retriggerable one-shot timer that resets or interrupts F0823 Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash Option Bit. The WDT_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable down counter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTM[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10 kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 59 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

Table 59. Watchdog Timer Approximate Time-Out Delays

WDT Reload Value (Hex)	WDT Reload Value (Decimal)	Approximate Time-Out Delay (with 10 kHz typical WDT oscillator frequency)	
		Typical	Description
000004	4	400 μs	Minimum time-out delay
FFFFFF	16,777,215	28 minutes	Maximum time-out delay

Watchdog Timer Reload High Byte Register (WDTH): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 95

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the Reload registers.

This register address is shared with the read-only Reset Status Register.

Table 60. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Bit	Description
[7:0]	Watchdog Timer Unlock
WDTUNLK	The software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer reload registers.

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 61 through 63, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate Reload Value. Reading from these registers returns the current Watchdog Timer count value.

! **Caution:** The 24-bit WDT Reload Value must not be set to a value less than 000004H.

Table 61. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF1H							
Note: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

Bit	Description
[7:0] WDTU	WDT Reload Upper Byte Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 62. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	04H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF2H							
Note: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

Bit	Description
[7:0] WDTH	WDT Reload High Byte Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 63. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	00H							
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF3H							
Note: R/W*—Read returns the current WDT count value. Write sets the appropriate Reload Value.								

Flash Status Register

The Flash Status Register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the write-only Flash Control Register.

Table 82. Flash Status Register (FSTAT)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		FSTAT					
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	FF8H							

Bit	Description
[7:6]	Reserved These bits are reserved and must be programmed to 0 when read.
[5:0] FSTAT	Flash Controller Status 000000 = Flash Controller locked. 000001 = First unlock command received (73H written). 000010 = Second unlock command received (8CH written). 000011 = Flash Controller unlocked. 000100 = Sector protect register selected. 001xxx = Program operation in progress. 010xxx = Page erase operation in progress. 100xxx = Mass erase operation in progress.

Flash Page Select Register

The Flash Page Select (FPS) register shares address space with the Flash Sector Protect Register. Unless the Flash controller is unlocked and written with 5EH, writes to this address target the Flash Page Select Register.

The register is used to select one of the eight available Flash memory pages to be programmed or erased. Each Flash Page contains 512 bytes of Flash memory. During a Page Erase operation, all Flash memory having addresses with the most significant 7-bits given by FPS[6:0] are chosen for program/erase operation.

Table 83. Flash Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF9H							

Bit	Description
[7] INFO_EN	Information Area Enable 0 = Information Area is not selected. 1 = Information Area is selected. The Information Area is mapped into the Program Memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	Page Select This 7-bit field identifies the Flash memory page for Page Erase and page unlocking. • Program Memory Address[15:9] = PAGE[6:0]. • For Z8F04x3 devices, the upper 4 bits must always be 0. • For Z8F02x3 devices, the upper 5 bits must always be 0. • For Z8F01x3 devices, the upper 6 bits must always be 0.

Stuff Instruction (11H). The Stuff command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

DBG ← 11H
DBG ← opcode[7:0]

Execute Instruction (12H). The Execute command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.

DBG ← 12H
DBG ← 1–5 byte opcode

On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

OCD Control Register

The OCD Control Register controls the state of the OCD. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It also resets Z8 Encore! XP F0823 Series device.

A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.

Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a non-standard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency. The features of IPO include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a fast and a slow mode)
- Trimming possible through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

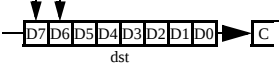
Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53MHz (fast mode) or 32.8kHz (slow mode) is required. This trimming is done at +30°C and a supply voltage of 3.3 V, so accuracy of this operating point is optimal.

Power down this block for minimum system power. By default, the oscillator is configured through the Flash Option bits. However, the user code can override these trim values, as described in the [Trim Bit Address Space](#) section on page 151.

Select one of the two frequencies for the oscillator: 5.53MHz and 32.8kHz, using the OSCSEL bits in the [Oscillator Control](#) chapter on page 169.

Table 118. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
SBC dst, src	$dst \leftarrow dst - src - C$	r	r	32	*	*	*	*	1	*	2	3
		r	lr	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	$dst \leftarrow dst - src - C$	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3
SCF	$C \leftarrow 1$			DF	1	–	–	–	–	–	1	2
SRA dst		R		D0	*	*	*	0	–	–	2	2
		IR		D1							2	3
SRL dst		R		1F C0	*	*	0	*	–	–	3	2
		IR		1F C1							3	3
SRP src	$RP \leftarrow src$		IM	01	–	–	–	–	–	–	2	2
STOP	STOP Mode			6F	–	–	–	–	–	–	1	2
SUB dst, src	$dst \leftarrow dst - src$	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
SUBX dst, src	$dst \leftarrow dst - src$	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29							4	3
SWAP dst	$dst[7:4] \leftrightarrow dst[3:0]$	R		F0	X	*	*	X	–	–	2	2
		IR		F1							2	3

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 119. Opcode Map Abbreviations

Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 121. DC Characteristics (Continued)

Symbol	Parameter	T _A = -40°C to +105°C (unless otherwise specified)			Units	Conditions
		Minimum	Typical	Maximum		
I _{LED}	Controlled Current Drive	1.8	3	4.5	mA	{AFS2,AFS1} = {0,0}.
		2.8	7	10.5	mA	{AFS2,AFS1} = {0,1}.
		7.8	13	19.5	mA	{AFS2,AFS1} = {1,0}.
		12	20	30	mA	{AFS2,AFS1} = {1,1}.
C _{PAD}	GPIO Port Pad Capacitance	–	8.0 ²	–	pF	
C _{XIN}	X _{IN} Pad Capacitance	–	8.0 ²	–	pF	
C _{XOUT}	X _{OUT} Pad Capacitance	–	9.5 ²	–	pF	
I _{PU}	Weak Pull-up Current	30	100	350	μA	V _{DD} = 3.0V–3.6V.
V _{RAM}	RAM Data Retention Voltage	TBD			V	Voltage at which RAM retains static values; no reading or writing is allowed.

Notes:

1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.

Ordering Information

Order your F0823 Series products from Zilog using the part numbers shown in Table 135. For more information about ordering, please consult your local Zilog sales office. The [Sales Location](#) page on the Zilog website lists all regional offices.

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 8 KB Flash, 10-Bit Analog-to-Digital Converter								
Standard Temperature: 0°C to 70°C								
Z8F0823PB005SG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005SG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005SG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005SG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005SG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005SG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005SG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005SG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005SG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package
Extended Temperature: -40°C to 105°C								
Z8F0823PB005EG	8 KB	1 KB	6	12	2	4	1	PDIP 8-pin package
Z8F0823QB005EG	8 KB	1 KB	6	12	2	4	1	QFN 8-pin package
Z8F0823SB005EG	8 KB	1 KB	6	12	2	4	1	SOIC 8-pin package
Z8F0823SH005EG	8 KB	1 KB	16	18	2	7	1	SOIC 20-pin package
Z8F0823HH005EG	8 KB	1 KB	16	18	2	7	1	SSOP 20-pin package
Z8F0823PH005EG	8 KB	1 KB	16	18	2	7	1	PDIP 20-pin package
Z8F0823SJ005EG	8 KB	1 KB	22	18	2	8	1	SOIC 28-pin package
Z8F0823HJ005EG	8 KB	1 KB	22	18	2	8	1	SSOP 28-pin package
Z8F0823PJ005EG	8 KB	1 KB	22	18	2	8	1	PDIP 28-pin package

Table 135. Z8 Encore! XP F0823 Series Ordering Matrix (Continued)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Description
Z8 Encore! XP F0823 Series with 1 KB Flash								
Standard Temperature: 0°C to 70°C								
Z8F0113PB005SG	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005SG	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005SG	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005SG	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005SG	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005SG	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005SG	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005SG	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005SG	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package
Extended Temperature: -40°C to 105°C								
Z8F0113PB005EG	1 KB	256 B	6	12	2	0	1	PDIP 8-pin package
Z8F0113QB005EG	1 KB	256 B	6	12	2	0	1	QFN 8-pin package
Z8F0113SB005EG	1 KB	256 B	6	12	2	0	1	SOIC 8-pin package
Z8F0113SH005EG	1 KB	256 B	16	18	2	0	1	SOIC 20-pin package
Z8F0113HH005EG	1 KB	256 B	16	18	2	0	1	SSOP 20-pin package
Z8F0113PH005EG	1 KB	256 B	16	18	2	0	1	PDIP 20-pin package
Z8F0113SJ005EG	1 KB	256 B	24	18	2	0	1	SOIC 28-pin package
Z8F0113HJ005EG	1 KB	256 B	24	18	2	0	1	SSOP 28-pin package
Z8F0113PJ005EG	1 KB	256 B	24	18	2	0	1	PDIP 28-pin package

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